# TRG readout

TRG/DAQ workshop Yonsei University 20190828 H. Nakazawa (NTU)

### **Event buffer problems**

- For CDCTRG and GDL
- Data truncation
  - 1st several bytes (sometimes a few words) missing
  - <0.3% for GDL. If ~1%, we won't use the FW.
- Shift of clock cycle
  - Recovered by reboot. Less likely happens.
- Event slip
  - Happens during run.
- Raw data quality checker
  - feature/trgrawdata

## The bug

- When readout for an event is done, readout for the next event must not start 23 clocks because of B2L design
- This requirement has been properly implemented for waiting events, but not for other events.

Normal re	adou	ıt	Event with data Event with header only						
∾ cb2.ren	0000 0000		00000000						
⊶ eb. if ul lent	2872 2873								
∾ cb.sis_b2lout	ET 23	<u>}</u>							
⊶ ch. addr_i	005 00								
⊶ cb.eddr_o	0AE 0AI								
🗢 cb. b2 l_readont	070 07		000						
⊶ cb. dbuf . addr_i	23 20								
∾cb.dbuf.addr u	15 1		<u>X 18 X 00 X02( c0 % FX 00 X03( 00 X1c( cc %0)X 00 X0FX 00 X1c( cc %1BX 00 X6X 00 X13X 00 X11X</u>						
🗠 eb. dbut . b2 lent	UE2 UE4	2	02FX_\J2F\_\02FX_\02FX_\J2F\_\02FX\02FX_\0						
obClent_contting	1								
- ch2lenn_hont tirs	1	I							
⊶ cb. <b>r_order</b>	01 0		) J2 X OJ X O5 X O6 X O7 X J0 X C9 X OA X JJ X OG X						
- cb.nworking	12 13	12	<u>13 (17 (11 ) 10 ) 3 ( 8 ) 7 ) 5 ) 4 ( 3 ) 7 ) 1 )</u>						
⊶ <mark>cb.nwaiting</mark>	11 I		<u>12 (11 ) 10 9 8 ) 7 ) 6 ) 5 ) 4 ) 3 (2 ) 1 )</u>						
e∽ cultrs	C8B00 58B0	<u>583008 X</u>	58B00C						
⊶ cb3.reg_henttrg	£8800, 2880		£8EC00						
← cb0.res_denttrs	50AFT 50AF		58AFFF						
∾ cnttr≰	58B00 58B0	58-00B X	58B00C						
- conL1	0		13th trigger Event number in header						
H. Nakazawa			3						

#### **Test OK**

- Dummy 30 kHz with 2 usec event separation
- GDL + skeleton 3Ds
- Will test with other modules when ready
  - Large dead time at 10 kHz solved?
- Struggling with compiling latest 2D
  - Clocks unified. This caused difficulty?

	hdrok	data ok	hdr bad	data bad	bad#wd	dd shift	ccdisodr	cc ok
2D0	0	0	Θ	Θ	Θ	Θ	Θ	0
2D1	0	0	Θ	0	0	0	0	0
2D2	0	0	Θ	0	0	0	0	0
2D3	0	0	Θ	0	0	Θ	0	0
3D0	221082	3505	Θ	0	0	Θ	0	3505
3D1	221082	3505	Θ	0	0	Θ	0	3505
3D2	221082	3505	Θ	0	0	0	0	3505
3D3	221082	3505	Θ	0	0	0	0	3505
NNO	0	0	Θ	0	0	0	0	0
NN1	0	0	Θ	0	Θ	0	0	0
NN2	0	0	Θ	0	Θ	0	0	0
NN3	0	0	0	0	Θ	0	0	0
SL0	0	0	0	0	0	0	0	0
SL1	0	0	0	0	0	0	0	0
SL2	0	0	Θ	0	0	Θ	0	0
SL3	0	0	0	0	Θ	0	0	0
SL4	0	0	0	0	Θ	0	Θ	0
SL5	0	0	0	0	Θ	0	0	0
SL6	0	0	0	0	Θ	0	0	0
GDL	0	224587	0	0	Θ	0	0	224587
ETF	0	0	Θ	Θ	Θ	Θ	0	0
							242,1	末属

#### **GDL full readout**

- For debugging
- At present, integrated (127MHz -> 32MHz) data.
  Logic consistency partially lost.
- Suppress mode?
- Readout through dedicated UT3 (GDL->one readout UT3-> 4\*B2L)
  - Koga-san started FW implementation
- Copper and hslb15003a,3b,4a,4b ready by Yamada-san
  - Can login from trg01
- trg03 is there. PS=4 if only trg03.
- Negotiation on FTSW
- SC

#### Last page

- DAQ group is timing monitor in b2tt code to solve ttlost
- Plan to detect busy on GDL with chipscope