TRG readout

TRG/DAQ workshop
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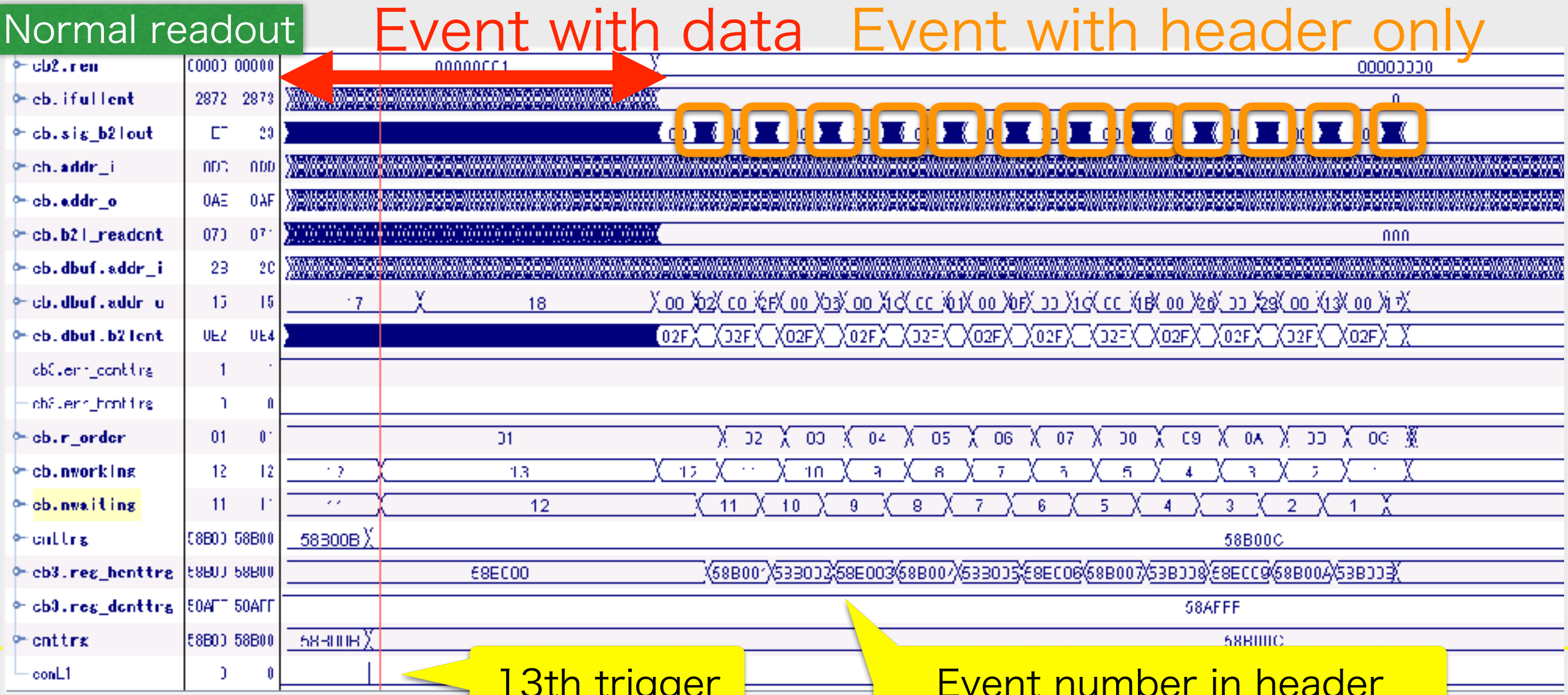
Event buffer problems

- For CDCTRG and GDL
- Data truncation
  - 1st several bytes (sometimes a few words) missing
  - <0.3% for GDL. If ~1%, we won't use the FW.
- Shift of clock cycle
  - Recovered by reboot. Less likely happens.
- Event slip
  - Happens during run.
- Raw data quality checker
  - feature/trgrawdata

The bug

- When readout for an event is done, readout for the next event must not start 23 clocks because of B2L design
- This requirement has been properly implemented for waiting events, but not for other events.



Test OK

- Dummy 30 kHz with 2 usec event separation
- GDL + skeleton 3Ds
- Will test with other modules when ready
  - Large dead time at 10 kHz solved?
- Struggling with compiling latest 2D
  - Clocks unified. This caused difficulty?

	hdr ok	data ok	hdr bad	data bad	bad#wd	dd shift	ccdisodr	cc ok
2D0	0	0	0	0	0	0	0	0
2D1	0	0	0	0	0	0	0	0
2D2	0	0	0	0	0	0	0	0
2D3	0	0	0	0	0	0	0	0
3D0	221082	3505	0	0	0	0	0	3505
3D1	221082	3505	0	0	0	0	0	3505
3D2	221082	3505	0	0	0	0	0	3505
3D3	221082	3505	0	0	0	0	0	3505
NN0	0	0	0	0	0	0	0	0
NN1	0	0	0	0	0	0	0	0
NN2	0	0	0	0	0	0	0	0
NN3	0	0	0	0	0	0	0	0
SL0	0	0	0	0	0	0	0	0
SL1	0	0	0	0	0	0	0	0
SL2	0	0	0	0	0	0	0	0
SL3	0	0	0	0	0	0	0	0
SL4	0	0	0	0	0	0	0	0
SL5	0	0	0	0	0	0	0	0
SL6	0	0	0	0	0	0	0	0
GDL	0	224587	0	0	0	0	224587	
ETF	0	0	0	0	0	0	0	0

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GDL full readout

- For debugging
- At present, integrated (127MHz -> 32MHz) data.
  Logic consistency partially lost.
- Suppress mode?
- Readout through dedicated UT3 (GDL->one readout UT3-> 4*B2L)
  - Koga-san started FW implementation
- Copper and hslb15003a,3b,4a,4b ready by Yamada-san
  - Can login from trg01
  - trg03 is there. PS=4 if only trg03.
  - Negotiation on FTSW
  - SC

Last page

- DAQ group is timing monitor in b2tt code to solve ttlost
- Plan to detect busy on GDL with chipscope