Event buffer problems

- For CDCTRG and GDL
- Data truncation
  - 1st several bytes (sometimes a few words) missing
  - <0.3% for GDL. If ~1%, we won't use the FW.
- Shift of clock cycle
  - Recovered by reboot. Less likely happens.
- Event slip
  - Happens during run.
- Raw data quality checker
  - feature/trgrawdata
The bug

- When readout for an event is done, readout for the next event must not start 23 clocks because of B2L design.
- This requirement has been properly implemented for waiting events, but not for other events.
Test OK

- Dummy 30 kHz with 2 usec event separation
- GDL + skeleton 3Ds
- Will test with other modules when ready
  - Large dead time at 10 kHz solved?
- Struggling with compiling latest 2D
  - Clocks unified. This caused difficulty?
GDL full readout

- For debugging
- At present, integrated (127MHz -> 32MHz) data. Logic consistency partially lost.
- Suppress mode?
- Readout through dedicated UT3 (GDL->one readout UT3-> 4*B2L)
  - Koga-san started FW implementation
- Copper and hslb15003a,3b,4a,4b ready by Yamada-san
  - Can login from trg01
- trg03 is there. PS=4 if only trg03.
- Negotiation on FTSW
- SC
• DAQ group is timing monitor in b2tt code to solve ttlost
• Plan to detect busy on GDL with chipscope