

TRG software issues

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TRG software issues

| Package details | | | | | | | | | |
|-----------------|---------------|--------------|--------------------|--------------------|---------------|-------------|------------------|--------------|----------------|
| Package | Librarian | Build Result | Intel Build Result | Clang Build Result | Cppcheck | Test Result | Geometry Doxygen | Sphinx | Dependencies |
| trg | Yun-Tsung Lai | OK | OK | Warnings: 2 | Warnings: 892 | 0/2, 0/1 | OK | Missing: 437 | OK Extra: 1 |

- Missing documentation: ~2000 → 437 in this month.
- What remains:
 - GDL unpacker, DQM, DB, etc.
 - xsi_loader: Xilinx package for firmware co-simulation.
 - trg/scripts/bitstring.py
- I will start to work on Cppcheck error step-by-step.

TRG software issues (cont'd)

- Same interface (TRGSummary/TrgBit) to access trg bits in TSIM and data.
 - BII-4853/BII-5287/PR 4558
- BII-5347: Event t0 error message
 - [ERROR] No binned event t0 available for the given detector. Returning 0.
{ module: TRGGRLProjects }
- Introducing short tracking algorithm in fast TSIM.
- Other software tasks?