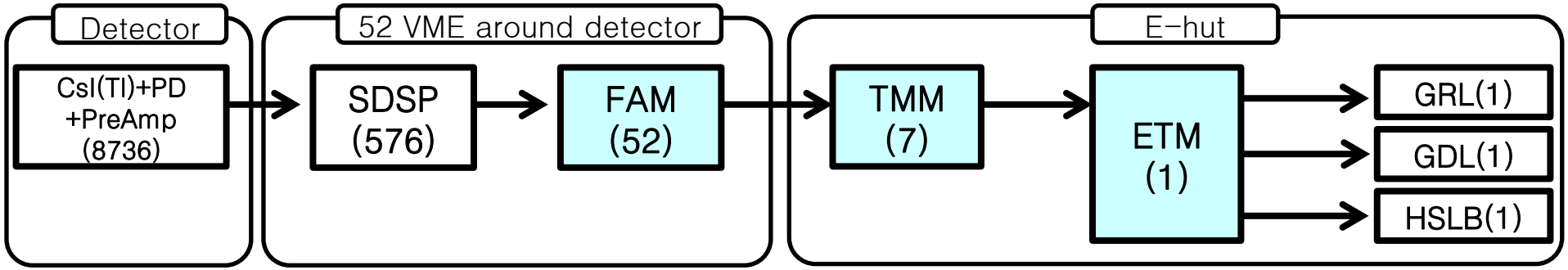
ECL Trigger Summary

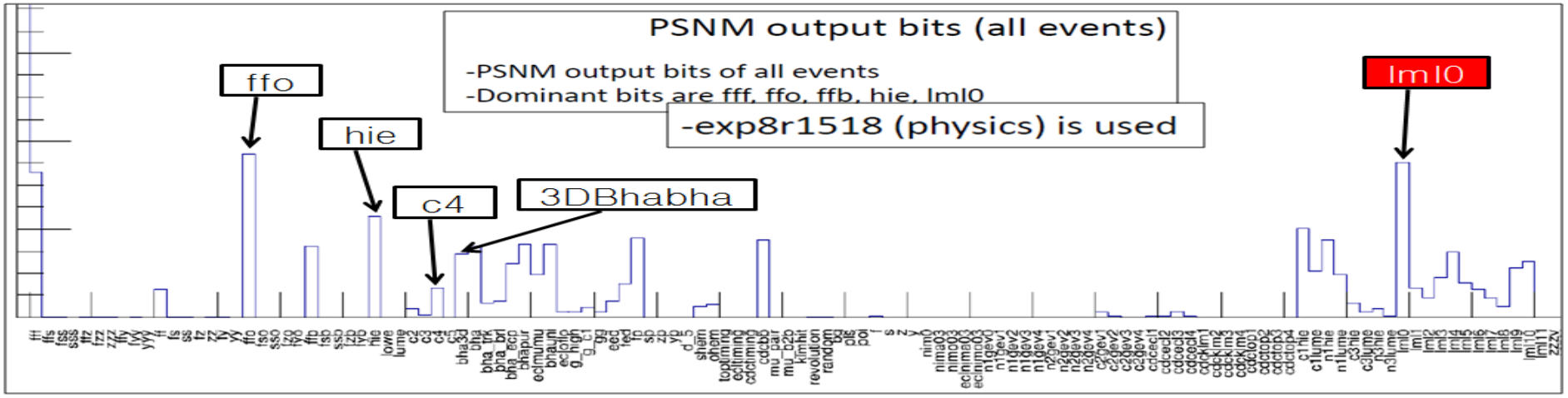
Y.Unno
Hanyang univ.
TRG/DAQ workshop
2019/08/26-29

Belle2 ECL trigger system



- FAM
  - Receive 576TC analog data from ShaperDSP
    - 1TC consists of 4x4=16Xtals
  - Digitization with FADC
  - TC E&T rec. by waveform analysis(χ^2 fit) on kintex7
- TMM
  - Play an role of merger on kintex7
- ETM
  - ECL trigger decision by all TC E&T on virtex6
  - Send ECL trigger summary to GDL
  - Send cluster data to GRL
  - Send fired TC E&T and trigger summary to HSLB

3 cluster trigger



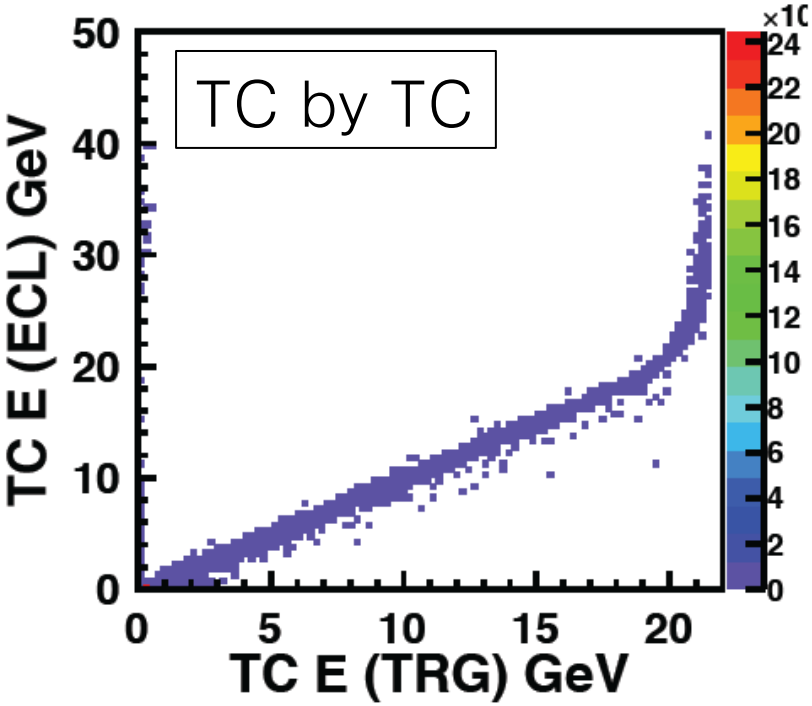
- New 3 cluster trg(lml12) proposed by Chris.
  - Trigger rate → 1/4
  - ε(τ) to 87.6% from 89.5%
    - τ group is checking if it's ok or not.
- L1 will be issued by "lml0.OR.lml12" during autumn run
- hie will be highest in ecltrg bit
  - Could be highest in trigger bit after z-trg is ready
  - Need new hie(?) or alternative bit in the near future

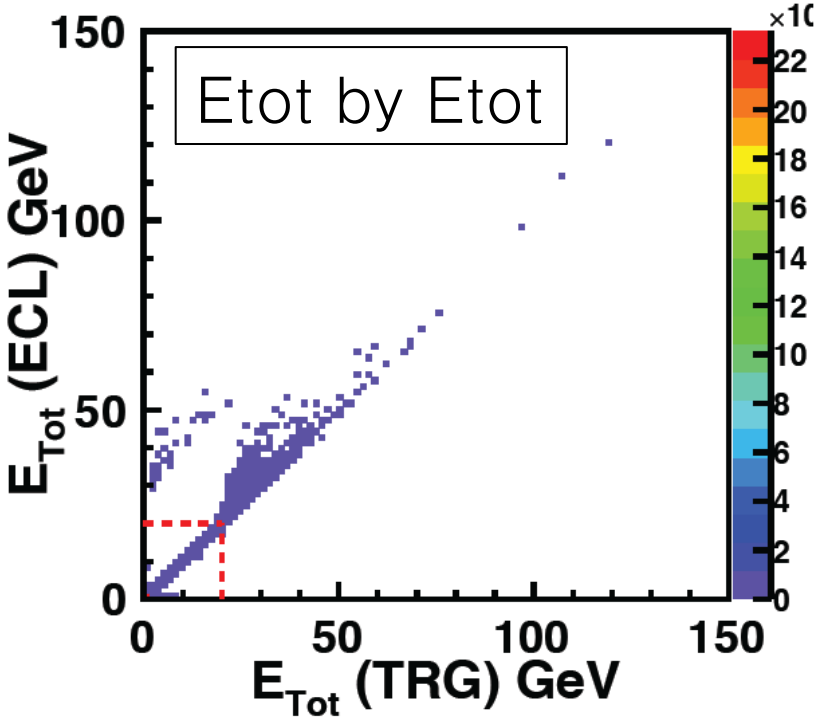
ecl_bst bit (Etot>20GeV)

- To avoid ERROR in ECL by vetoing “ECL burst” events
  - ecl_bst was prepared and tested in beam data
  - Found ECL and ecltrg data inconsistency…
- ECL prepared FW to avoid the ERROR w/o ecl_bst veto…
- Requested to activate ecl_bst bit from Alex since
  - The event will not be used in physics analysis
  - might be useful to avoid ERROR in other sub-detector
  - Can CDCTRG provide similar bit !?
- Decided to record ecl_bst during autumn run w/o veto

ECL and ecltrg data consistency

- O(0.01%) data inconsistency are found
  - Both in cosmic and beam data
  - Both in TC by TC, and evt by evt data comparison





- More detail study is necessary.

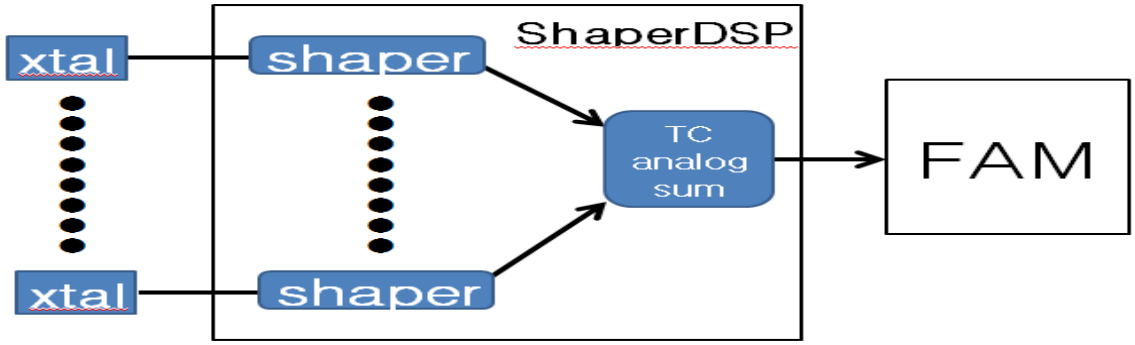
3D Bhabha veto bit

- 3D Bhabha logic is available on GDL during Phase2.
- 2D is used in GDL, but 2D and 3D recorded w/o pre-scale
- Need an approval from belle2 collaboration based on data
- Asking the approval for physics groups.
  - JIRA ticket(https://agira.desy.de/browse/BIIOPS-8)
  - Chris quickly checked beam data
    - Bhabha and $\gamma\gamma$ efficiencies are OK
    - For $\pi\pi\gamma$, 3D is much better than 2D
  - τ group approved
    - https://agira.desy.de/secure/attachment/29730/29730_Tau_L1BhabhaVeto_28June2019.pdf
  - Waiting for approval from low multi and dark sector physics group

- (I think) 3D will be used from autumn run.

TC timing problems

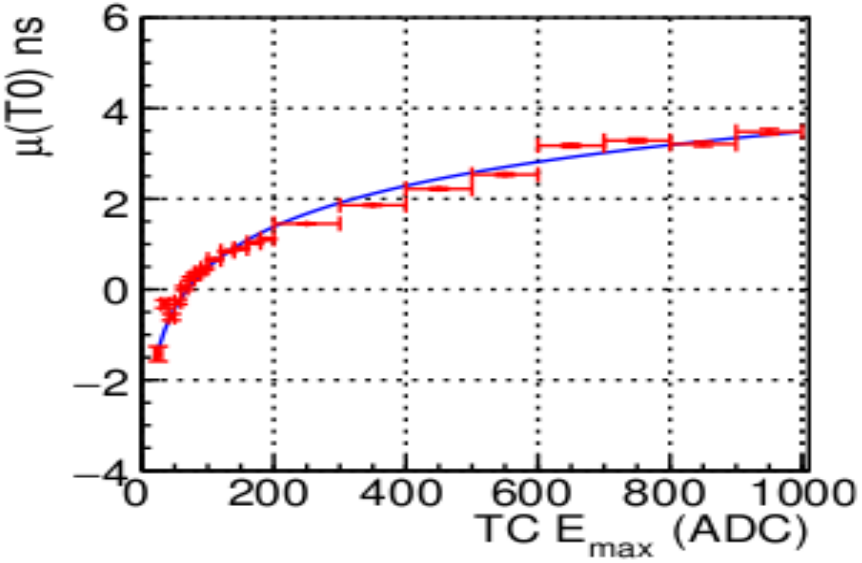
- Timing source in spring run was only ECL trigger
- TC Timing problems from Phase2
  - ① run by run TC timing shift due to 3 bugs in FAM
    - ➔ All fixed, TC T calibration is possible.
  - ② Large TC timing resolution than expected
    - σ(T)~6ns in data, but ~1ns in tsim for Bhabha event

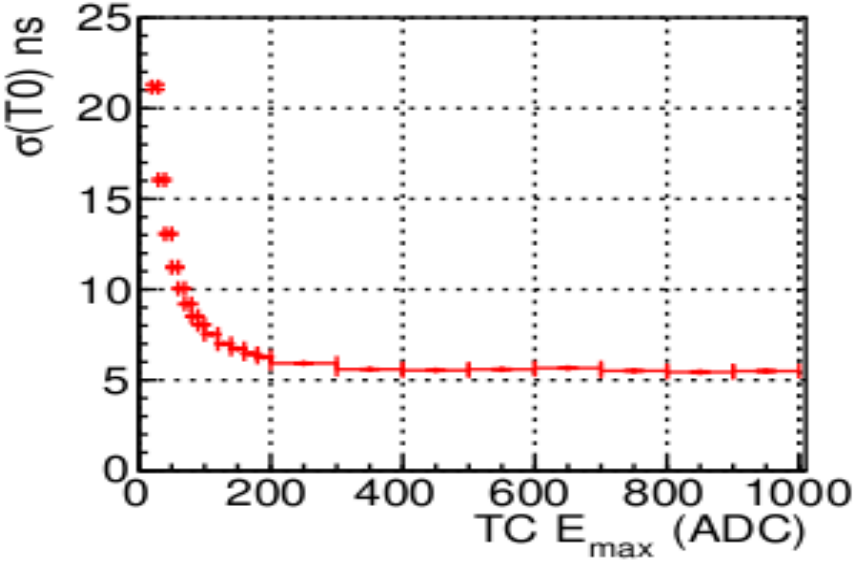


    - Xtal ch by ch timing adjustment is not possible…
    - Need to implement the effect into tsim
  - ③ TC timing bias from fitter on FAM
    - ~5ns shift as function of energy (+ noise)
    - → not started yet

TC timing problems

- Offline (CDC based) eventT0 for hadron skim





- Bias comes from fitter
- Depends on TC E and noise
- Bias correction is possible after fitter on FAM

- Large resolution in low E deposition
- Difficult to improve TC T resolution
- TC energy weighted event T0 on ETM would improve the resolution

- Progress / improvement on timing resolution are necessary
  - if TOP and CDC need much more time to provide timing

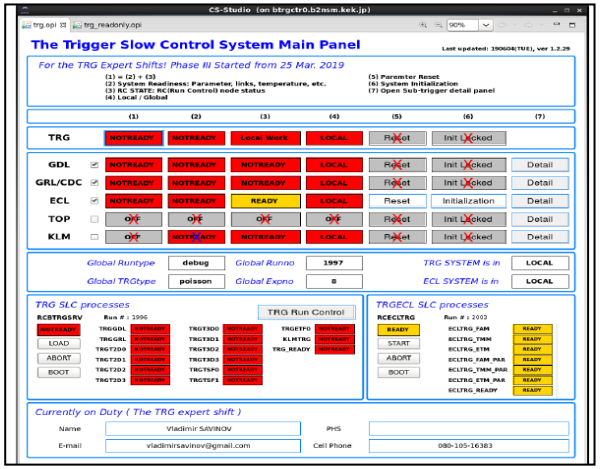
TC E and T calibration

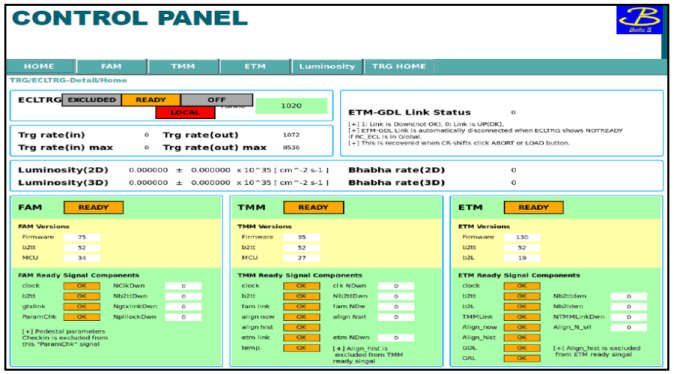
- Energy calibration
  - calibration was NOT possible during Phase2
    - Run by run energy fluctuation was fixed by ECL expert
  - Xtail ch by ch (~9000Xtal) calibration using ecltrg & ECL
    - Gain tuning by ~9000 attenuators on ShaperDSPs
  - Energy resolution became 2 times better

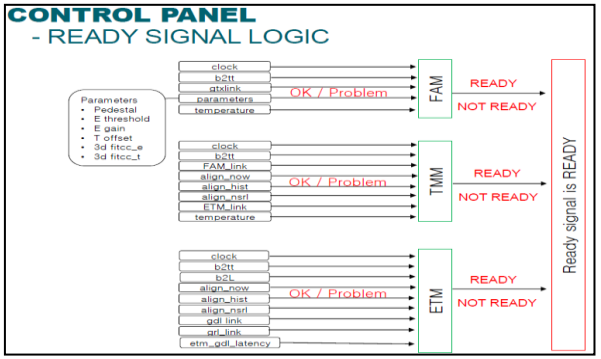
- TC Timing calibration
  - Not possible until near end of spring run
    - TC timing fluctuated run by run due to bugs on FAM…
  - Variation of CC became much smaller than before
  - Effect on event timing will be checked with eventT0

- Confirmed methods of E and T calibration worked well
  - Modularizing calibration programs

Slow control







- Developed by C.H.Kim/E.J.Jang. Worked in phase3 very well.
  - SLC status check and recovery procedure
  - Manual for trg and ecltrg experts worked well too.
- Provides “ecl trg ready” signal, checking many pars continuously.
- Worked well to store/read 60k parameters to/from configuration DB
- Fully utilize archiver to check important parameters
  - TC hit rate, TC noise, temp., trg rate of each bit, etc.
  - Par check not only by CSS but also by CUI (Thx to Seohkee, Sungin)
- Some issues(e.g. initialization button didn’t work), but we are on fine tuning stage.

software

Update for Release 04-00

- Unpacker Update
  - Add ecl-burst bit
- Condition DB update
  - Modify ADC conversion factor(int -> double)
  - Selection bhabha condition
  - $\mu\mu$ bit condition
  - ECL burst bit
  - The number of Cluster exceeding 300 MeV
- Calibration Module
  - Timing calibration module
- QAM
  - Basf2 base QAM
  - Add few variables
    - ECLTRG Total Energy peak and width
    - ECLTRG Cal-timing peak and width
    - ECLTRG Cluster Energy peak and width
    - Low Hit TC (Less than 0.1 x Average) in Forward,

    Add executing scripts in examples dir.

To do list for ECL Trigger software

- Simulation
  - Background Overlay
  - Realistic timing resolution in MC
    - Crystal base shaping module has been prepared.
    - Need more study in FAM and ShaperDSP.
  - Integer version
  - Firmware version
- ECL Trigger Unpacker
  - Update with ETM firmware.
- Calibration Module
  - Energy calibration Module.
- Condition DB update
  - Configuration DB → Condition DB system is needed

Summary

- ECL trigger system worked stably during phase3
- Many progresses in spring run and summer
  - New 3 cluster trigger and ecl_bst are ready
  - 3D Bhabha would be used from autumn urn
  - Big timing problems were understood and fixed.
  - TC E and T calibration worked as expected
  - SLC system in fine tuning stage

- many to-do items remains still
  - Will be done before(or during) autumn run

backup

To-do list

- Firmware (FAM)
  - correction of TC timing bias
  - TC E and T measurements for 2 continuous signal pulses
  - Take into account injection veto for noise monitoring

- Firmware (ETM)
  - Event timing logic from most energetic TC to multiple TC
    - Simulation study is needed first to see the performance
  - Make firmware more healthy (currently > 7 strategies are needed)
  - Clustering to all from 6 cluster
  - UT3 to UT4

- Test pulse
  - Prepare test pulse analysis basf2 module
    - Analyze both ECL and ecl trigger data for TC E and T
    - New CC quickly for HW replacement(ShaperDSP, etc)
  - Investigate the reason of 2 timing peaks

To-do list

- Update of confluence of ecltrg trigger bits for other belle2 members

- Trigger rate and beam background study for high luminosity condition

- Software
  - Beam background mixing module
  - Take into account nuclear counter effect
    - (but we don't know the signal shape…)
  - ConditionDB
  - Integer/firmware tsim-ecl

- Noise related program
  - updates noise level automatically for bkg mixing module
  - updates noise covariance matrix automatically
  - check TC waveform when injection veto is off.

- Belle2 note
- Paper

To-do list

- Study for future upgrade
  - (strongly depends on upgrade of ECL HW)
  - Pure CsI option
  - New bit instead of hie(!?), which is insensitive for beam background
  - Xtal ch by ch timing correction before analog sum on ShaperDSP
  - Improve timing resolution for low energy deposition
  - (Waveform record(?) by FAM or ETM ?)

Energy calibration

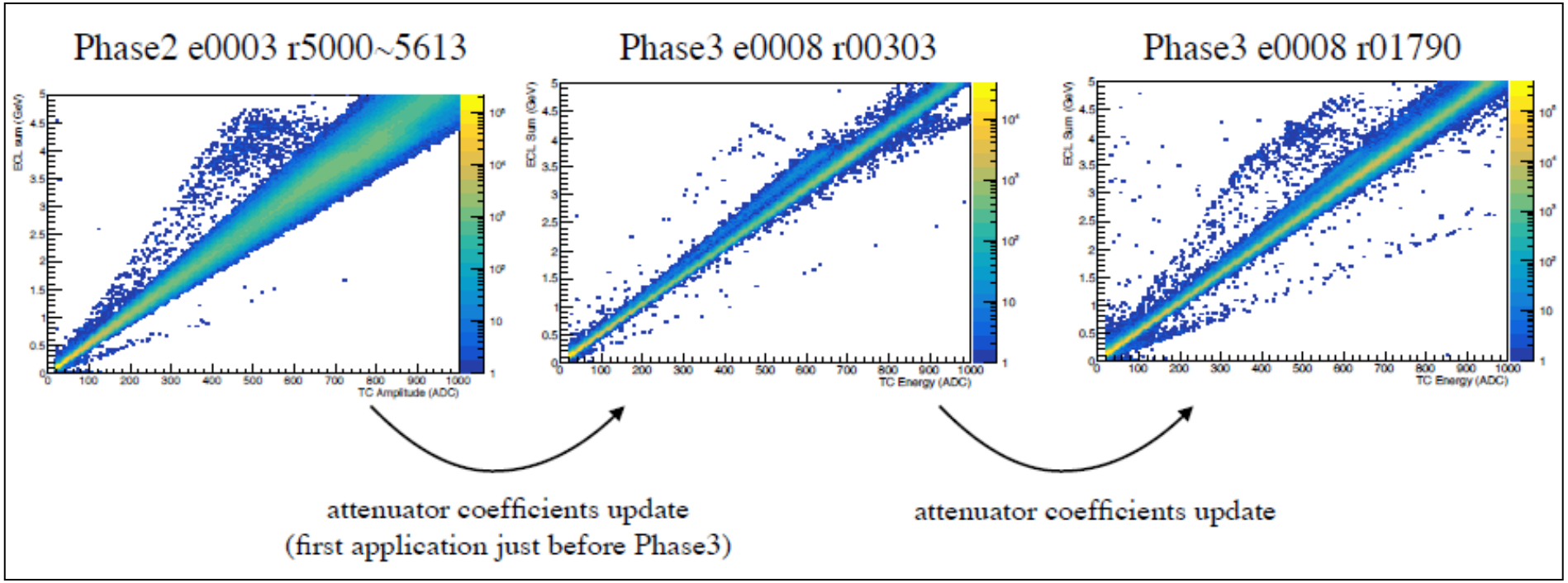
$$f(E^n, E_i^n; p_i) \equiv \sum_n (aE^n - \sum_i p_i E_i^n)^2 \rightarrow min$$

$$\frac{\partial f}{\partial p_i} = \sum_n (-2)(aE^n - \sum_j p_j E_j^n) E_i^n = 0$$

$$\rightarrow \sum_n aE^n E_i^n = \sum_n \sum_j p_j E_j^n E_i^n$$

n : event index
i, j : crystal index in TC
E^n : TC energy
E_i^n : crystal energy in TC
p_i : **Attenuator gain ratio (current / new)**
a : calibration factor (5.25 MeV / ADC)

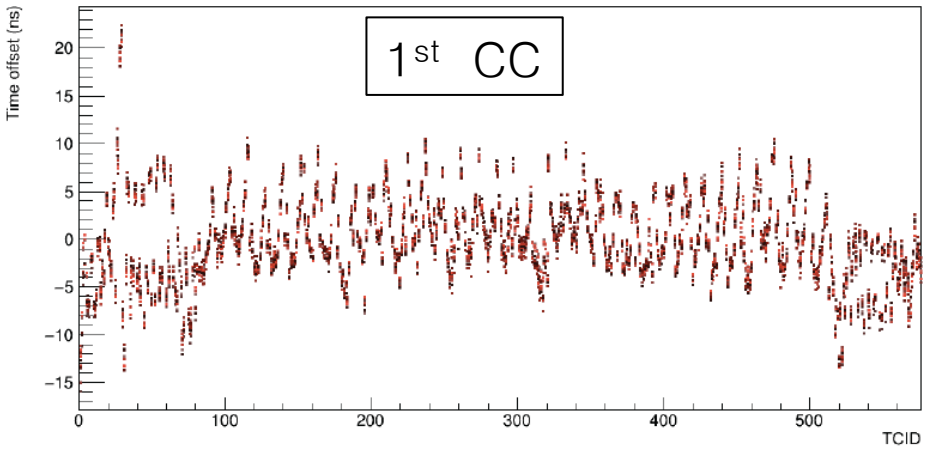
- (meaningful) calibration was possible from spring run
- Xtail ch by ch (~9000Xtal) calibration using eclltrg & ECL beam data
  - Gain tuning by ~9000 attenuators on ShaperDSPs

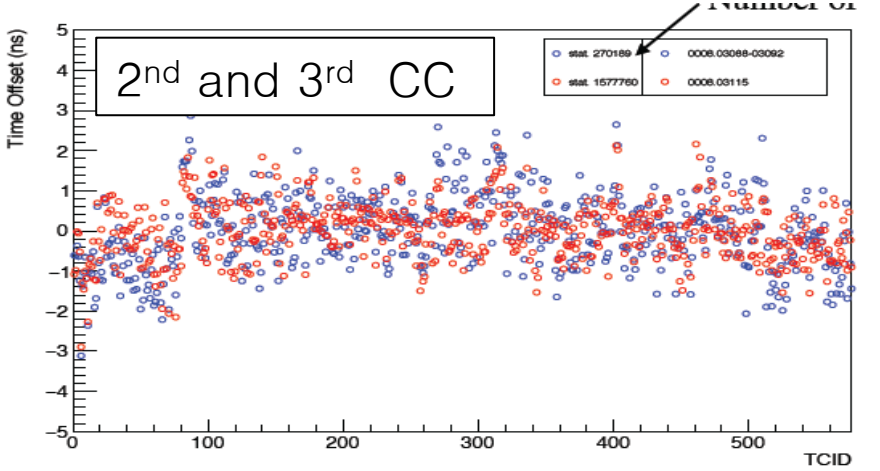


- Energy resolution became 2 times better(σ(hie) from ~50MeV to ~25MeV)
- TC energy measurement became much stable than Phase2
- Modularizing energy calibration softwares is in progress.

TC timing calibration

- **TC by TC timing calibration** was not possible until near end of spring run
  - TC timing largely fluctuated run by run due to bugs on FAM…
- Calibration was done using Bhabha samples
- TC timing correction is done in FPGA on FAM

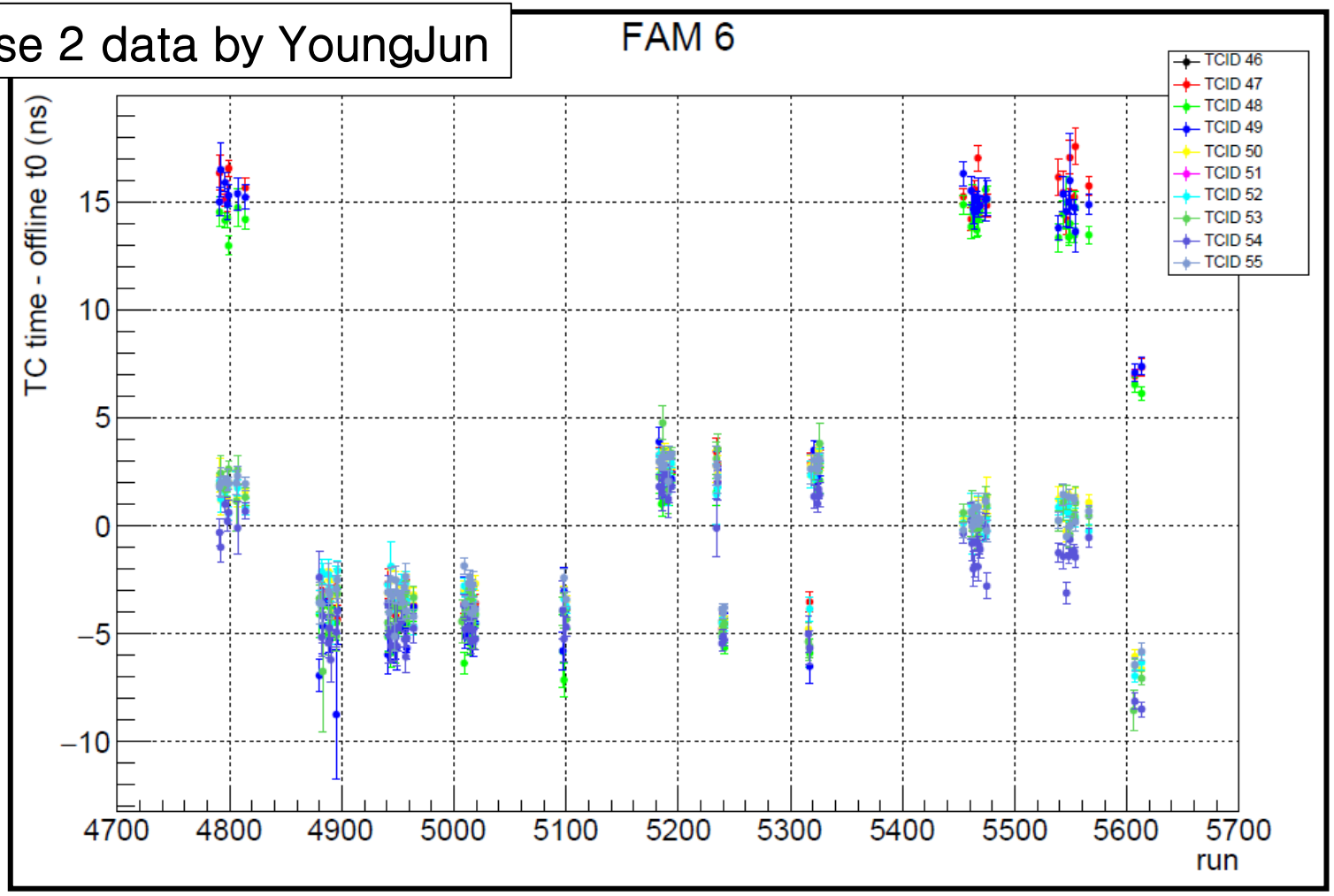




- **TC timing became much stable than before**
- **Effect on event timing will checked with CDC based eventT0 using data**
- Preparation of module for calibration with test pulse is in progress.

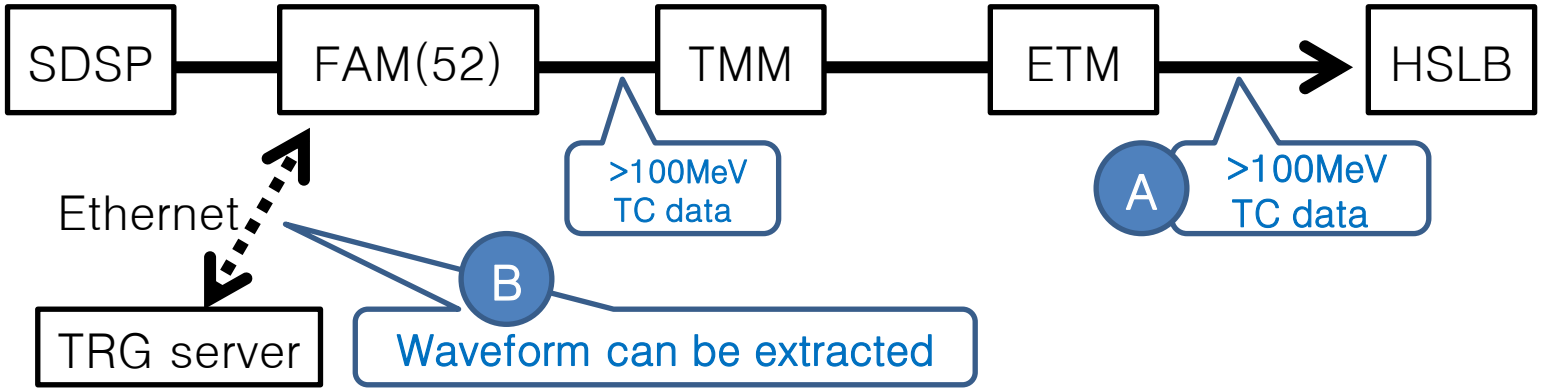
Run by run TC timing shift

Phase 2 data by YoungJun

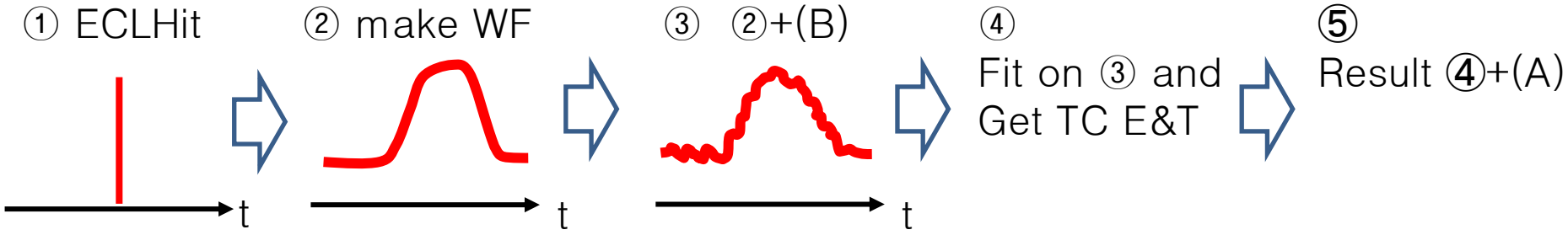


- Run by run TC timing shift even in single FAM board!
- TC timing calibration cannot be done, it's almost meaningless…

beam background overlay



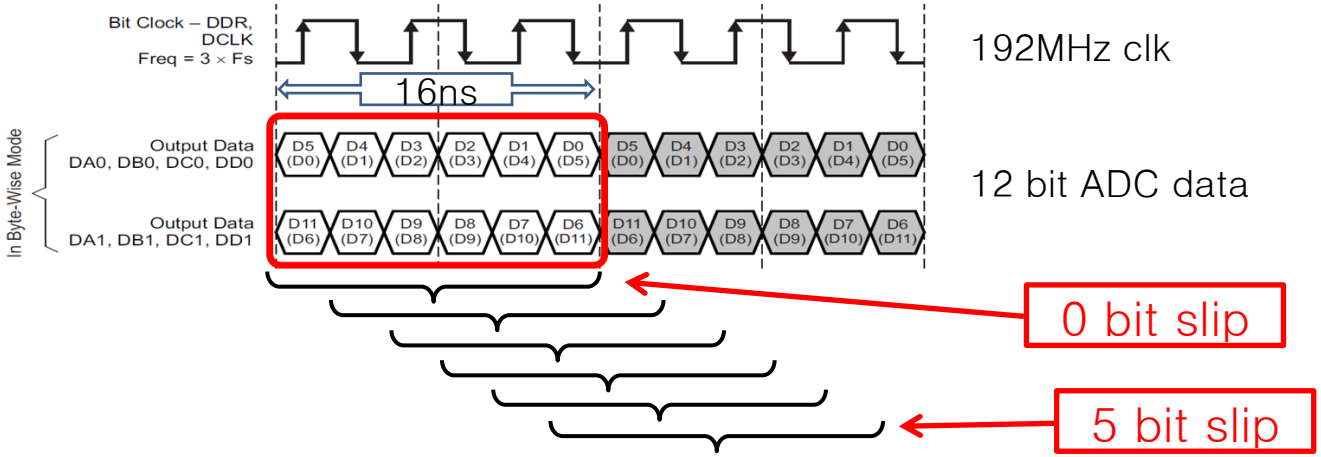
- FAM does not have b2link, no optical transceiver.
  - Difficult to take waveform data of all TC for each random trigger
- Alternative idea is to utilize data from (A) and (B)
  - (A) TC data(not WF) 100% associated with random trg by GDL
  - (B) waveform taken random trg by FAM
    - Check averaged noise level in each run and store into conditionDB



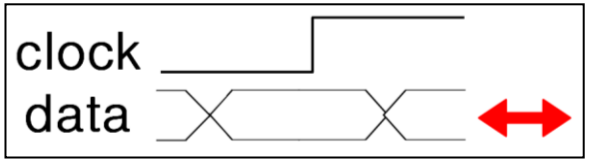
- No objection for this method in trg/soft session at last b2gm, but no actual progress since then…

Correction of bitslip and tap

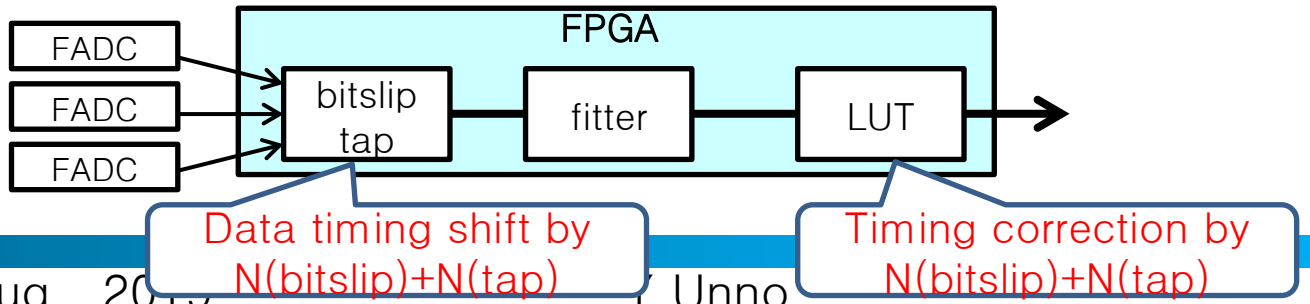
- ADC data capture by two parameters, bitslip and tap
  - bitslip: slip 12bits data by 0–5 bit (1bitslip=3ns) to find correct set of 12bit data.



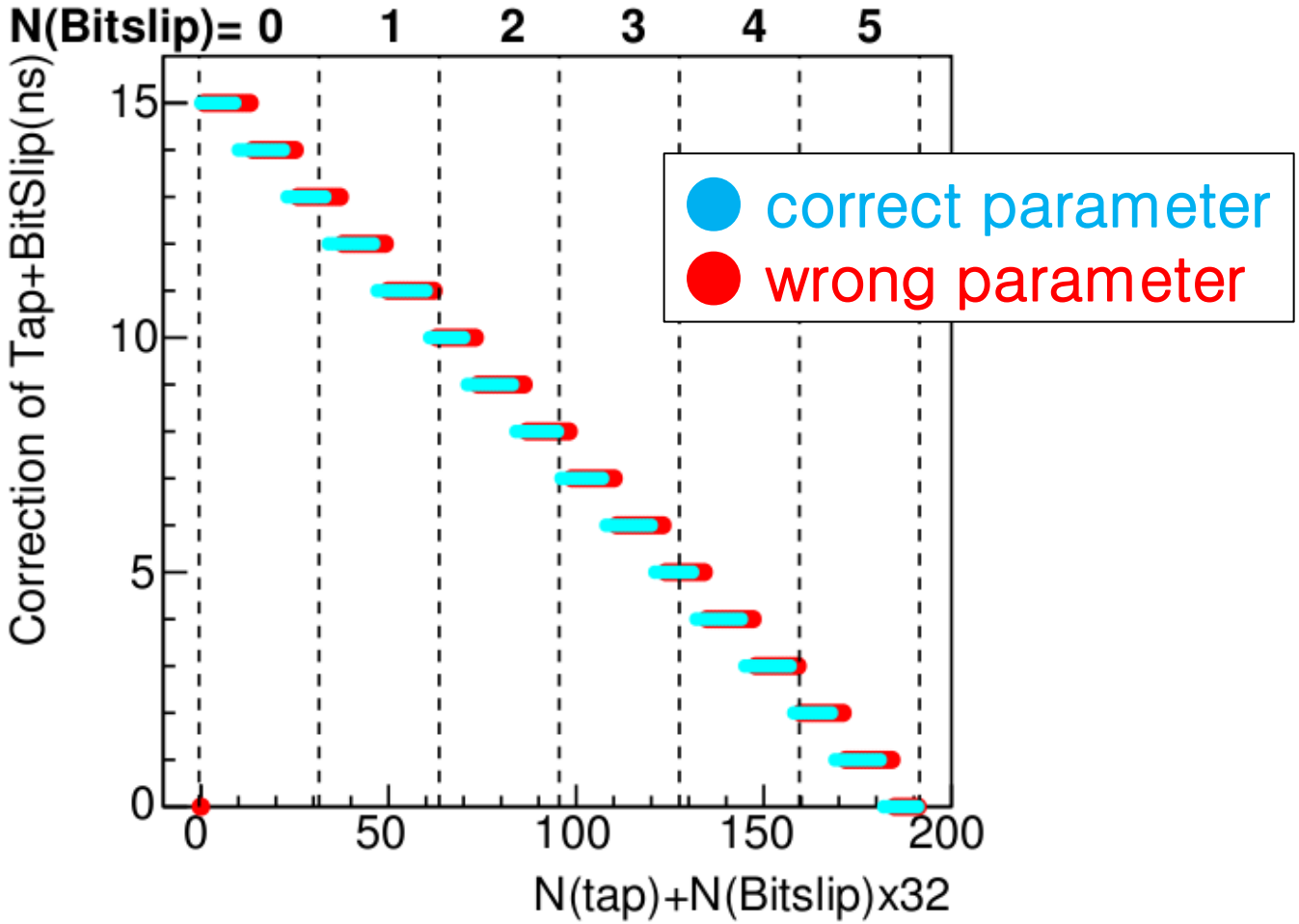
  - tap : shift ADC data with 0–31 tap(=0.0–2.3ns) with 75ps interval in order to adjust position of middle of data to clock edge(192MHz).



- Correction of data timing from N(bitslip) and N(tap)



Correction of bitslip and tap



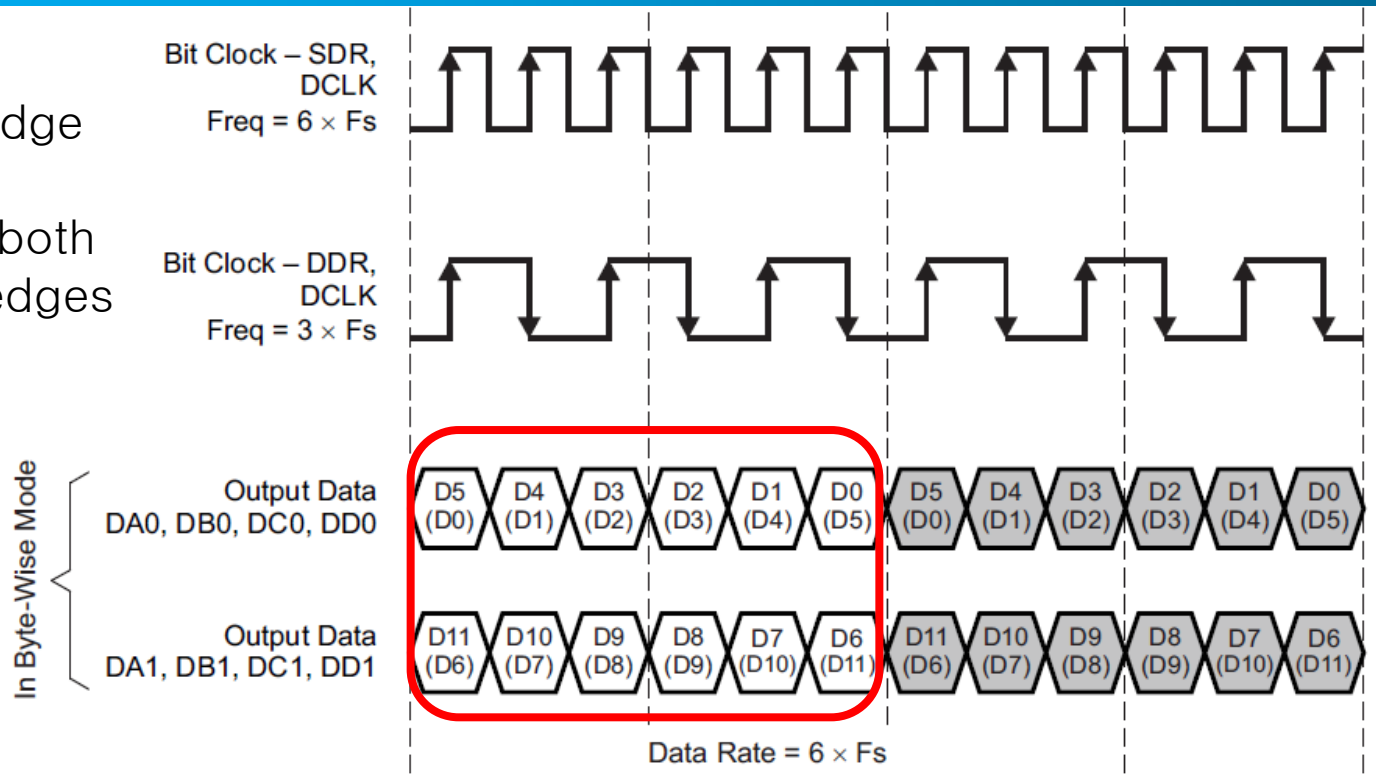
With wrong parameters, 1 or 15 ns TC timing shift happened whenever FPGA was rebooted…

Clock of ADC data capture

(A) 384MHz clk
only w/ leading edge

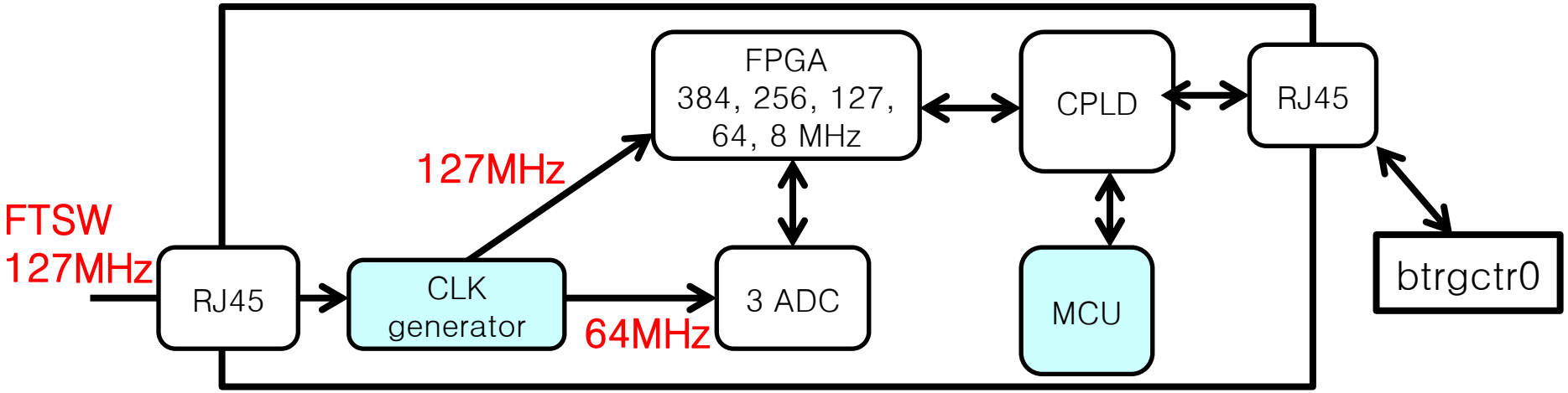
(B) 192MHz clk with both
Leading/trailing edges

ADC data



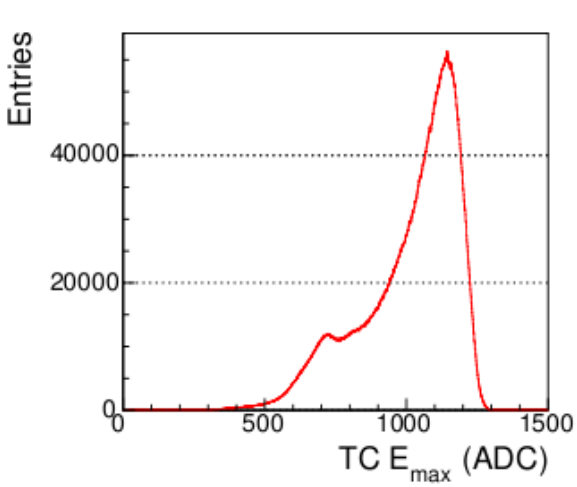
- In (B), leading edge captures odd # data, trailing captures even # data
  - Phase(0 or 180) of 192MHz is set arbitrary intentionally
  - This causes 3ns TC timing shift whenever FPGA is rebooted.
- Changed to (A) from (B) to avoid 3ns timing shift

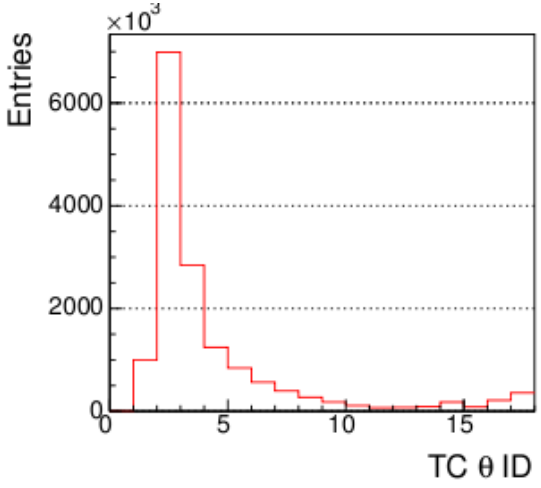
auto-reboot function in MCU

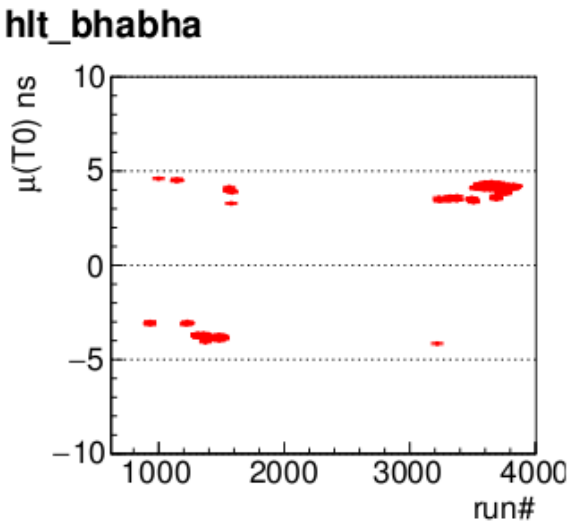


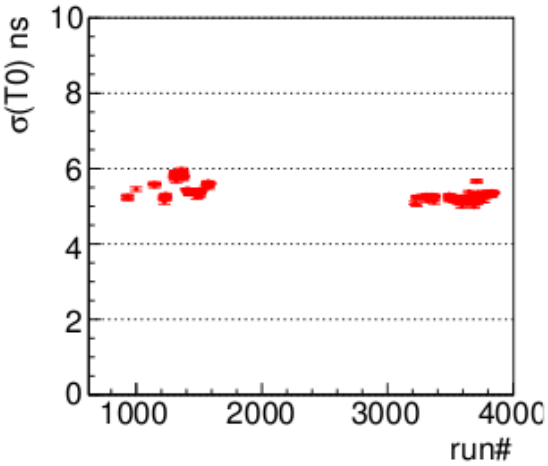
- Auto FGPA reboot function in MCU
  - when MCU detects unlocked clock (b2tt too !?),
  - it starts initialization of clock generator, and then reboot FPGA automatically.
- When FPGA reboot command is sent to MCU from btrgctr0 by user
  - (1) clock generator initialization, then (2) FGPA reboot
  - however, auto-reboot function detects clock down at (1), then
  - All are screwed up, input 127MHz and output 127, 64MHz not synchronized, then causes a few(?) ns timing shift…
  - Excluded auto-reboot function from MCU.
  - (wondering how FAM were working well so far…)

Study with offline eventT0



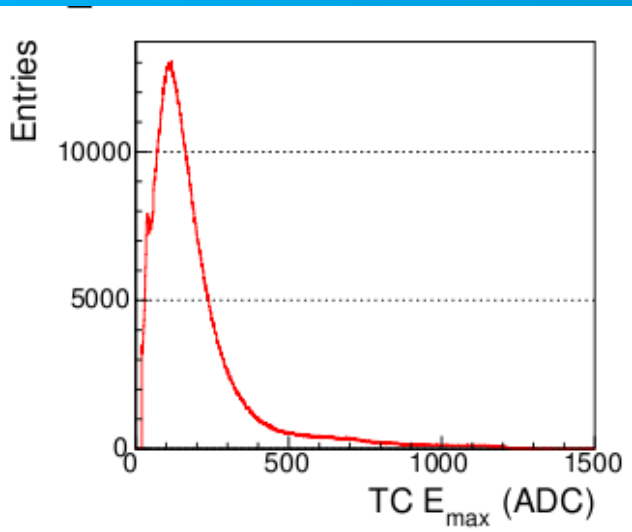


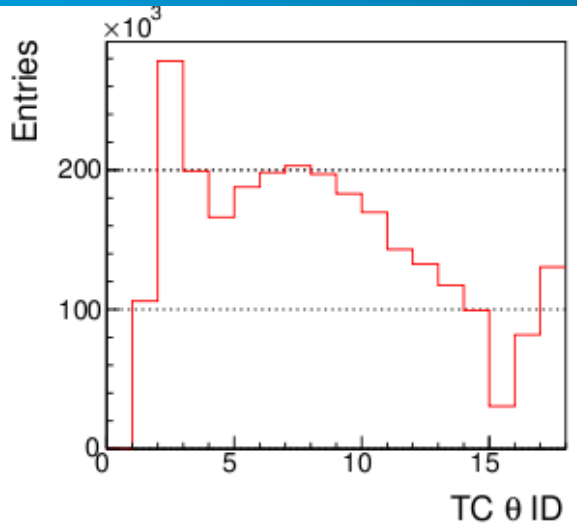


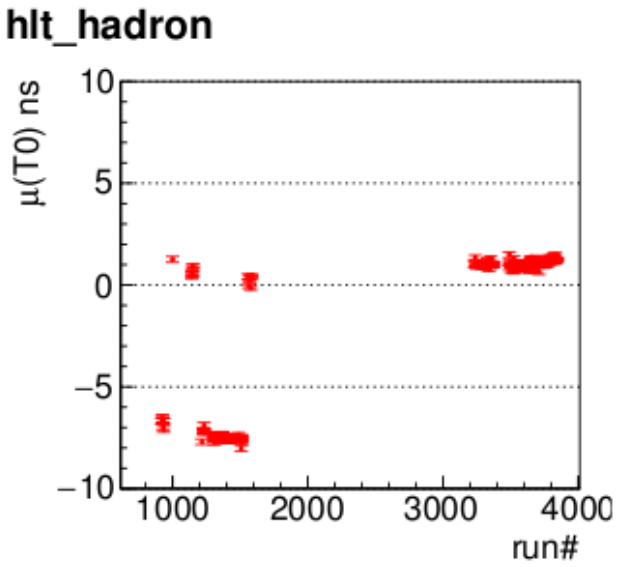


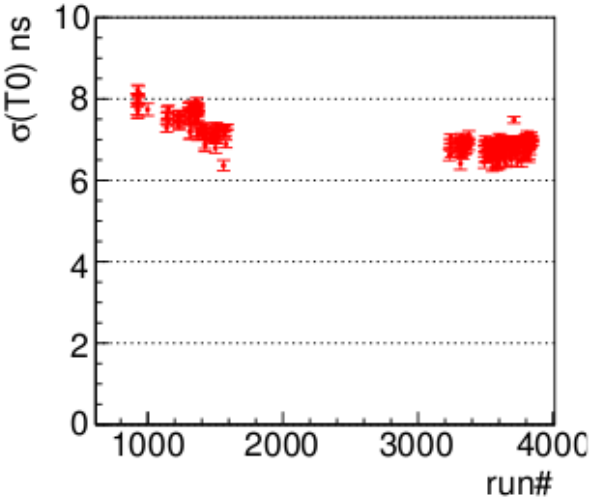
8ns timing shift is cased by GDL+FTSW (probably)

Study with offline eventT0

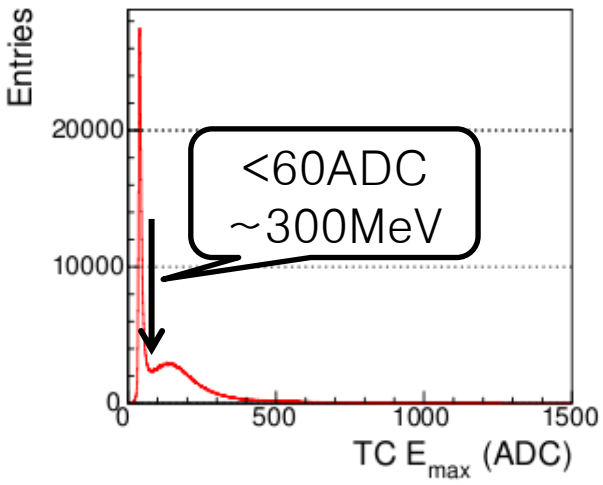


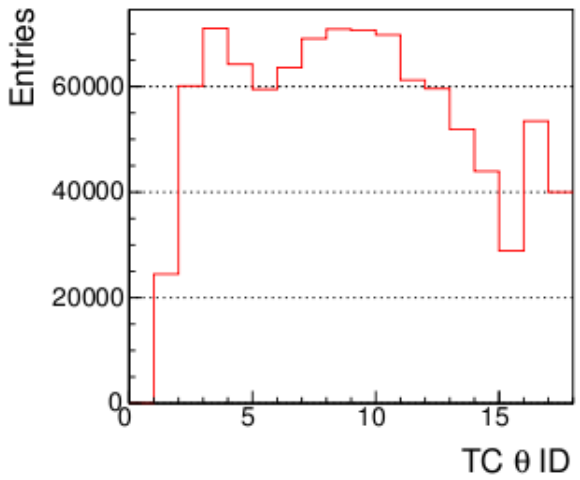


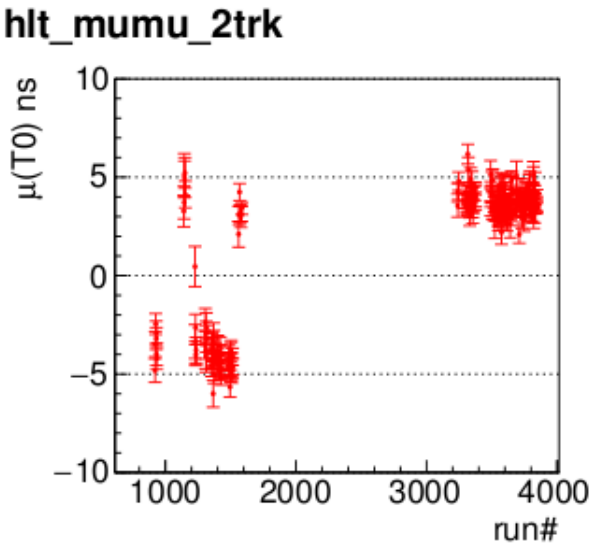


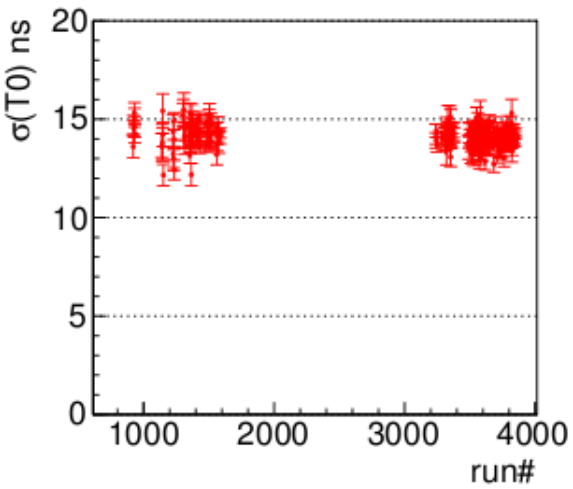


Study with offline eventT0



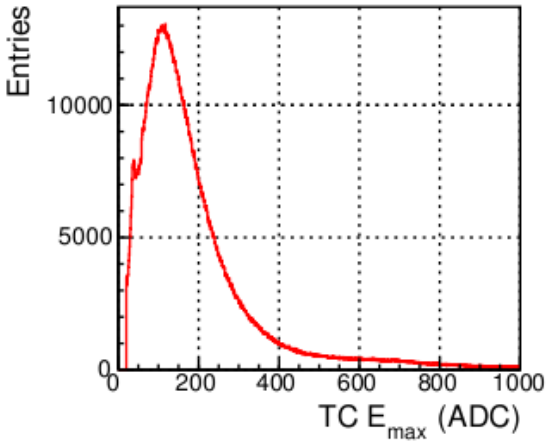


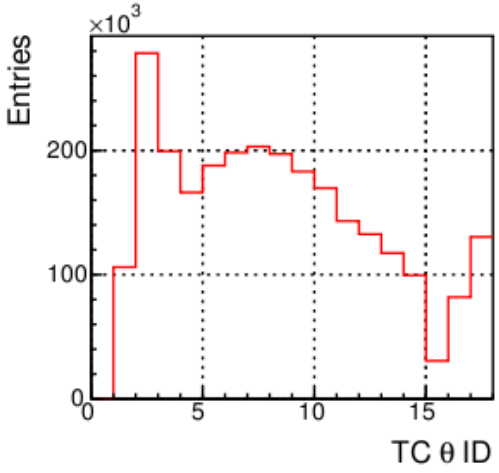


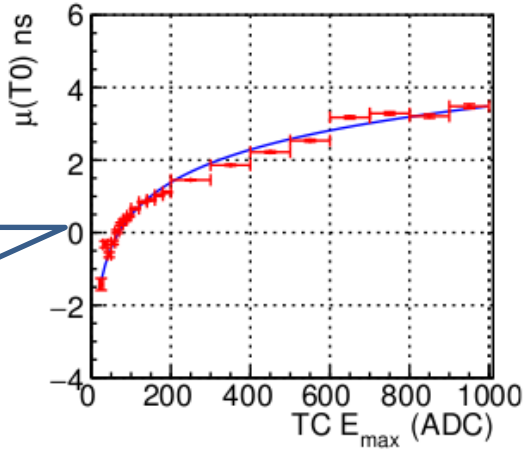


Why peak position is different from that of hadron skim ?

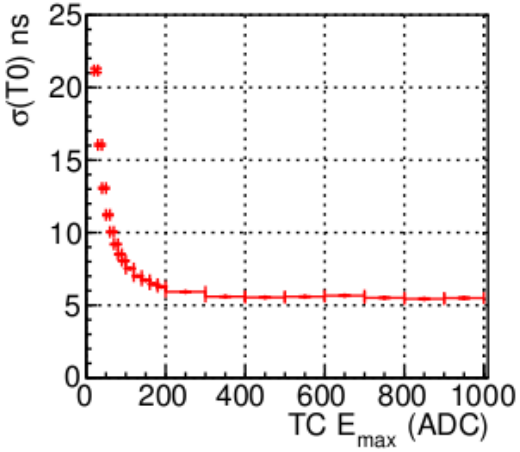
Study with offline eventT0







Probably, shown by Torben at last b2gm already



- Plan to update FAM firmware to apply timing correction by LUT.
- First, revisit simulator to find correlation between bias and noise level.