TTD status

Mikihiko Nakao (KEK)

mikihiko.nakao@kek.jp

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Outline of this talk

- **TTD:** intro
- FTSW: inventory, failures, replacement
- Cold startup
- Injection veto
- GDL timing
- git repository and software

TTD intro in one page

- TTD (Trigger Timing Distribution) the system
- FTSW (Front-end Trigger SWitch) the module
- b2tt (Belle II Trigger Timing) the protocol
- Features
 - Clock 127 MHz from SuperKEKB RF to everywhere
 - b2tt protocol to send trigger and many other things, receive busy, error and many other things
 - CAT-7 cable connections / fibers between E-hut and detector
 - JTAG connections to remote FEEs and FTSWs
- Specs
 - O(a few 10ps) jitter clock for readout/Belle2link
 - 30kHz triggers, 190ns minimum trigger separation
 - Trigger flow control mostly based on SVD APV emulator

TTD connection status



Updated plot for the Phase 3 setup (not to change until DAQ upgrade)

FTSW inventory

- FTSW version 2 21 boards are in use (SVD, TOP, ECL)
 - 7 type-P (8 port optical), 8 type-S (24-port RJ-45)
 - type-P \Leftrightarrow type-S conversion by soldering 8-port RJ-45
 - 6 type-R (receiver) with no +5V for ECL, incompatible with others
 - only 2 fresh spares, 1 used spare, + 2 for ECL special
 - no boards to loan for pocketDAQ, unless Virtex 5 chip is donated
- **FTSW** version 3 122 boards are in use
 - >5 spares, but now some are taken by Kunigo-san's setup
 - 6 type-S (receiver) with no +5V for ECL, incompatible with others
 - others can be converted between type-P, -R, -S by soldering work
 - ready-to-go type-R spare should be always preapared
- Production plan?

FTSW port degradation

- FTSW ports are not equal...
 - Well, ports are designed to be equal, except for trace differences
 - But, time-to-time, exchanging ports is a solution to a problem
 - There have been several FTSW boards with one broken port
- Some FPGA I/O-buffer may be broken or degraded?
 - If broken, it is easy to identify
 - So far we had no measure for the degraded ports
- Avoiding the degraded ports?
 - If we can quantify the degraded ports, we can avoid using them
 - Kunigo-san's b2tt checker firmware (talk tomorrow)
 - Replacing FPGA fixes the problem if the board has no other use

FTSW 032 for TOP

Problem

FTSW 032 (TOP COPPER) lost jitter cleaner setup at power-cycle

Solution?

- FTSW is replaced with a spare (FTSW 082)
- but FTSW 032 does not show this problem at B2 setup
- FTSW 032 is considered to be a spare

If it happens again?

- FTSW 082 looks fine now, but the same problem may happen again
- Jitter cleaner programming procedure is now included in a script, can be fixed by any DAQ / TOP expert

Other possible FTSW failures

- 3.3V DC-DC converter breakdown
 - sign: no LED light
 - fix: replace the SIP DC-DC module (easy soldering)
- Spartan-3AN program lost
 - sign: JTAG-port lower LED is OFF
 - fix: reprogram Spartan-3AN (need to sit in front of FTSW)
- Jitter cleaner permanent damage
 - probably it will not happen, but jitter cleaner setup can be made unchangable (with correct or incorrect config)
 - it happened when I was developing the jitter cleaner setup firmware
 - therefore, jitter cleaner reprogramming should be minimized
- Other Virtex-5 FPGA breakdown?
 - **Example:** too high current draw on +2.5V power line

Spare production?

- So far, the FTSW hardware error rate is rather low
 - In several places, ports were exchanged and behaving better
 - Only two FTSWs on detector were clearly broken: 1 KLM and 1 ARICH
 - Replacing FPGA solved the ARICH problem (KLM FTSW is yet to be repaired)
- Long term lifetime is yet unknown
 - Current failure rate is low enough for 10-year operation
- Availability
 - IO PC-boards are in hand for each of FTSW version 2 and 3
 - Most of the parts are still available online in the market
 - Virtex-5 FPGA may take a few months for delivery
 - Rare parts (DC-DC, Xtal) are in hand for \sim 40 boards

Other spares

- Item list to run TTD (besides FTSW)
 - FTOP / FTOR cards for optical transceiver
 - Optical transceivers
 - 🗕 TT-IO boards
 - VME CPU
 - VME crate
 - **Status**
 - Only one spare of FTOP / FTOR cards since they are almost / fully passive card, FTOP / FTOR to be reused when FTSW with them is replaced
 - Ready-to-use spares are available for the rest

FTSW errors

clklost

- no clklost if nobody work in E-hut near rack B-1
- **ttlost** (more in Kunigo-san's talk tomorrow)
 - FTSW port dependence, cable dependence, FEE dependence?
 - Possible reasons: attenuation, noise, spike, clock jitter?



ttlost in COPPER

- Probably different reason, yet to study
- Busy not cleared in next slide
- **b2llost due to clock? —** FTSW port characteristics?
- **other b2llost, seu, fifoerr —** these are not TTD errors...

BUSY not cleared?

BUSY collection of TTD

- To minimize latency and deadtime, busy-up and busy-down are implemented as special 8b10b signal inside b2tt
- If busy-down is missed, busy is kept even if real source is cleared
- Happens in SVD, ECL-COPPER (?)

Suspicion 1

- Timing of reset and busy: SVD needs to become busy at run start
- SVD problem turned out to be a wrong parameter setting of APV busy emulator

Suspicion 2

Merging many short busy signals may be the cause? Plan to study

SEU reset

FTSW counts recovered SEU

- shown as seu=NN in statft
- SEU count is not reset by regular resetft
- "resetft seu" to clear, but there was a bug in this command...
- Fixed in hardware and firmware

Cold start procedure

- **Recovery:** from power loss, clock loss, firmware update
- **Document:** 2019.8.5 version on git ttd repo
 - Power-up procedure
 - Programming main TTD crate modules
 - Checking JTAG connection to remote FTSWs (and FEEs)
 - Trouble-shooting
- Drill by Kunigo-san (twice)
 - Basic procedure could be done without me
 - One (undocumented) problem happened, need to be written down
- More...
 - Master firmware update is planned in September
 - The document should include up to the procedure to identify and replace broken modules

JTAG scripts

jtagft

Command-line version of subset of Xilinx impact, but it is not a userfriendly program

script

- to check the JTAG connection to remote FTSWs and FEEs
- to reprogram remote FTSWs (and jitter cleaner on them)
- this script can be updated to program remote FEEs, if we decide how to keep firmware files to be used

ttd11% ls /usr/local/bin/jtag-*

/usr/local/bin/jtag-chain-ari.sh /usr/local/bin/jtag-chain-bklm.sh /usr/local/bin/jtag-chain-cdc.sh /usr/local/bin/jtag-chain-ecl.sh /usr/local/bin/jtag-chain-eklm.sh /usr/local/bin/jtag-chain-svd.sh /usr/local/bin/jtag-chain-top.sh

/usr/local/bin/jtag-program-ari.sh /usr/local/bin/jtag-program-bklm.sh /usr/local/bin/jtag-program-cdc.sh /usr/local/bin/jtag-program-ecl.sh /usr/local/bin/jtag-program-eklm.sh /usr/local/bin/jtag-program-svd.sh /usr/local/bin/jtag-program-top.sh

JTAG failure

1 CDC and 2 ARICH FEE

• jtagft does not work, but can be programmed by Xilinx impact

not because of a particular FTSW port

Reason?

- could not be a signal level probelm since both cases are driven by LVDS (same type chip)
- timing of jtag TCK is different, jtagft is generating more equal-interval TCK signals at lower rate
- impact may be trying something undocumented in addition when it detects the problem?

How to prove?

- Need to capture the jtag bit stream of impact to the problematic FEE
- A special FTSW firmware (and lot of work) to do this

Injection veto

- **Kicker signal:** it has been implemented and tried to use
 - Kicker signal itself is correctly distributed
 - Bug: HER flag was always on, even for LER injection
 - Also in pocketTTD version of firmware, used at DESY by PXD
 - Took sometime to fix, now in git repo
 - Master FTSW firmware is yet to be reprogrammed
 - Injection veto pattern
 - Pattern is decided and generated in GDL, available via slow control
 - TTD has a mechanism to distribute to FEE
 - But PXD is not using it (!), their gated mode uses its own pattern
 - Slow control part is not yet working, but low priority to fix

GDL timing

GDL to TTD

> TTD receives one-bit decision and 4-bit type, in one clock signal

- GDL is driven by clock from TTD
- Therefore timing adjustment is needed, done at every run start
- Problem
 - Nakazawa-san reports that trigger timing is shifted by one-clock
- **Fix?**
 - Reason not known yet
 - Probably need some feedback signal from GDL, e.g., trigger timing from TTD to GDL sent back via another line
 - 5-4 pair of CAT-7 into OUT-1 can be used
 - Another modification to ft3m firmware

git repository and software

• ftsw repo

- firmware source and bit files (including TT-RX, TT-IO)
- schematics of FTSW boards
- software and documents are moved to a separate report

ttd repo

- ftprogs: command line tools, including statft
- ttaddr: program to configure connections and collect status
- pocket_ttd: main data taking process
- documents
- daq_slc
 - ttd repo to be used as submodule of, to replace "extra" files

More to be discussed in parallel session tomorrow

Summary

- TTD expert other than me (Kunigo-san) strengthen the team
- Some of the small hardware problems are fixed
- Other small hardware problems are yet to be fixed
- More hard work needed on software