Investigation CDC b2llost / b2lerror via IBERT

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Outline

- Belle2link lost / error
- CDC specific belle2link issue
- Investigation of hardware setup via IBERT
- Test results
- Test plan

Belle2link lost / error



- Belle2link lost
 - Correct K character is missing or not detected, or when CRC error is detected during data transmission.
 - Can happen on either direction of CDC FEE -> HSLB or HSLB -> CDC FEE
- Belle2link error
 - Mostly, data corruption during transmission, belle2link goes down when data write to COPPER fifo.
 - CDC FEE -> HSLB

Issue overview

- Several belle2link pairs shows frequent errors during phase2 and phase 3, which was masked during the operation.
 - cpr2017d 247 (b2llost)
 - cpr2017c 193 (b2llost)
 - cpr2014d 204 (b2llost)
 - cpr2006a 7 (b2lerror)
 - cpr2034b 97 (ttlost / crc error / b2lerror)
 - ...
- The dedicated problematic belle2link pairs are the CDC issue, specifically, the other sub detectors have no such b2l pairs.
- Since this issue occurs on specific b2l setup of CDC, the logic error is unlikely.
- The tool of IBERT (Integrated Bit Error Ratio Test) provided by Xilinx is dedicated IP core for evaluating and monitoring the MGT.
- Firstly, we propose to use IBERT to find the problem independent on the b2l logic, if lucky we may found some solutions for the issue.

IBERT firmware generation

RECBE	HSLB		
Virtex 5	Virtex 5		
XC5VLX155T	XC5VLX50T		
 For the case of CDC FEE P source pin: J16 (refer to ucf file of CDC firmware) System clock frequency: 127 MHz (from FTSW) 	 For the case of hslb P source pin: AG22 (refer to ucf file of hslb firmware) System clock frequency: 42 MHz (copper local oscillator) 		
GTP: x0y5	GTP:x0y3		
reference clock: 127 MHz	reference clock: 127 MHz		

- Comments:
 - Start up Chipscope for IBERT (virtex5 GTP need to start it from chipscope not ISE)
 - The frequency of system clock need to be 10 MHz ~ 100 MHz according to user manual. However, for the case of RECBE(CDC F/E), there is no better choice then FTSW clock 127 MHz, fortunately, it works for single direction FEE -> HSLB

IBERT test setting

🕸 IE	BERT Console - DEV:2 MyDe	vice2 (XC5VLX50T) UNIT:0 MyIB	ERT_V5_GTP0 (IBERT_V5_GTP)	
Clock Settings MGT/BERT Settings Sweep Test Settings			gs	MGTAVTTTX —
		GTP_DUAL_X0Y3_0	GTP_DUAL_X0Y3_1	
	Edit Line Rate	Edit	Edit	TXPREEMPHASIS[2:0]
П	- Coding	None	None	
9 1	X Settings			
	TXOUTCLK DCM Status	LOCKED	LOCKED	Pre-Driver Pad Driver
	Invert TX Polarity			
	Inject TX Bit Error	Inject	Inject	
	TX Diff Boost	On 💌	On 💌	
	TX Diff Output Swing	1100 mV (000) 🗸 🗸	1100 mV (000)	
	TX Pre-Emphasis	3% (000) 💌	3% (000) 💌	
Ŷ F	XX Settings			
	RXOUTCLK DCM Status	LOCKED	NOT LOCKED	Pre-Driver Pre-emphasis
	Invert RX Polarity			Pad Driver
	RX AC Coupling	v	V	TX Serial Clock
	RX Termination Voltage	GND 💌	GND	TXPREEMPHASIS[2:0]
	Enable RX EQ			UG196_c6_14_051107
	RX EQ WB/HP Ratio	50% / 50% (00) 🗸 🗸	50% / 50% (00) 💌	
	RX EQ HP Pole Loc	Ext. Resistors (0000) 🛛 🔻	Ext. Resistors (0000) 🛛 🔻	
	RX Sampling Point	640.504 UI	64 0.504 UI	
φ E	BERT Settings			
	- TX/RX Data Pattern	PRBS 7-bit	PRBS 7-bit	
	- RX Bit Error Ratio	1.666E-011	2.752E-011	
	- RX Line Rate	2.518 Gbps	0.000 Mbps	
	- RX Received Bit Count	6.004E010	3.634E010	
	RX Bit Error Count	0.000E000	0.000E000	
	BERT Reset	Reset	Reset	

- Three features to maximize the signal integrity on the TX output buffer.
 - Differential voltage control
 - Pre-emphasis
 - Configurable termination impedance

Stability test of bit error rate

É Parallels Desktop File View Virtua	Machine Devices Wind	ow Help		🥞 🔲 😻 💬• 101 🕙 🖇 🤶 🔳 100% 페 🔺 Thu 14:16	(् ≔		
			🕎 Windows 7 - Para	Ilels Desktop			
ChipScope Pro Analyzer [recbe_v56]	NELLETI_CDCWRECBE_VERS8_1	0315#RECBE_VER58#ise14#	se14.xise - (Design Summary)		• X		
Eile View JTAG Chain Device IBERT_V5GTP Win	ndow <u>H</u> elp						
😳 🕑 🔊 JTAG Scan Rate: 1s 💌 S!							
Project: recbe_v56	BERT Console - DEV:2 MyDe	evice2 (XC5VLX50T) UNIT:0 MylB	BERT_V5_GTP0 (IBERT_V5_GTP)		r م ا		
JTAG Chain — DEV:0 MvDevice0 (XC2C64A)	Clock Settings MGT/BER	Sweep Test Settin	gs				
- DEV:1 MyDevice1 (XCF16P)							
- DEV:2 MyDevice2 (XC5VLX501) - System Monitor Console					A		
P UNIT:0 MyIBERT_V5_GTP0 (IBERT_V5_GTP)			LOCKED				
IDERT CONSOLE	Invent TX Polarity	Inject	Inject				
Signals: DEV: 2 UNIT: 0	TX Diff Output Swing	1100 mV (000)	1100 mV (000)				
	TX Pre-Emphasis	3% (000)	3% (000)				
	RX Settings						
	- RXOUTCLK DCM Status	LOCKED	NOT LOCKED				
	- Invert RX Polarity						
	- RX AC Coupling	<pre> </pre>	v				
	- RX Termination Voltage	GND	GND				
	- Enable RX EQ						
	- RX EQ WB/HP Ratio	50% / 50% (00)	50% / 50% (00)				
	- RX EQ HP Pole Loc	Ext. Resistors (0000)	Ext. Resistors (0000)				
	RX Sampling Point		640.504 UI				
	BERT Settings						
	- TX/RX Data Pattern	PRBS 7-bit	PRBS 7-bit				
	- RX Bit Error Ratio	8.079E-013	3.846E-003				
141 errors in 20 i	NOURS RX Line Rate	2.520 Gbps	0.000 Mbps				
so more than 1 bit error i	n 10 _R minutescount	1.745E014	2.233E012				
	- RX Bit Error Count	1.410E002	8.590E009				
	BERT Reset	Reset	Reset				
· · · · · ·					-		
COMMAND: open_cable INFO: Started ChipScope host (localhost:50001)							
INFO: Successfully opened connection to server: localhos INFO: Trying to open Xilinx Platform USB Cable on port US	st:50001 (localhost/127.0.0.1) SB2						
INFO: Successfully opened Xilinx Platform USB Cable					1		
INFO: Cable. Platform Cable USB, Port USB21, Speed: 3 INFO: Found 1 Core Unit in the JTAG device Chain.	3 MHZ						
INFO: ******************** Start Run ******************							
🕙 🏉 🚍 👂 🚾 🍃 🤯 🧱 🐘 🗎 🖢 🕪 14:16							

Error ratio: 8.08 x 10⁻¹³ Approximately 1 error occurs pre 10 minutes

IBERT test setting

• Ø 🗵 IBERT Console - DEV:2 MyDevice2 (XC5VLX50T) UNIT:0 MyIBERT_V5_GTP0 (IBERT_V5_GTP) Sweep Test Settings Clock Settings MGT/BERT Settings Sweep Test Setup GTP_DUAL_X0Y3_0(MGT112_0) GTP_DUAL_X0Y3_1(MGT112_1) Set Parameters to Current MGT Values Clear All Parameters Sweep Test Result File Settings. Sweep Start Value Sweep End Value Sweep Value Count Sweep Parameter On TX Diff Boost On 1100 mV 1100 mV • TX Diff Output Swing 1 3% (TX Diff Boost = On) 3% (TX Diff Boost = On) • TX Pre-Emphasis -1 **RX EQ Enable** Off -Off • 1 **RX EQ WB/HP Ratio** Ŧ 1 RX EQ HP Pole Loc \mathbf{T} -1 0 (0.000 UI) 127 (1.000 UI) **RX Sampling Point** Ŧ 128 Time per Sweep Iteration (sec.): 1 Total Iterations: 128 Sweep Test Status Start Pause Stop & Reset Current Sweep Result File: C:\BELLEII\belle2link-0.19\hslb e12\MGT112_0_sweep_results.csv Ending edge of clock **Beginning edge of clock** BER 10 sampling point of 1 clock interval Error rate 1 100 120 20 40 60 80 140 0.1 0.01 0.001 0.0001 BFR 0.00001000001 000001 1E-08

UI (sampling point)

1E-09

1E-10



- The b2llost links show bad eye diagram, while the b2lerror links show normal eye diagram.
- By swapping the fiber on HSLB side, RX of fiber data transmission on the HSLB is working well.

Specify the issue



Using loopback function at different can specify the problem is related to FPGA or optical fibre

Summary & conclusion

- Several specific CDC FEE HSLB links show frequent b2llost.
- IBERT was used to investigate the b2l issues, it valid the test independent on b2l firmware.
- The link shows b2llost also detected frequent bit error during IBERT test (means it is hardware issue).
- Corresponding link with b2llost shows worse eye diagram, while link with b2lerror shows normal eye diagram.
- The test point out the issue is coming form CDC FEE board or optical fiber (hslb has been excluded by specific test), in the future the loopback function can help to identify problem from board or fiber.
- b2lerror link are more like sudden noise (means not the continuous optical signal quality, may come from clock or CDC FEE board)

Additional

- When we loaded the IBERT firmware on CDC FEE side (cpr2034b 97) which ttlost occurs frequently, IBERT shows error that clock is not correctly set.
- Corresponding IBERT firmware can detected which FEE has bad clock quality? Need more test to confirm if this coincidence is not by chance.