Investigation CDC b2llost / b2lerror via IBERT

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DAQ TROUBLE BUSTERS SESSION
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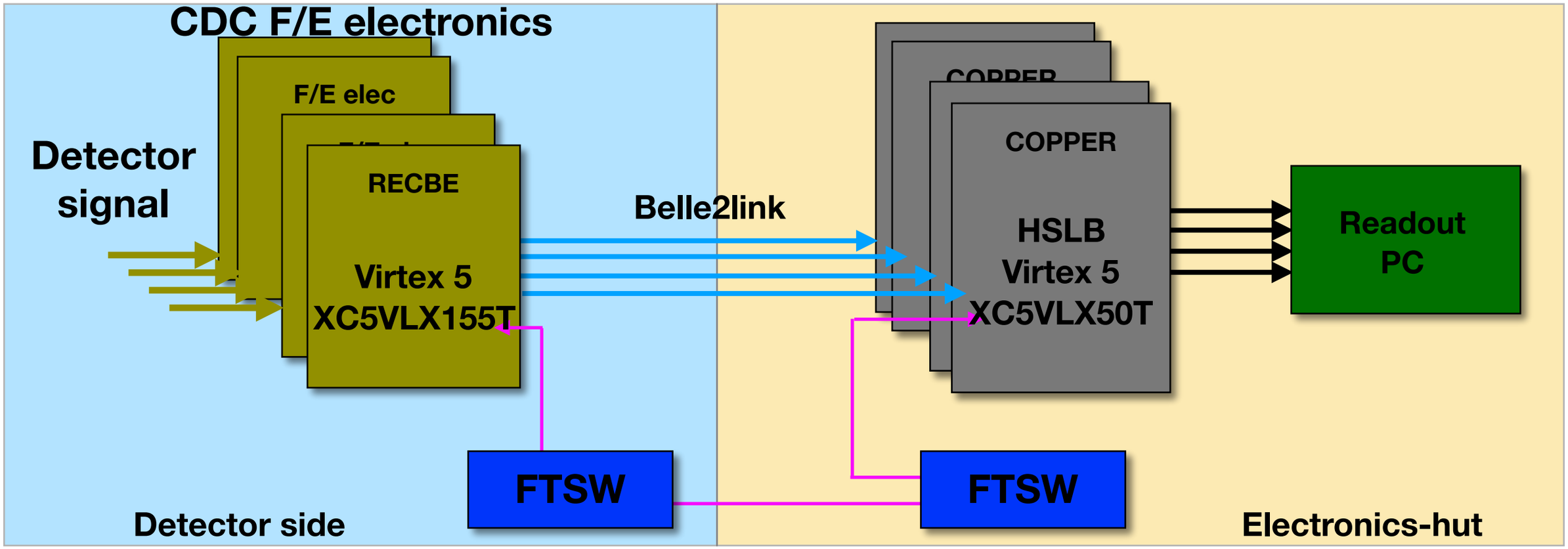
Outline

- **Belle2link lost / error**
- **CDC specific belle2link issue**
- **Investigation of hardware setup via IBERT**
- **Test results**
- **Test plan**

Belle2link lost / error



- Belle2link lost
  - Correct K character is missing or not detected, or when CRC error is detected during data transmission.
  - Can happen on either direction of CDC FEE -> HSLB or HSLB -> CDC FEE
- Belle2link error
  - Mostly, data corruption during transmission, belle2link goes down when data write to COPPER fifo.
  - CDC FEE -> HSLB

Issue overview

- **Several belle2link pairs shows frequent errors during phase2 and phase 3, which was masked during the operation.**
  - **cpr2017d - 247 (b2llost)**
  - **cpr2017c - 193 (b2llost)**
  - **cpr2014d - 204 (b2llost)**
  - **cpr2006a - 7 (b2lerror)**
  - **cpr2034b - 97 (ttlost / crc error / b2lerror)**
  - **…**
- **The dedicated problematic belle2link pairs are the CDC issue, specifically, the other sub detectors have no such b2l pairs.**

- **Since this issue occurs on specific b2l setup of CDC, the logic error is unlikely.**
- **The tool of IBERT (Integrated Bit Error Ratio Test) provided by Xilinx is dedicated IP core for evaluating and monitoring the MGT.**
- **Firstly, we propose to use IBERT to find the problem independent on the b2l logic, if lucky we may found some solutions for the issue.**

IBERT firmware generation

RECBE

Virtex 5
XC5VLX155T

- **For the case of CDC FEE**
  - **P source pin: J16 (refer to ucf file of CDC firmware)**
  - **System clock frequency: 127 MHz (from FTSW)**

GTP: x0y5
reference clock: 127 MHz

HSLB

Virtex 5
XC5VLX50T

- **For the case of hslb**
  - **P source pin: AG22 (refer to ucf file of hslb firmware)**
  - **System clock frequency: 42 MHz (copper local oscillator)**

GTP:x0y3
reference clock: 127 MHz

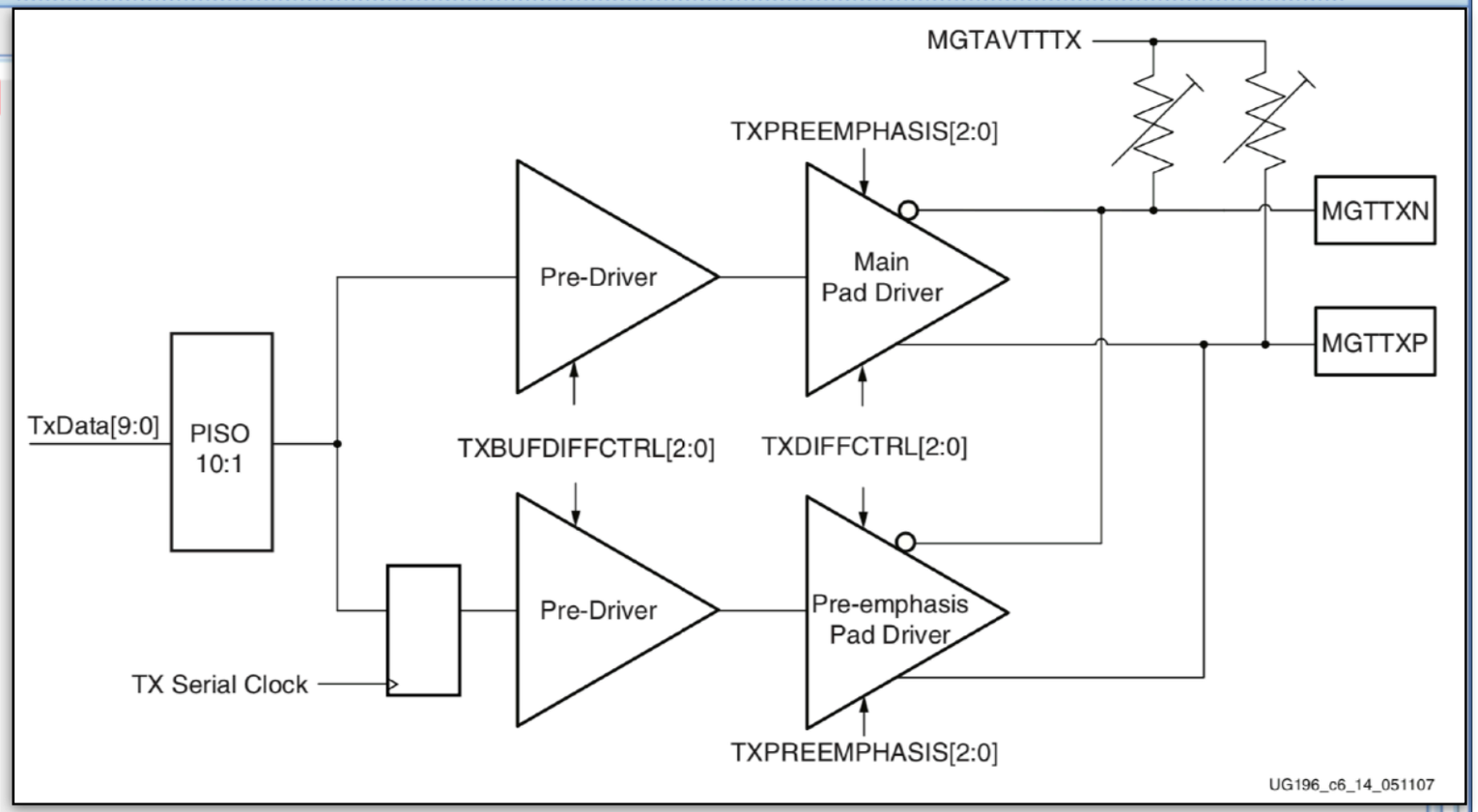
- **Comments:**
  - **Start up Chipscope for IBERT (virtex5 GTP need to start it from chipscope not ISE)**
  - **The frequency of system clock need to be 10 MHz ~ 100 MHz according to user manual. However, for the case of RECBE(CDC F/E), there is no better choice then FTSW clock 127 MHz, fortunately, it works for single direction FEE -> HSLB**

IBERT test setting

IBERT Console - DEV:2 MyDevice2 (XC5VLX50T) UNIT:0 MyIBERT_V5_GTP0 (IBERT_V5_GTP)

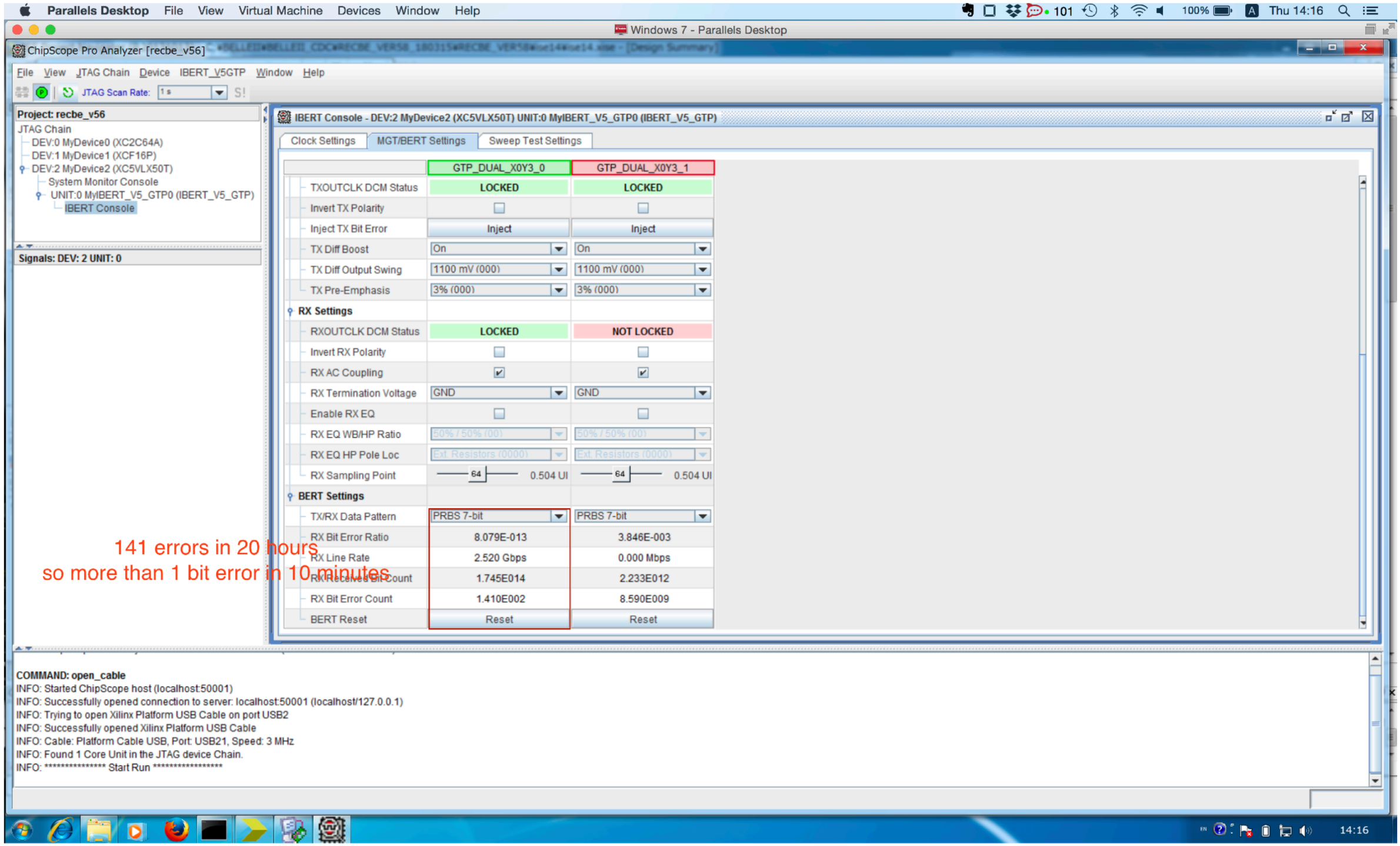
Clock Settings | MGT/BERT Settings | Sweep Test Settings

	GTP_DUAL_X0Y3_0	GTP_DUAL_X0Y3_1
Edit Line Rate	Edit...	Edit...
Coding	None	None
TX Settings		
TXOUTCLK DCM Status	LOCKED	LOCKED
Invert TX Polarity	☐	☐
Inject TX Bit Error	Inject	Inject
TX Diff Boost	On	On
TX Diff Output Swing	1100 mV (000)	1100 mV (000)
TX Pre-Emphasis	3% (000)	3% (000)
RX Settings		
RXOUTCLK DCM Status	LOCKED	NOT LOCKED
Invert RX Polarity	☐	☐
RX AC Coupling	☑	☑
RX Termination Voltage	GND	GND
Enable RX EQ	☐	☐
RX EQ WB/HP Ratio	50% / 50% (00)	50% / 50% (00)
RX EQ HP Pole Loc	Ext. Resistors (0000)	Ext. Resistors (0000)
RX Sampling Point	64 0.504 UI	64 0.504 UI
BERT Settings		
TX/RX Data Pattern	PRBS 7-bit	PRBS 7-bit
RX Bit Error Ratio	1.666E-011	2.752E-011
RX Line Rate	2.518 Gbps	0.000 Mbps
RX Received Bit Count	6.004E010	3.634E010
RX Bit Error Count	0.000E000	0.000E000
BERT Reset	Reset	Reset



- **Three features to maximize the signal integrity on the TX output buffer.**
  - **Differential voltage control**
  - **Pre-emphasis**
  - **Configurable termination impedance**

Stability test of bit error rate



Error ratio: 8.08 x 10^{-13}

Approximately 1 error occurs pre 10 minutes

IBERT test setting

IBERT Console - DEV:2 MyDevice2 (XC5VLX50T) UNIT:0 MyIBERT_V5_GTP0 (IBERT_V5_GTP)

Clock Settings | MGT/BERT Settings | Sweep Test Settings

Sweep Test Setup

GTP_DUAL_X0Y3_0(MGT112_0) | GTP_DUAL_X0Y3_1(MGT112_1)

Set Parameters to Current MGT Values | Clear All Parameters | Sweep Test Result File Settings...

Sweep Parameter	Sweep Start Value	Sweep End Value	Sweep Value Count
TX Diff Boost	On	On	1
TX Diff Output Swing	1100 mV	1100 mV	1
TX Pre-Emphasis	3% (TX Diff Boost = On)	3% (TX Diff Boost = On)	1
RX EQ Enable	Off	Off	1
RX EQ WB/HP Ratio	50% / 50%	50% / 50%	1
RX EQ HP Pole Loc	0%	0%	1
RX Sampling Point	0 (0.000 UI)	127 (1.000 UI)	128

Total Iterations: 128 — Time per Sweep Iteration (sec.): 1

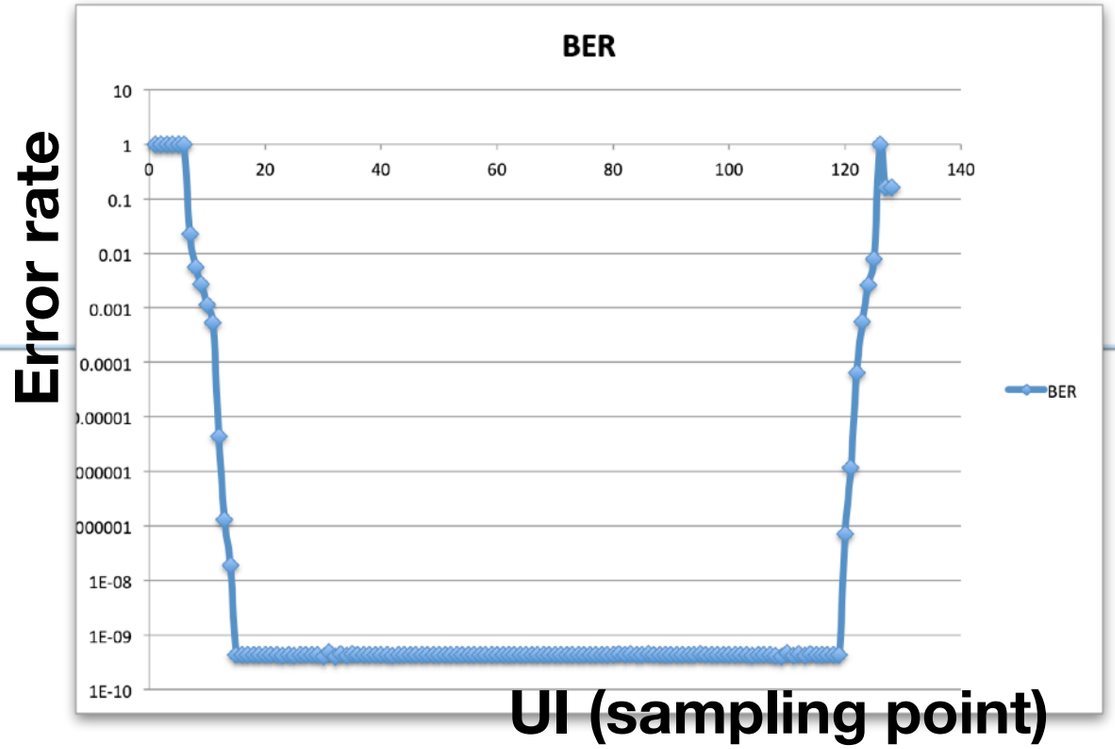
Sweep Test Status

Start | Pause | Stop & Reset — Current Sweep Result File: C:\BELLEII\belle2link-0.19\hslb_bse12\MGT112_0_sweep_results.csv

Beginning edge of clock

Ending edge of clock

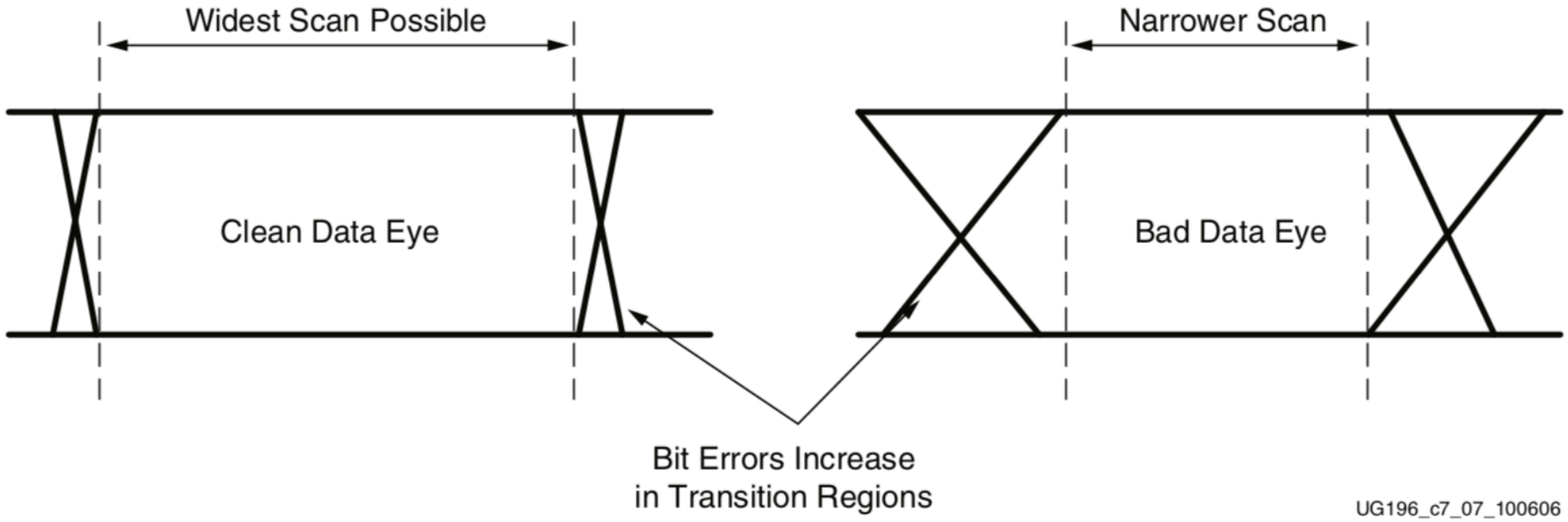
sampling point of 1 clock interval



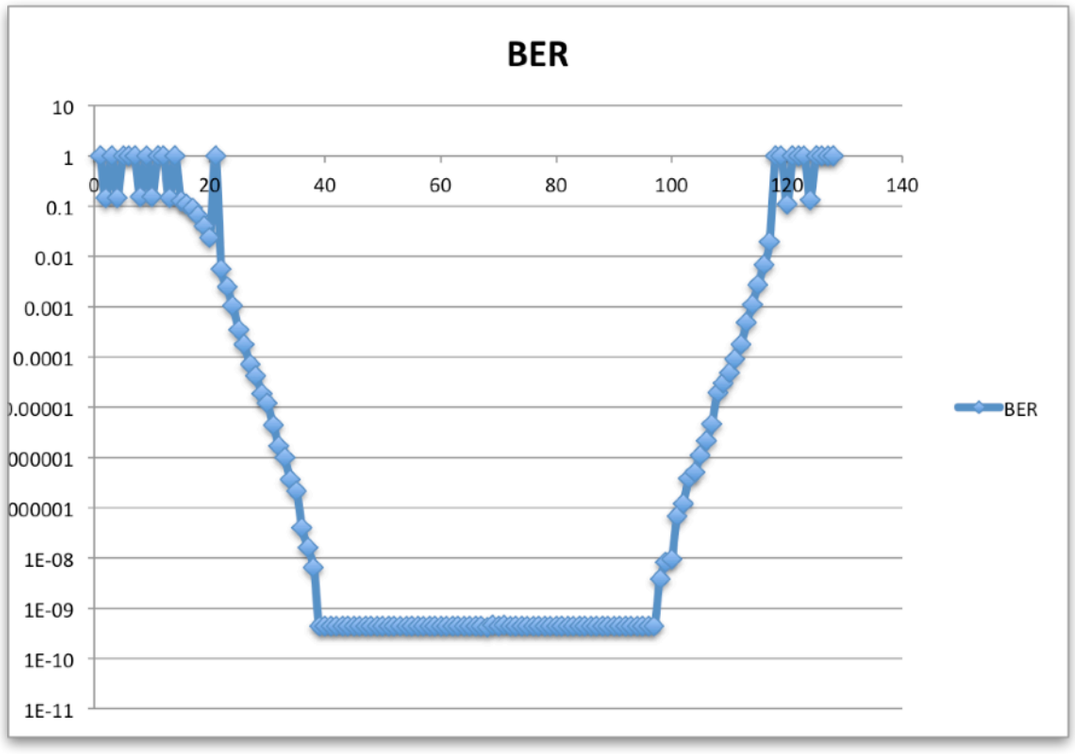
Error rate

UI (sampling point)

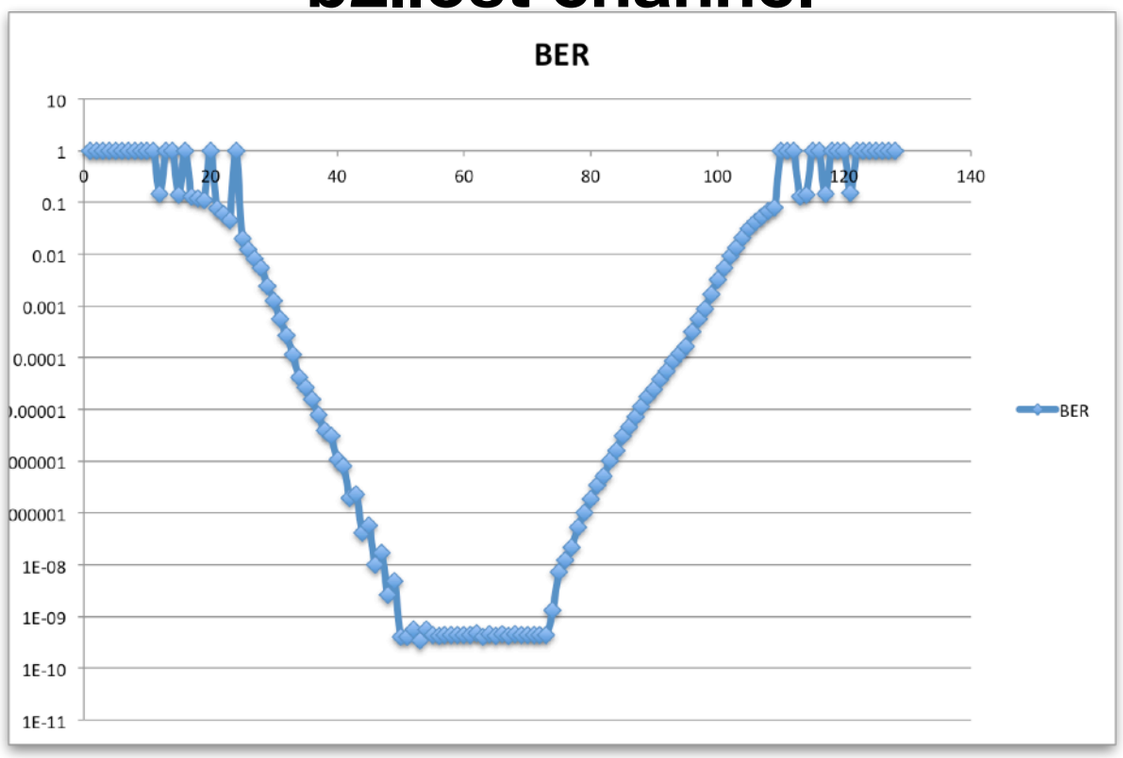
Swing test result



Reference channel

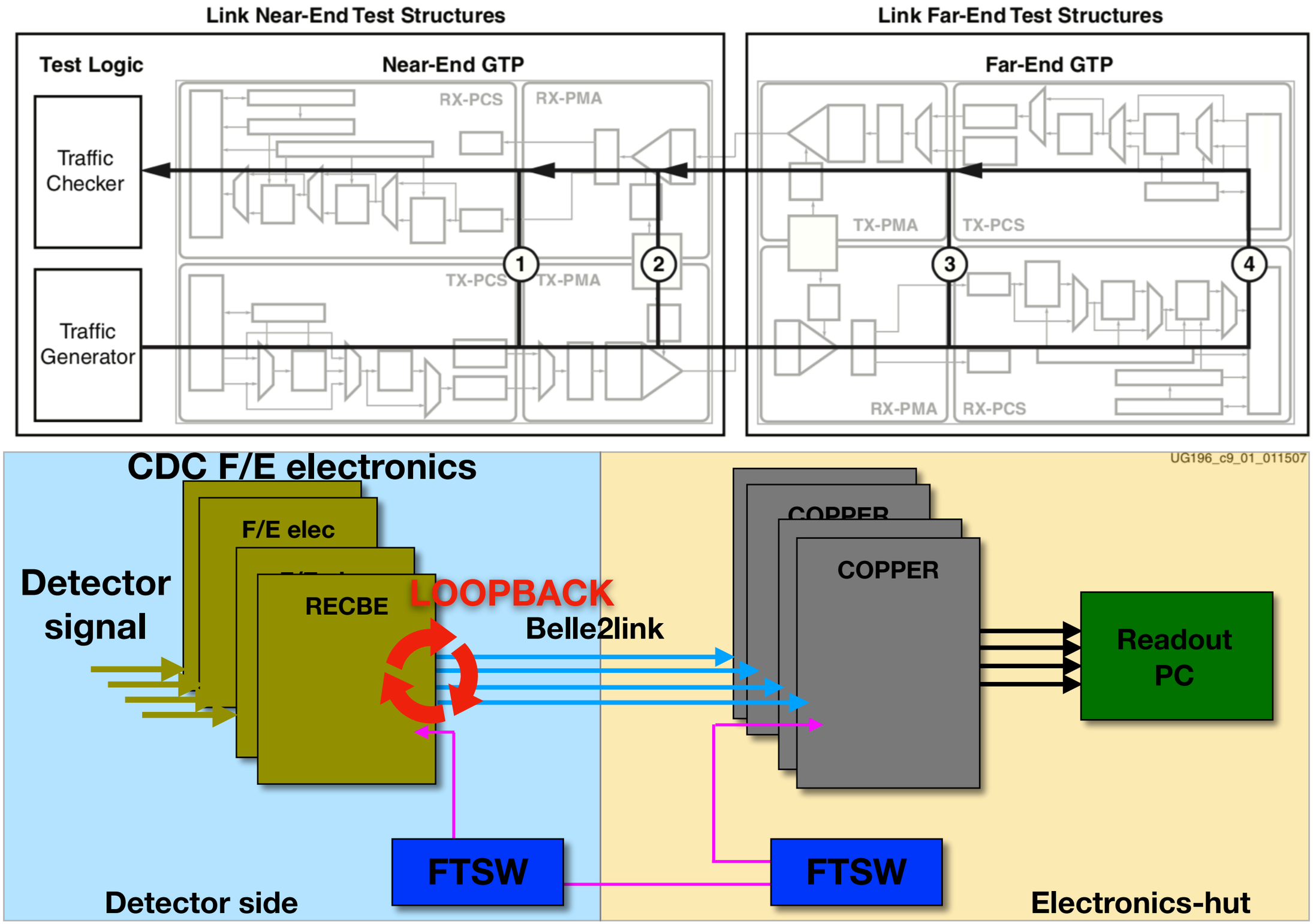


b2llost channel



- **The b2llost links show bad eye diagram, while the b2lerror links show normal eye diagram.**
- **By swapping the fiber on HSLB side, RX of fiber data transmission on the HSLB is working well.**

Specify the issue



Using loopback function at different can specify the problem is related to FPGA or optical fibre

Summary & conclusion

- **Several specific CDC FEE - HSLB links show frequent b2llost.**
- **IBERT was used to investigate the b2l issues, it valid the test independent on b2l firmware.**
- **The link shows b2llost also detected frequent bit error during IBERT test (means it is hardware issue).**
- **Corresponding link with b2llost shows worse eye diagram, while link with b2lerror shows normal eye diagram.**
- **The test point out the issue is coming form CDC FEE board or optical fiber (hslb has been excluded by specific test), in the future the loopback function can help to identify problem from board or fiber.**
- **b2lerror link are more like sudden noise (means not the continuous optical signal quality, may come from clock or CDC FEE board)**

Additional

- **When we loaded the IBERT firmware on CDC FEE side (cpr2034b - 97) which ttlost occurs frequently, IBERT shows error that clock is not correctly set.**
- **Corresponding IBERT firmware can detected which FEE has bad clock quality? Need more test to confirm if this coincidence is not by chance.**