Status of IHEP Project for Belle II DAQ Upgrade

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2019 Belle II Trigger and DAQ workshop
Aug. 28 2019
Outline

• IHEP Solution for Belle II DAQ upgrade
• CPPF introduce and upgrade
• Demo system at IHEP
• Progress/Status
• Summary
• Upgrading is straight forward:
  • Replacing HSLB/COPPER with CMS/CPPF designed by IHEP
  • Network link: GbE/10GbE

IHEP Solution for Belle II DAQ upgrade
More on IHEP Solution for Belle II DAQ upgrade

- Replacing HSLB/COPPER board with CPPF/CMS board/uTCA crate
- Merging/Concentration is based on 4 ports
- One CPPF board replaces 4-6 COPPERs (with HSLBs), 24 input links (depends on system bandwidth)
- One CPPF outputs one or more 1/10GbE to Event builder
- One CPPF with 1/2 TTD interface
- One CPPF with one Slow Control network
- No change to other DAQ parts
CPPF Introduction

- Data throughput
  - 3 MiniPoD, support 360Gb/s INPUT,
  - 2 MiniPoD, support 240Gb/s OUTPUT
- XC7VX415T-2 (Virtex-7)
  - Core FPGA for data processing,
  - Pin compatible with XC7VX690T,
  - 48 channel GTH Transceivers,
  - Support up to 13.1Gbps per channel.
- DDR3 2Gb (pin compatible with 4Gb)
- XC7K70T-2 (Kintex-7)
  - Control FPGA,
  - Configure and Control CPPF.
- Flash 1GB
  - Configuration file store
- AT32UC3A1512 (Atmel)
  - MMC, Module Management Controller.
CPPF upgrade for BelleII

- XC7VX415T upgrade to XC7V690T
- Added one TX MiniPoD (12 TX channel),
- Total: 36 channel input, 36 channel output,
- Added 156.25MHz OSC for 10GbE,
- Support up to 4x10GbE (If bandwidth needed)
- Added TWO FTSW RJ45 Ports,
- CPPF_V3_4 is ready and under testing.
Old version for CMS

New version for Belle II
Demo system Setup at IHEP

- Photo of Full Demo System

FTSW

use HSLB as data source

CPPF/Readout

Host PC

Connect to PC Ethernet card

CPPF and PC in working

Optical fiber to Ethernet card on PC

Optical fiber to data source

JTAG cable

RJ45 connector and CAT 7 to FTSW

2019-8-27
Demo system Based on 10GbE

• HSLB Clock/Trigger Gen
  • --Generate 125MHz clock
  • --Generate trigger signal
  • Trigger rate is controlled by PC;
  • Trigger signal can be masked by feedback BUSY signal;
  • --send clock and trigger to fan-out board

• Fan-out board
  • Fan out 125MHz clock and trigger signal to Data source boards,

• Data source board
  • --use hslb as data source (belle2link-0.19)
  • --generate dummy data and provide some register for slow control test

• Readout board
  • use CPPF as readout board
  • implement belle2link(data merge and slow control) and some COPPER and ROPC function on it
  • output data to PC and receive command from PC via Ethernet.

• host pc
  --receive data from CPPF through 10G Ethernet
  --send slow control command to CPPF via SiTCP

• Use an short-time(10min) evaluation version 10GbE IP core(from a company), implemented on CPPF
Firmware structure  Data merger based on 10GbE
COPPER Data format based on 10 GbE (4 links)

- 10GbE IP core data width 64 bits;
- Old COPPER data format header:
  - 13*32bits

Modification on COPPER Data format:
- Inserting a 32bit word called Reserve after channel D data length,
- make the header into 14*32bit,
- Inserting a 32bit word called Reserve in trail,
- Make the trail into 4*32bit
First 4 events shows below follows COPPER format, event number is incremented.
COPPER-like Data format based on 10 GbE(16 links)

- For 16 links
  - Similar to 4 link COPPER data format
  - Header add 12 more 32bit word to represent the data length of added links and total data length is the sum of 16 links’ data length
  - 4 links -> 16 links data in one event
  - Data format for 16 or 24 links should be further discussed with Yamada-san.
COPPER-like Data format based on 10 GbE (16 links)

- PC received data (1st event) is shown as right,
- COPPER event number and link event number are checked.
- Header of COPPER and link header and footer are checked.
- Event number are checked whether they are increased one by one.
- About 100 thousands events are received and checked, and data are correct.
Firmware structure - *Slow control*
Firmware structure: Slow Control
Interface between localbus and SiTCP

<table>
<thead>
<tr>
<th>Signal name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RBCT_ACT</td>
<td>O</td>
<td>Indicates the bus operating.</td>
</tr>
<tr>
<td>RBCT_ADDR[31:0]</td>
<td>O</td>
<td>Address in access</td>
</tr>
<tr>
<td>RBCT_WE</td>
<td>O</td>
<td>Write enable</td>
</tr>
<tr>
<td>RBCT_WD[7:0]</td>
<td>O</td>
<td>Write data</td>
</tr>
<tr>
<td>RBCT_RE</td>
<td>O</td>
<td>Read enable</td>
</tr>
<tr>
<td>RBCT_RD[7:0]</td>
<td>I</td>
<td>Read data</td>
</tr>
<tr>
<td>RBCT_ACK</td>
<td>I</td>
<td>Access response</td>
</tr>
</tbody>
</table>

**RBCP signal description**

**UDP RBCP packet format**

<table>
<thead>
<tr>
<th>CMD bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Access</td>
<td>Bus Access</td>
</tr>
<tr>
<td>2</td>
<td>R/W</td>
<td>0: Write, 1: Read</td>
</tr>
<tr>
<td>1</td>
<td>Reserve</td>
<td>Always 0</td>
</tr>
<tr>
<td>0</td>
<td>Reserve</td>
<td>Always 0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>FLAG bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>REQ/ACK</td>
<td>0: Request, 1: Acknowledge</td>
</tr>
<tr>
<td>2</td>
<td>Reserve</td>
<td>Always 0</td>
</tr>
<tr>
<td>1</td>
<td>Reserve</td>
<td>Always 0</td>
</tr>
<tr>
<td>0</td>
<td>Error</td>
<td>0: Normal, 1: Bus Error</td>
</tr>
</tbody>
</table>

**Interface between localbus and SiTCP (with RBCP)**
Slow control test result

Slow control

Main functions are realized and verified
--8 bit register read and write—A7D8
--32 bit register read and write—A16D32
--Stream write—Stream

A7D8: Delay parameter was written and read back correctly

A16D32 example

Test slow control, A7D8 and A16D32, up to 10000 times w/r, without error
Resource utilization in CPPF

- 16 links version resource utilization in CPPF.
- BRAM is used 57% in old version of CPPF.
- And BRAM 34% used in new version of CPPF.
- New version of CPPF based on xc7vx690t can provide enough BRAM for Data buffering.
Status of the IHEP Demo system

• Based on 10GbE(4 channels)
  • Functions are based 4 inputs implementation of COPPER
  • Data output to Event builder/readout PC via Optical Switch
  • Four Slow control links in one CPPF
  • TTD interface, BUSY handshake with FTSW
  • Data check function
    • checking event number
    • CRC and others not yet

• Based on 10GbE(16 channels)
  • Functions are based 4 inputs implementation of COPPER
  • Data output to Event builder/readout PC via Optical Switch
  • 16 Slow control links in one CPPF
  • TTD interface, BUSY handshake with FTSW
  • Data check function
    • checking event number
    • CRC and others not yet

Done
Done
Done (simple CDC parameters)
Done based on SiTCP, For 10 GbE Waiting for new version of CPPF

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Done
Done (simple CDC parameters)
Done based on SiTCP, For 10 GbE Waiting for new version of CPPF

Done
Manpower and tasks

• Zhen-An LIU: Overall.
• Jingzhou ZHAO/Jia TAO: Main person for the implementation.
• Wenxuan GONG/Na WANG: Hardware modification and production.
• Hanjun KOU: readout via 1G/10G Ethernet implementation with SITCP, B2TT implementation.
• Pengcheng CAO: Slow Control and control firmware.
• Jianing SONG: Hardware testing.
• Two students from Fudan Uni. are also possible
Summary

• CPPF is the main board in IHEP Demo system for DAQ upgrade.
• New version of CPPF for Belle II is ready and under testing.
• Demo system at IHEP achieved success for 16 channels.
  • Based on 10GbE
• IHEP proposal could meet all requirement
  • Open, scalable, upgradable, re-configurable hardware platform
  • Suitable for future FEE and DAQ networking upgrade also
• Join test in KEK could start to plan.