

Status of IHEP Project for Belle II DAQ Upgrade

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representing the IHEP/Fudan Team

2019 Belle II Trigger and DAQ workshop

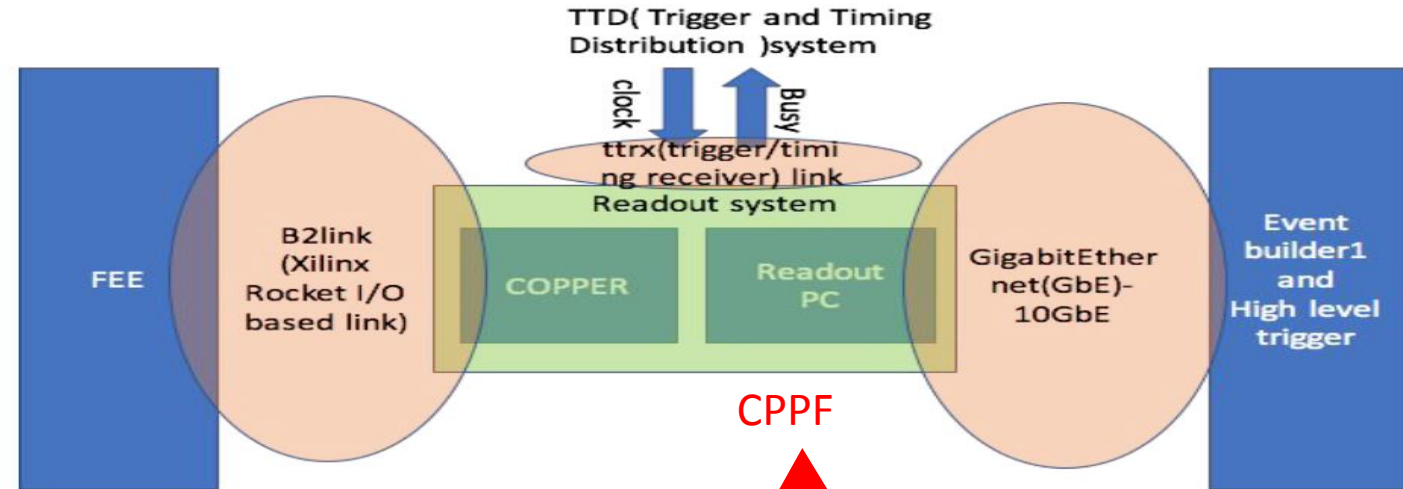
Aug. 28 2019

Outline

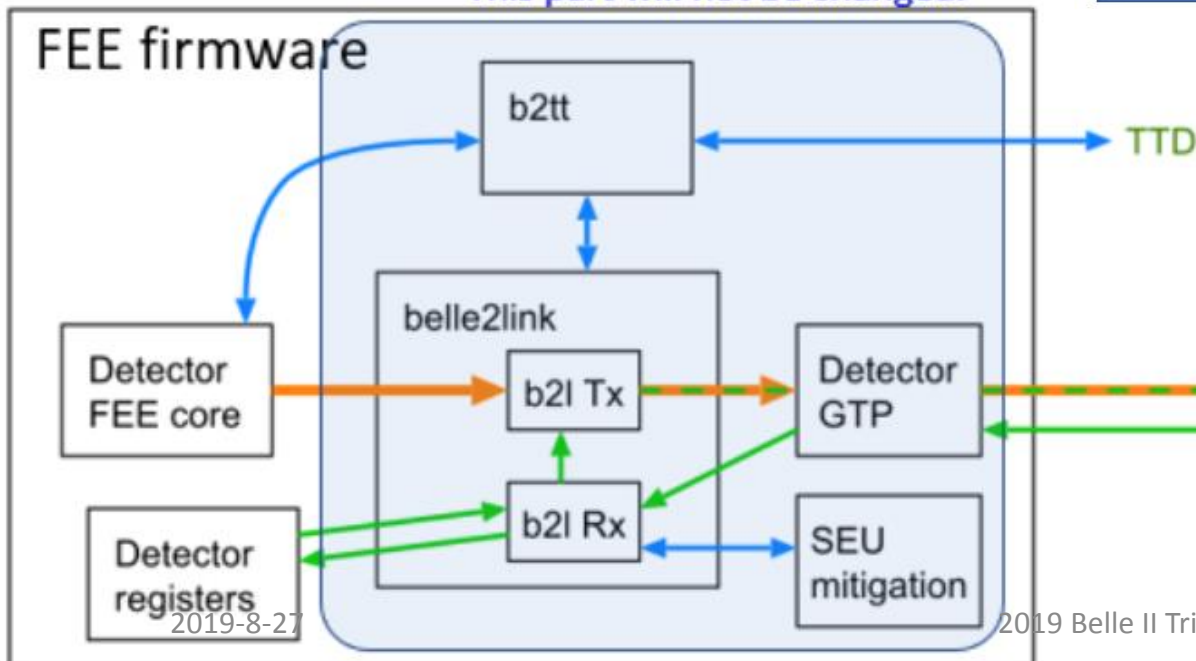
- IHEP Solution for Belle II DAQ upgrade
- CPPF introduce and upgrade
- Demo system at IHEP
- Progress/Status
- Summary

IHEP Solution for Belle II DAQ upgrade

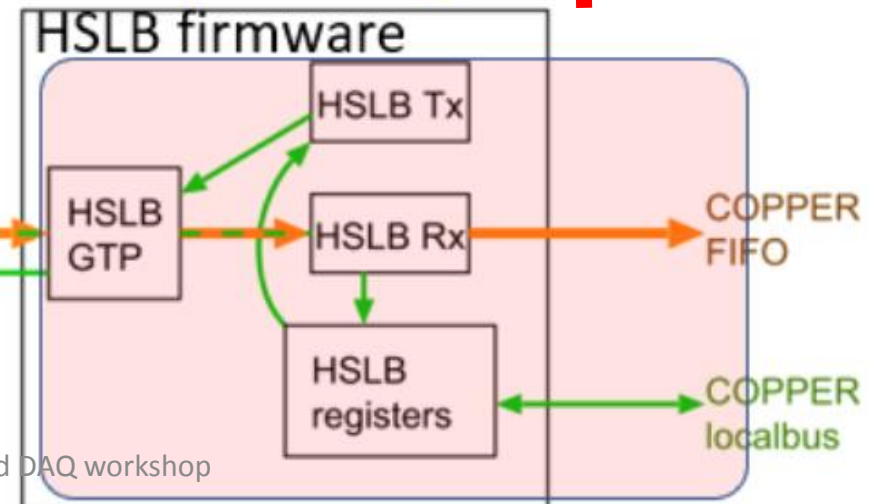
- Upgrading is straight forward:
 - Replacing HSLB/COPPER with **CMS/CPPF** designed by IHEP
 - Network link: GbE/10GbE



This part will not be changed.

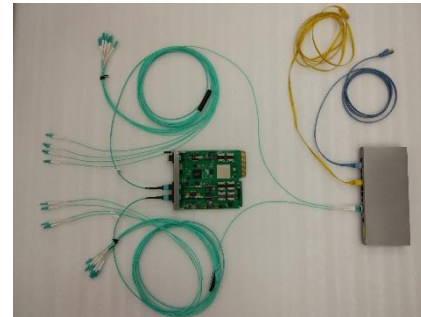
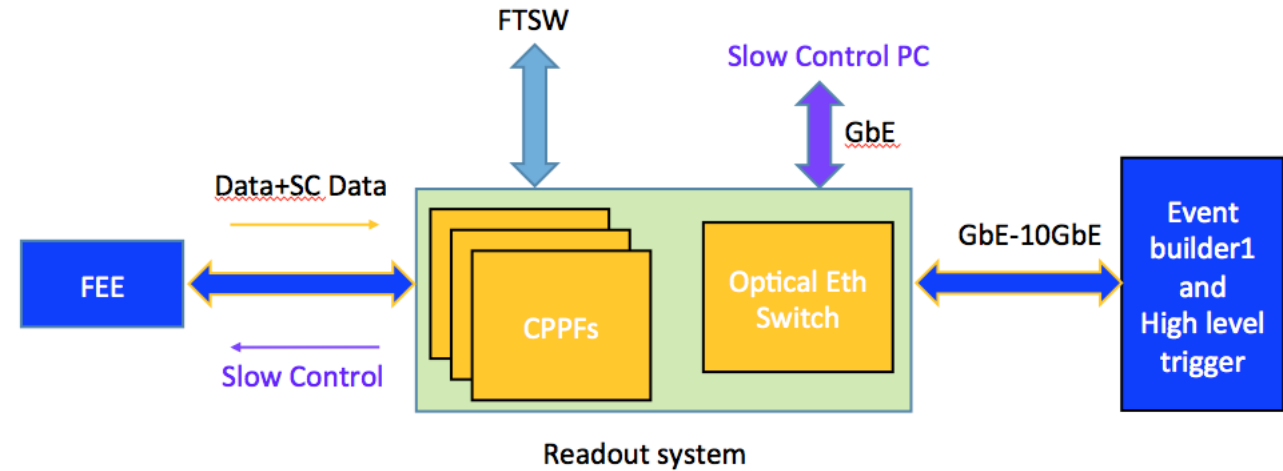


This part will be upgraded.



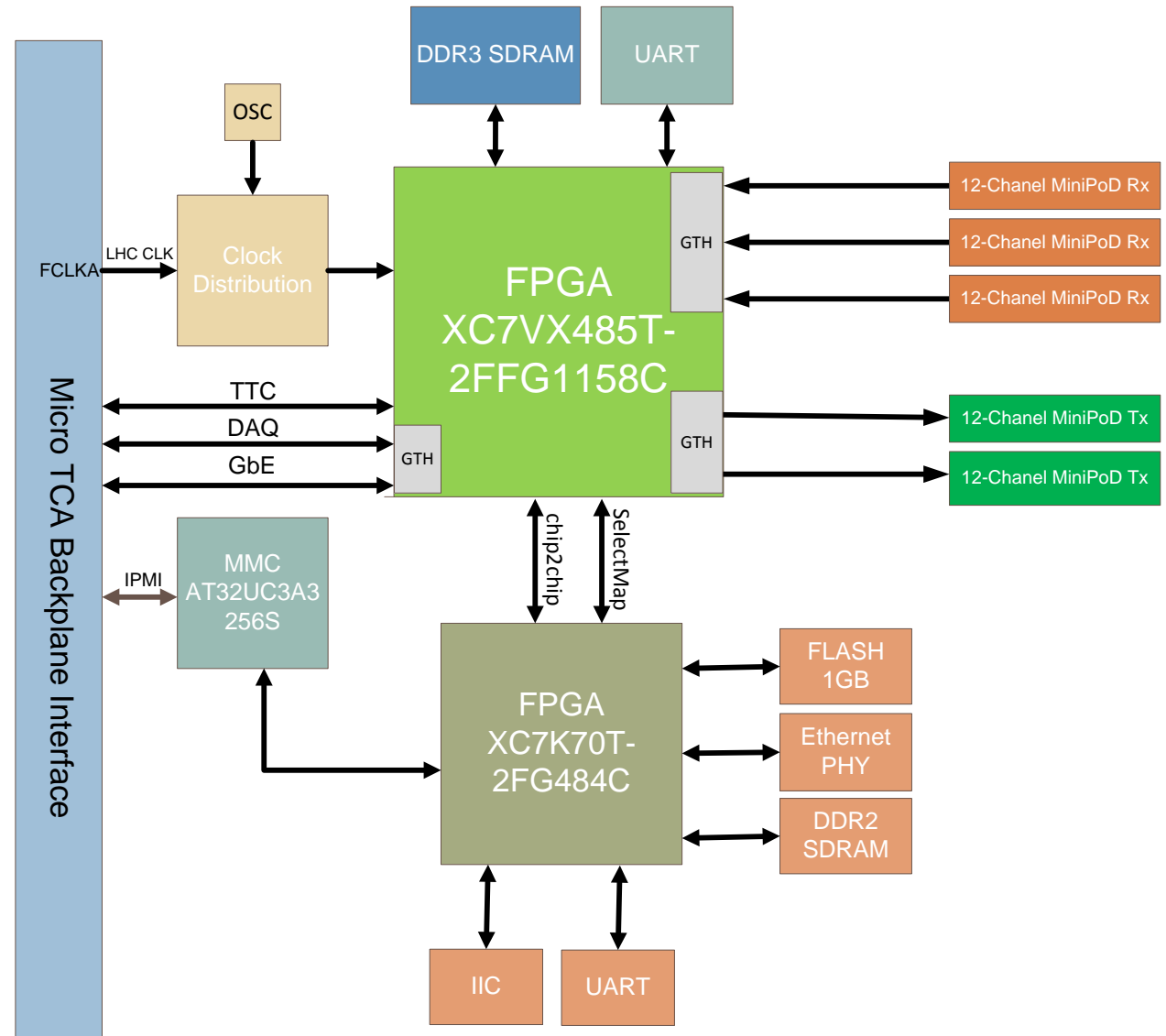
More on IHEP Solution for Belle II DAQ upgrade

- Replacing HSLB/COPPER board with CPPF/CMS board/uTCA crate
- Merging/Concentration is based on 4 ports
- **One CPPF board replaces 4-6 COPPERs(with HSLBs), 24 input links** (depends on system bandwidth)
- One CPPF outputs one or more 1/10GbE to Event builder
- One CPPF with 1/2 TTD interface
- One CPPF with one Slow Control network
- No change to other DAQ parts



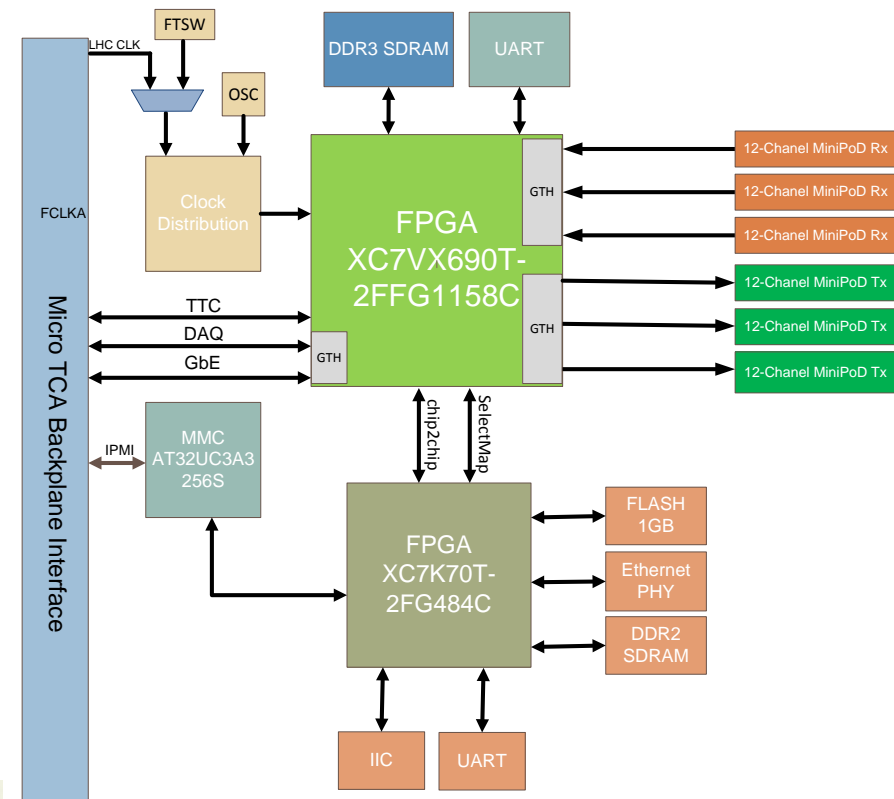
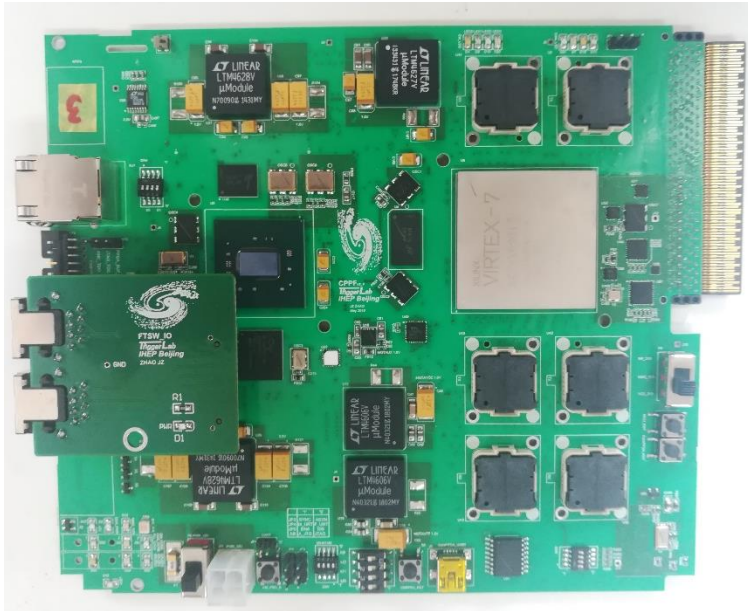
CPPF Introduction

- Data throughput
 - 3 MiniPoD, support 360Gb/s INPUT,
 - 2 MiniPoD, support 240Gb/s OUTPUT
- XC7VX415T-2 (Virtex-7)
 - Core FPGA for data processing,
 - Pin compatible with XC7VX690T,
 - 48 channel GTH Transceivers,
 - Support up to 13.1Gbps per channel.
- DDR3 2Gb(pin compatible with 4Gb)
- XC7K70T-2 (Kintex-7)
 - Control FPGA,
 - Configure and Control CPPF.
- Flash 1GB
 - Configuration file store
- AT32UC3A1512 (Atmel)
 - MMC, Module Management Controller.

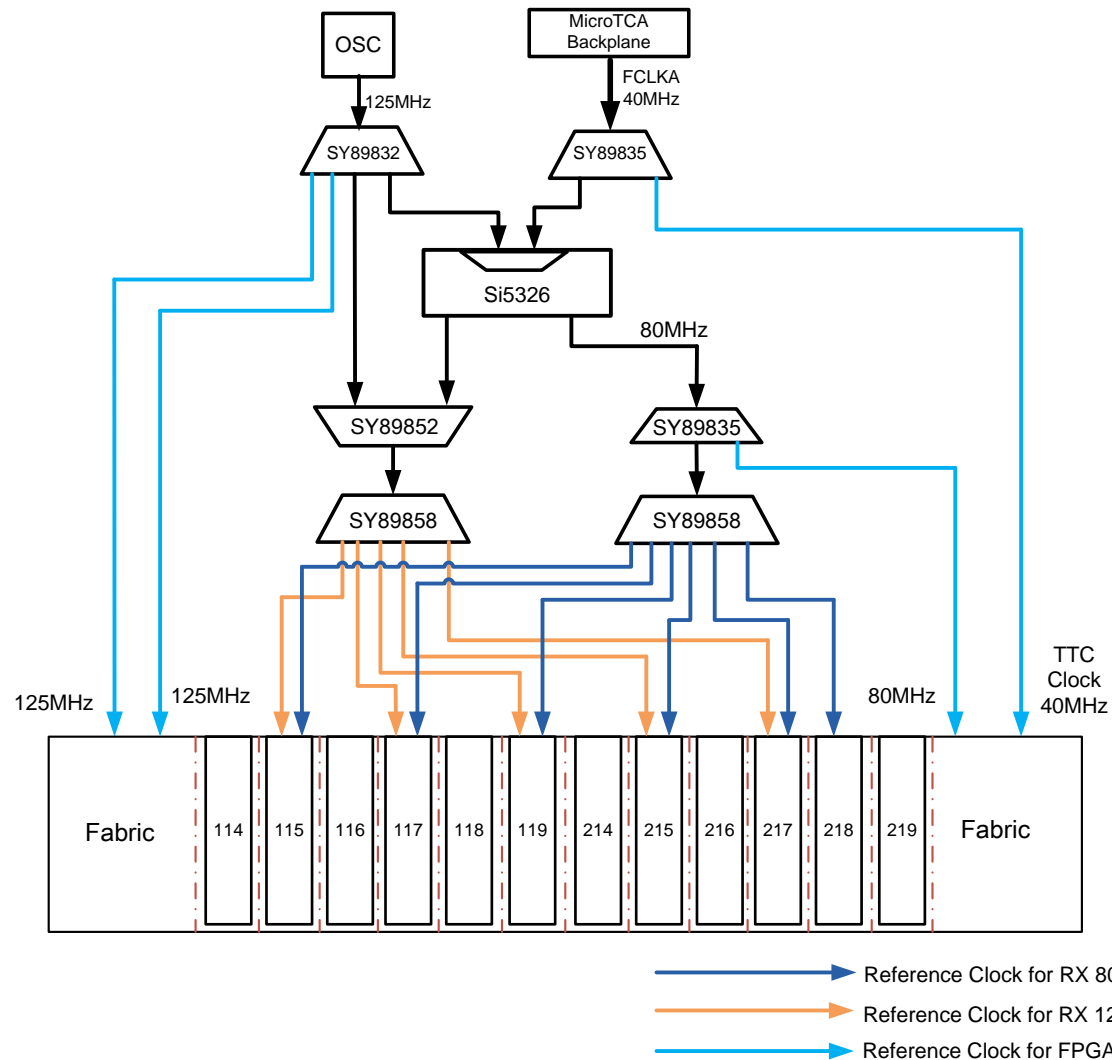


CPPF upgrade for BelleII

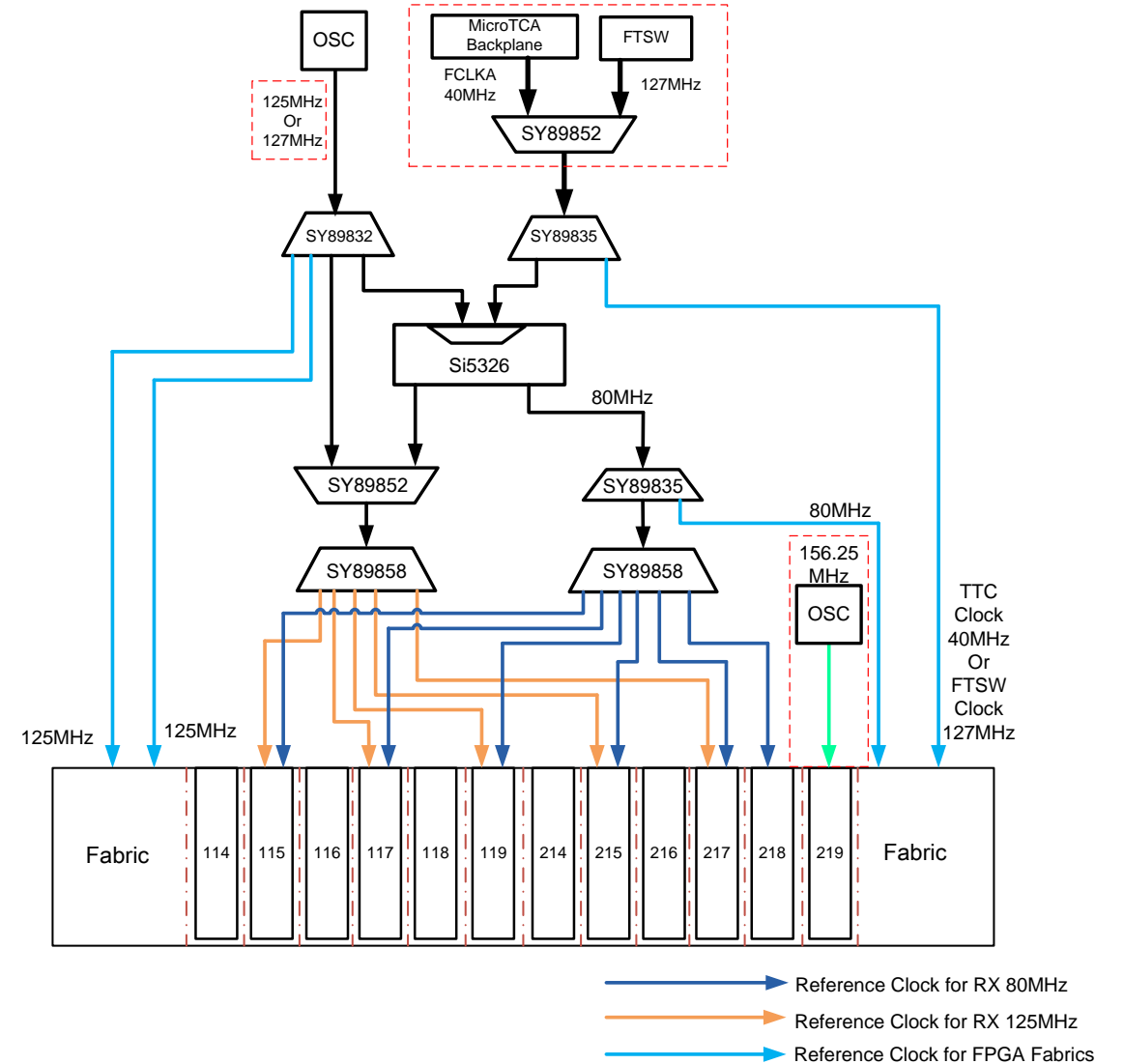
- XC7VX415T upgrade to XC7V690T
- Added one TX MiniPoD(12 TX channel),
- Total: 36 channel input, 36 channel output,
- Added 156.25MHz OSC for 10GbE,
- Support up to 4x10GbE(If bandwidth needed)
- Added TWO FTSW RJ45 Ports,
- CPPF_V3_4 is ready and under testing.



CPPF Clock Distribution



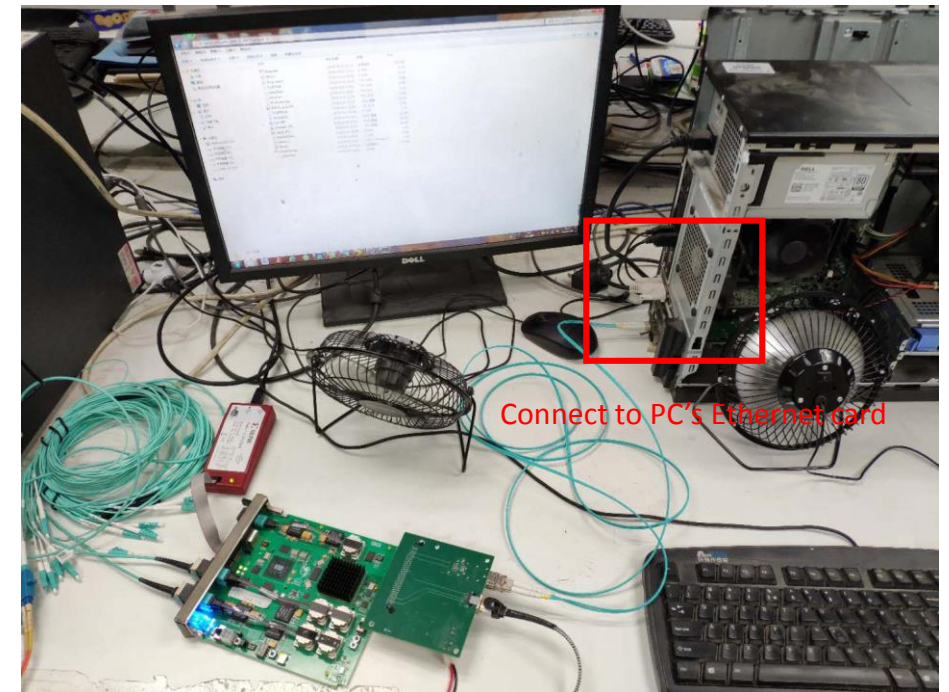
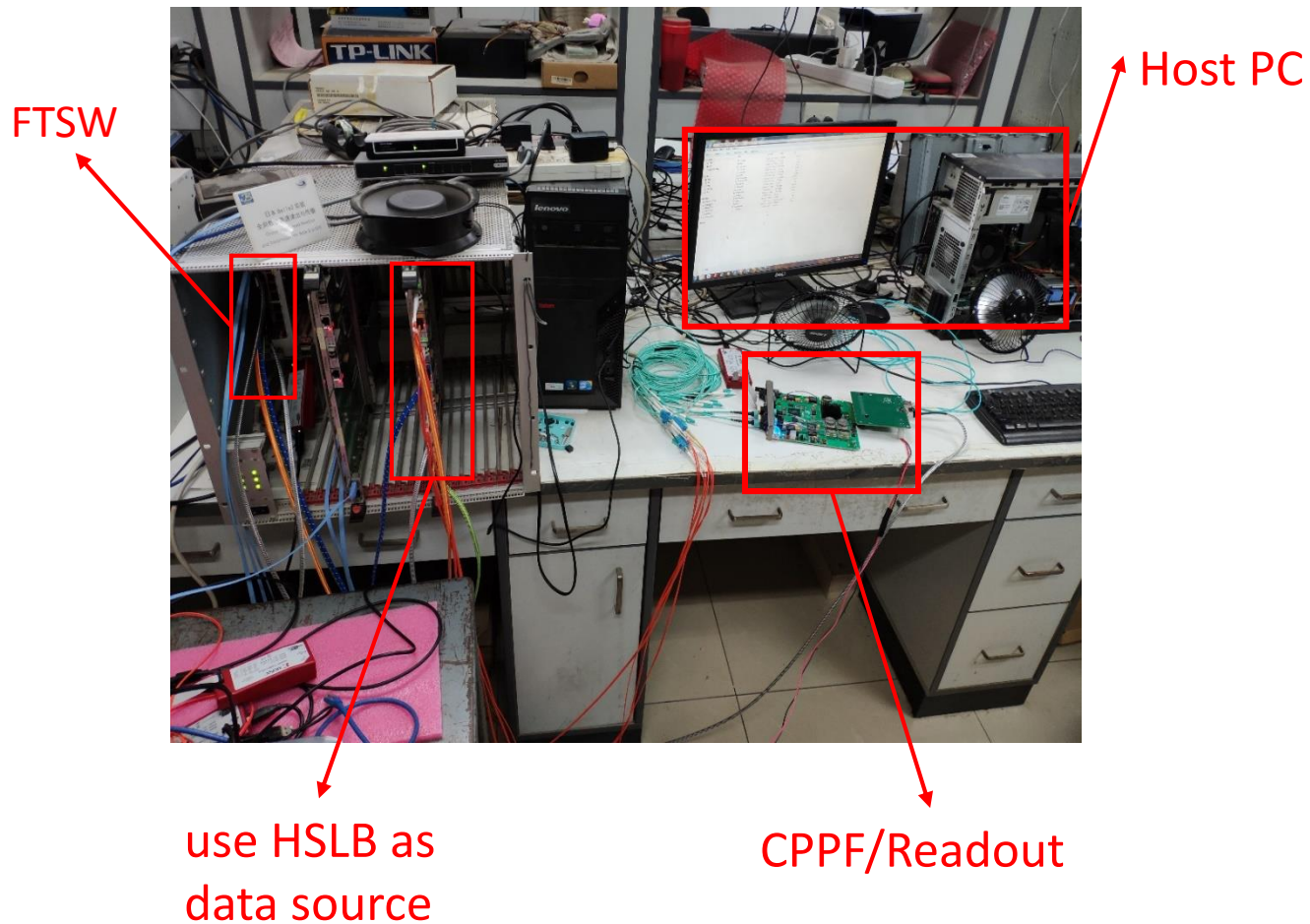
Old version for CMS



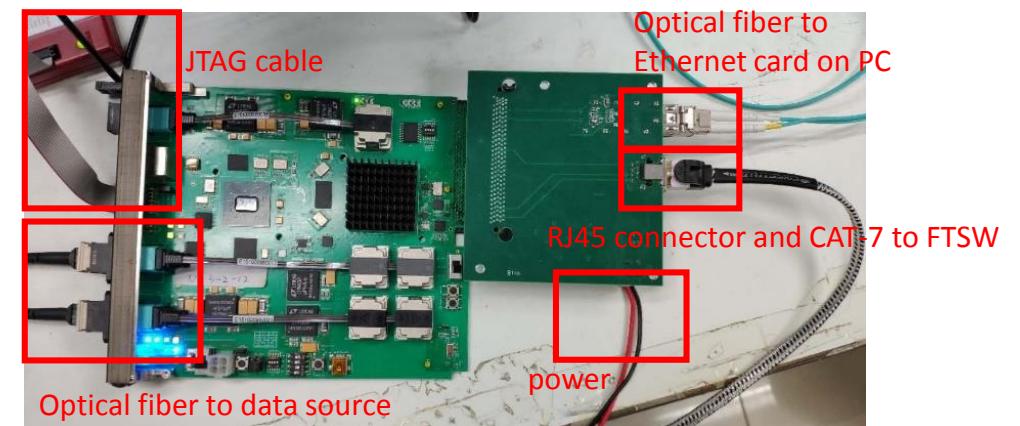
New version for Belle II

Demo system Setup at IHEP

- Photo of Full Demo System



CPPF and PC in working



CPPF and Interface to FTSW/PC

Demo system Based on 10GbE

- HSLB Clock/Trigger Gen

- --Generate 125MHz clock
- --Generate trigger signal
- Trigger rate is controlled by PC;
- Trigger signal can be masked by feedback BUSY signal;
- --send clock and trigger to fan-out board

- Fan-out board

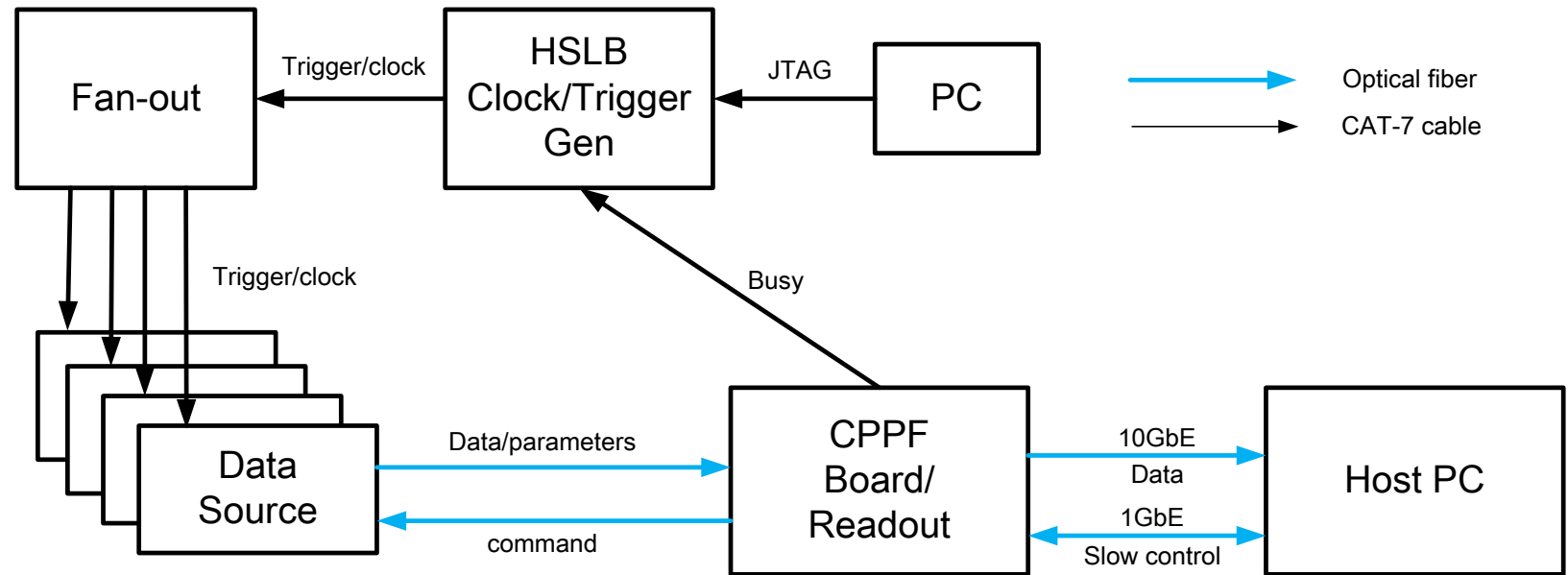
- Fan out 125MHz clock and trigger signal to Data source boards,

- Data source board

- --use hslb as data source (*belle2link-0.19*)
- --generate dummy data and provide some register for slow control test

- Readout board

- • use CPPF as readout board
- implement belle2link(data merge and slow control) and some COPPER and ROPC function on it
- output data to PC and receive command from PC via Ethernet.



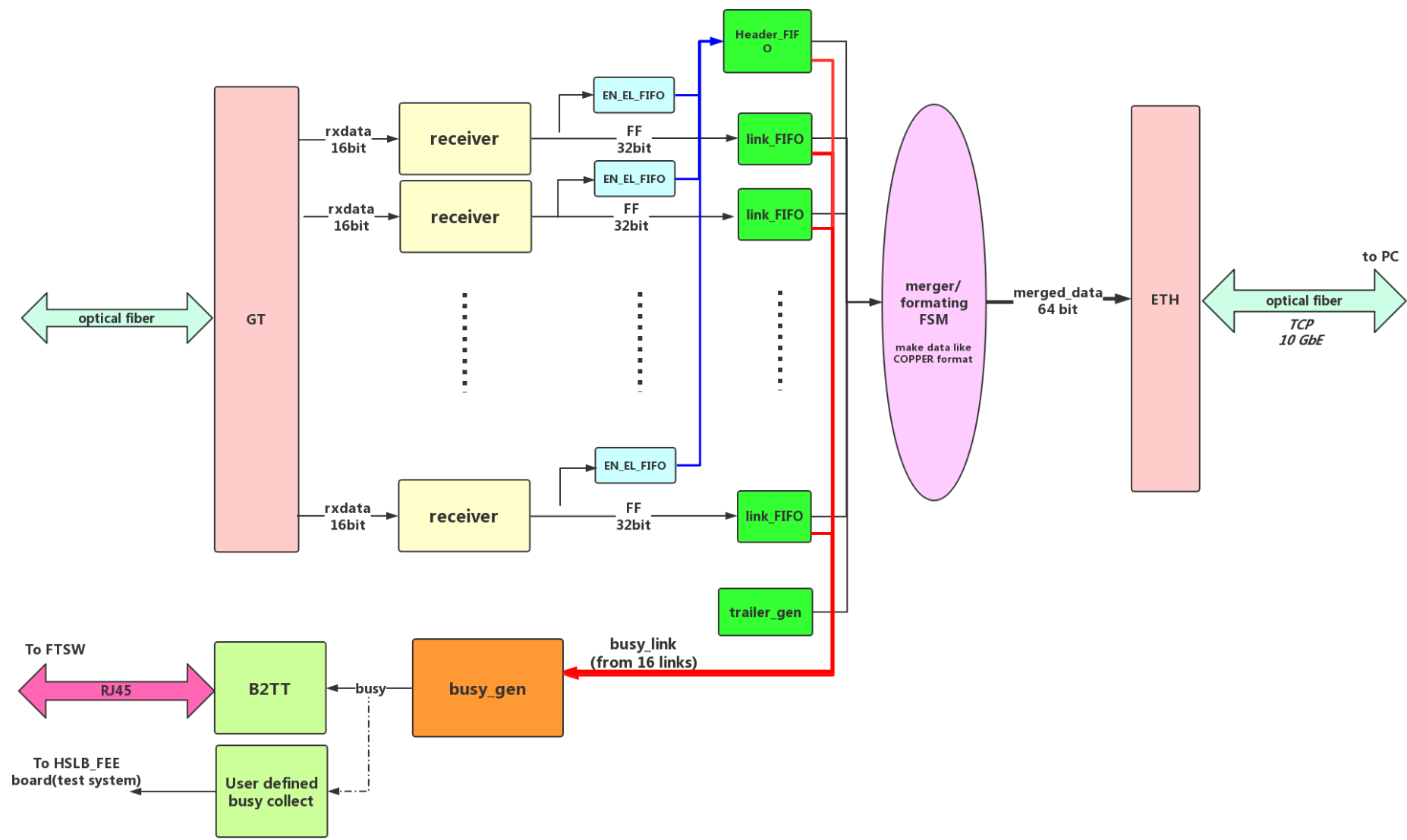
- host pc

- receive data from CPPF through 10G Ethernet
- send slow control command to CPPF via SiTCP

- Use an short-time(10min) evaluation version 10GbE IP core(from a company), implemented on CPPF

Firmware structure

Data merger based on 10GbE

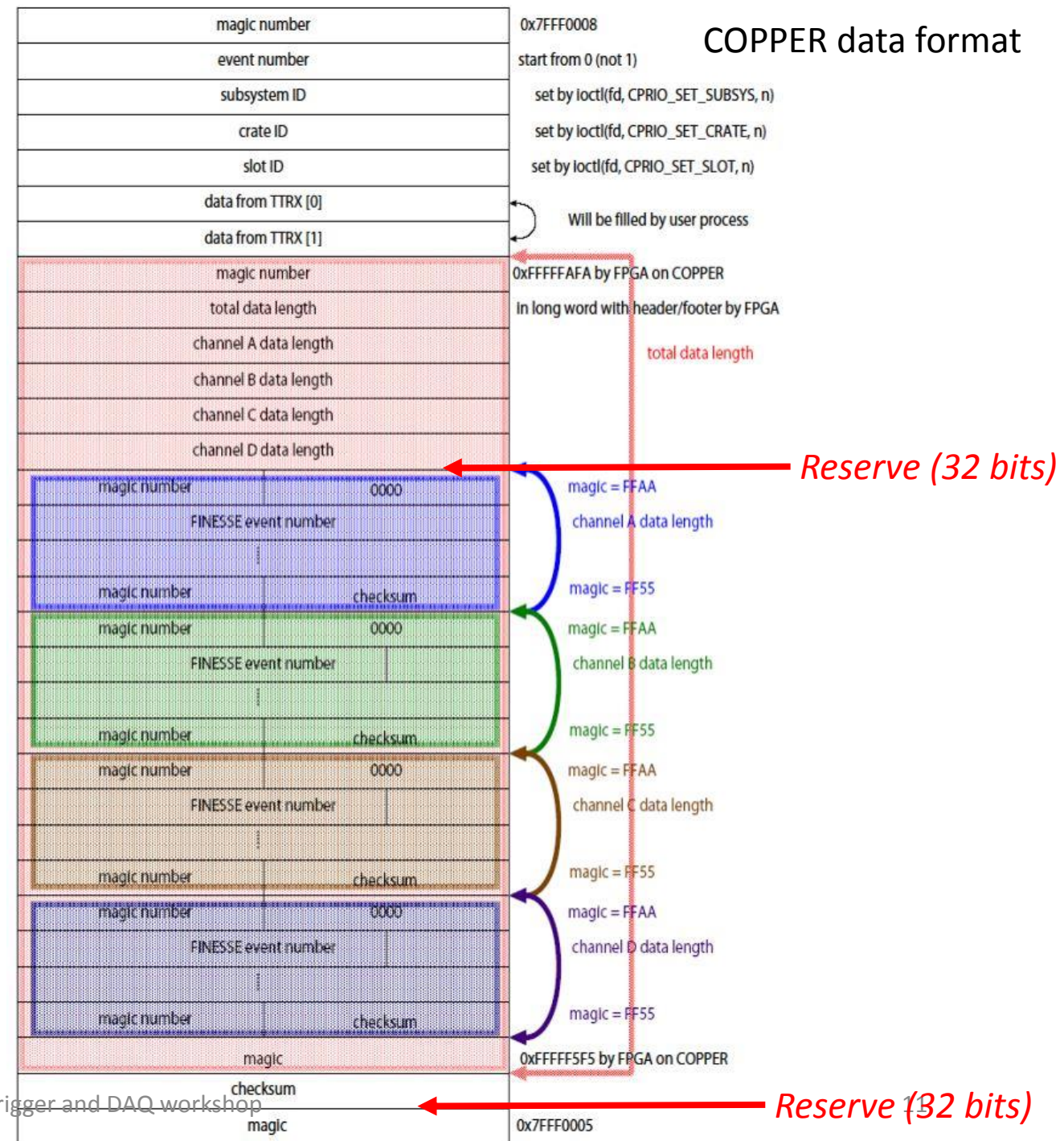


COPPER Data format based on 10 GbE(4 links)

- 10GbE IP core data width 64 bits;
- Old COPPER data format header:
 - 13*32bits

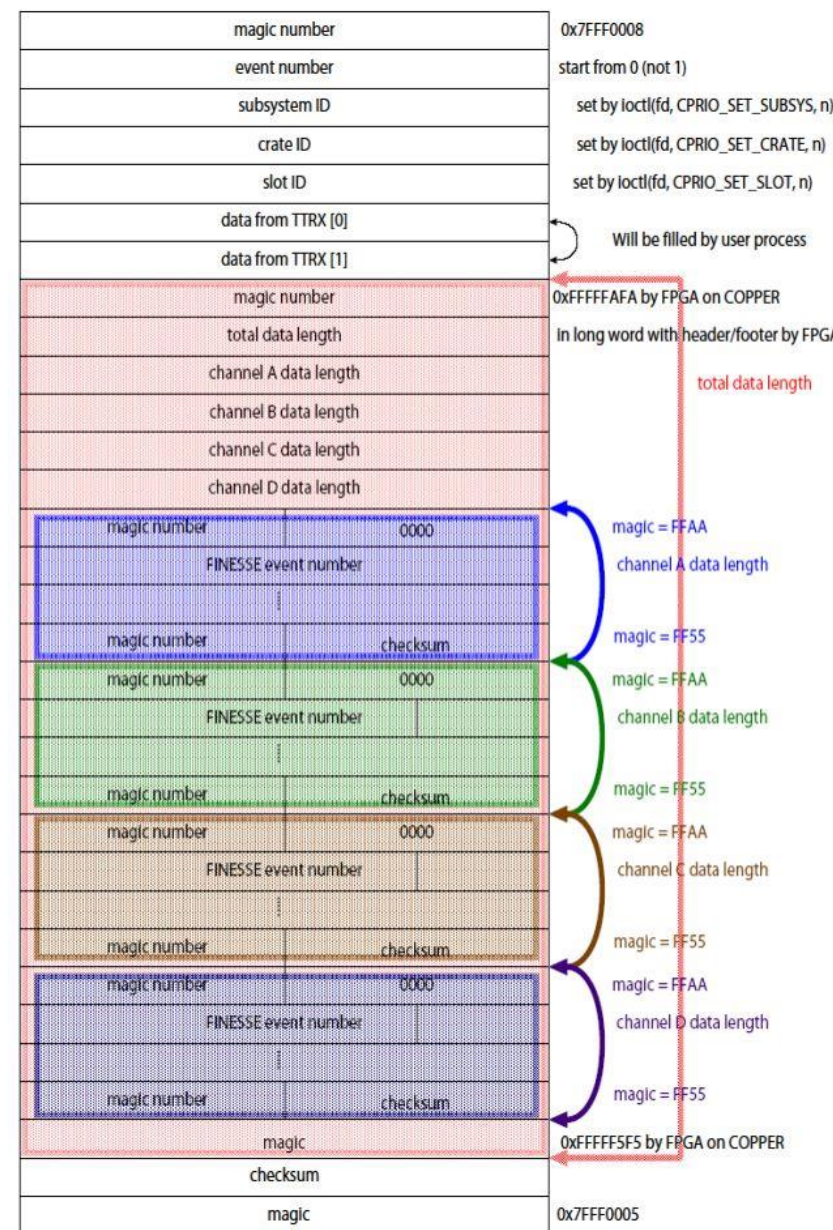
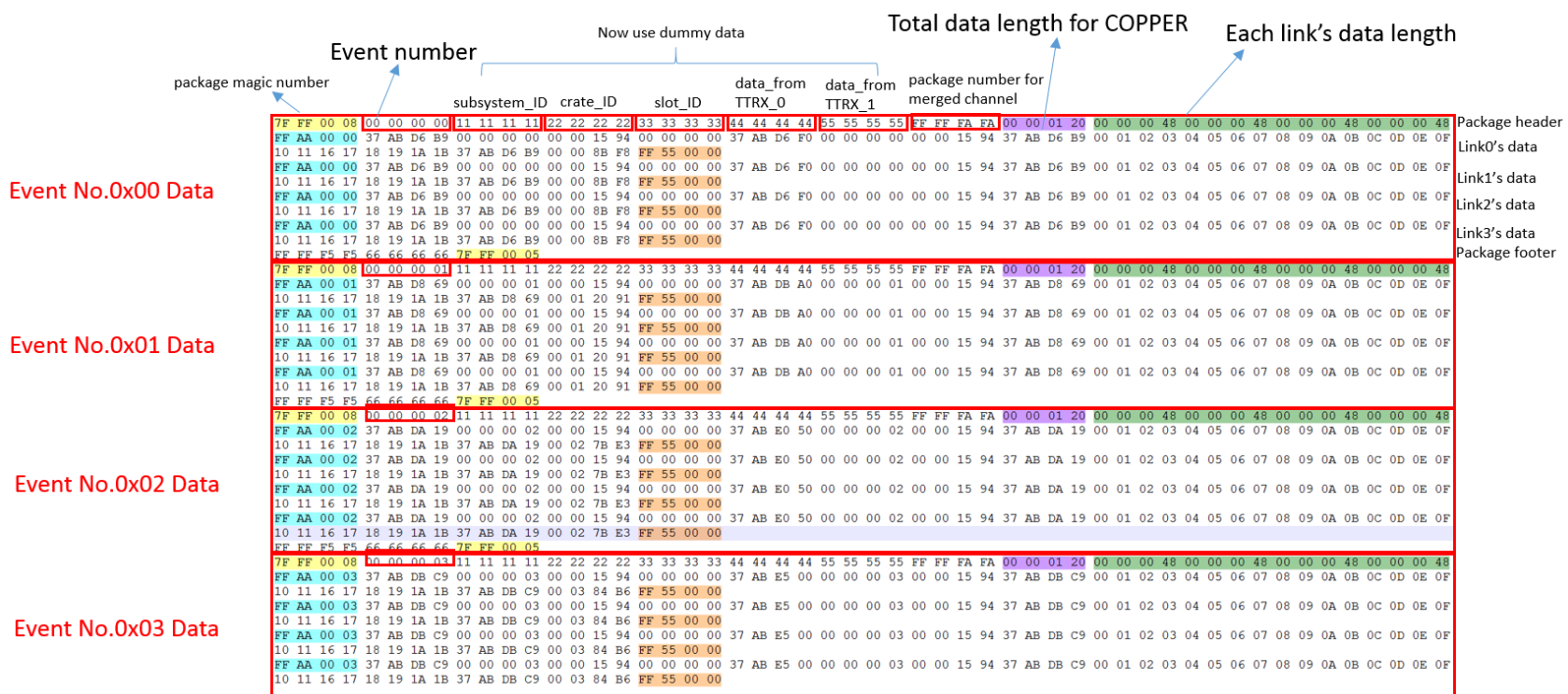
Modification on COPPER Data format:

- Inserting a 32bit word called *Reserve* after *channel D data length*,
- make the header into 14*32bit,
- Inserting a 32bit word called *Reserve* in *trail*,
- *Make the trail into 4*32bit*



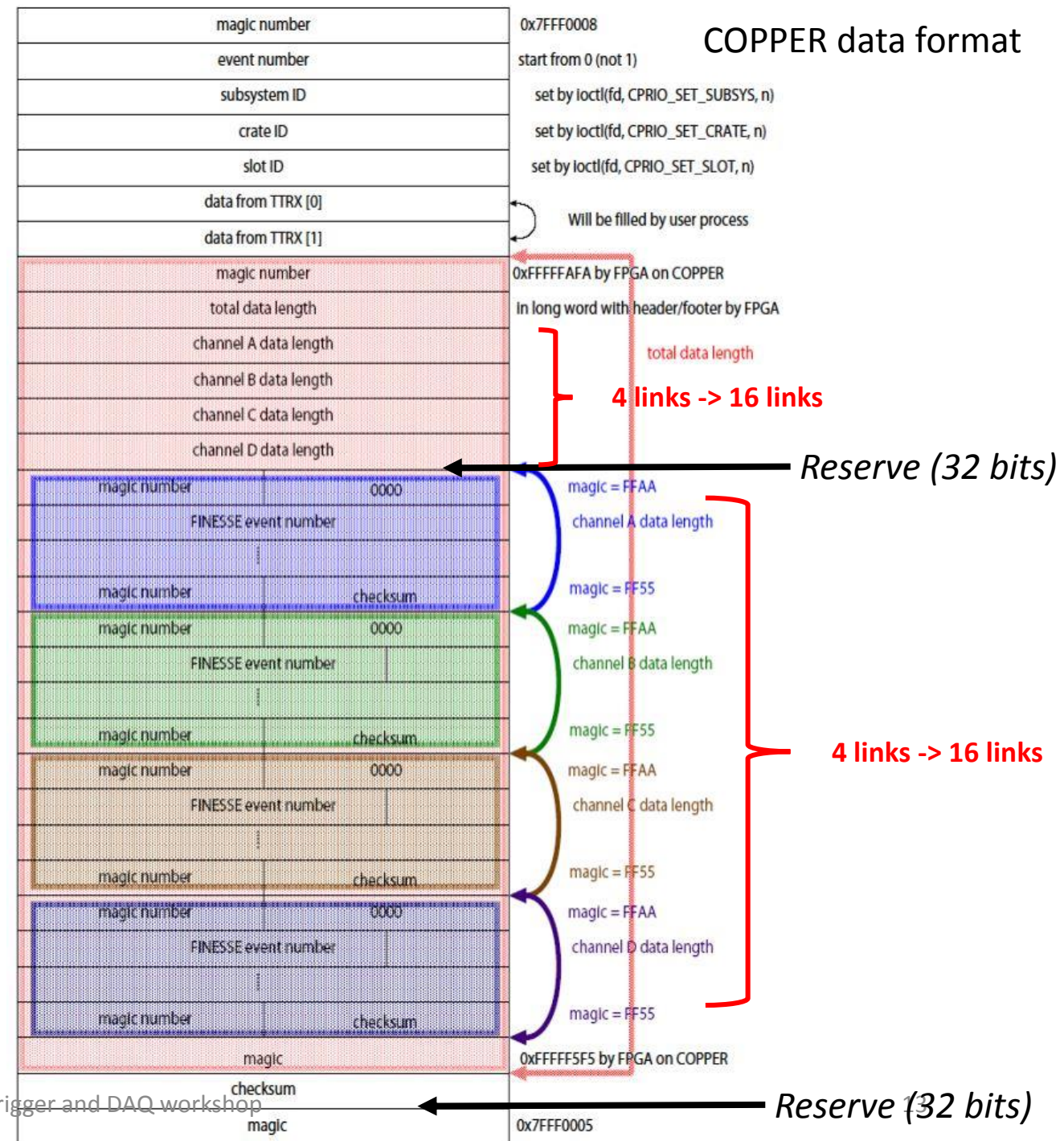
Merged data format(4 links)

First 4 events shows below follows COPPER format, event number is incremented



COPPER-like Data format based on 10 GbE(16 links)

- For 16 links
 - Similar to 4 link COPPER data format
 - Header add 12 more 32bit word to represent the data length of added links and *total data length* is the sum of 16 links' data length
 - 4 links -> 16 links data in one event
- Data format for 16 or 24 links should be further discussed with Yamada-san.



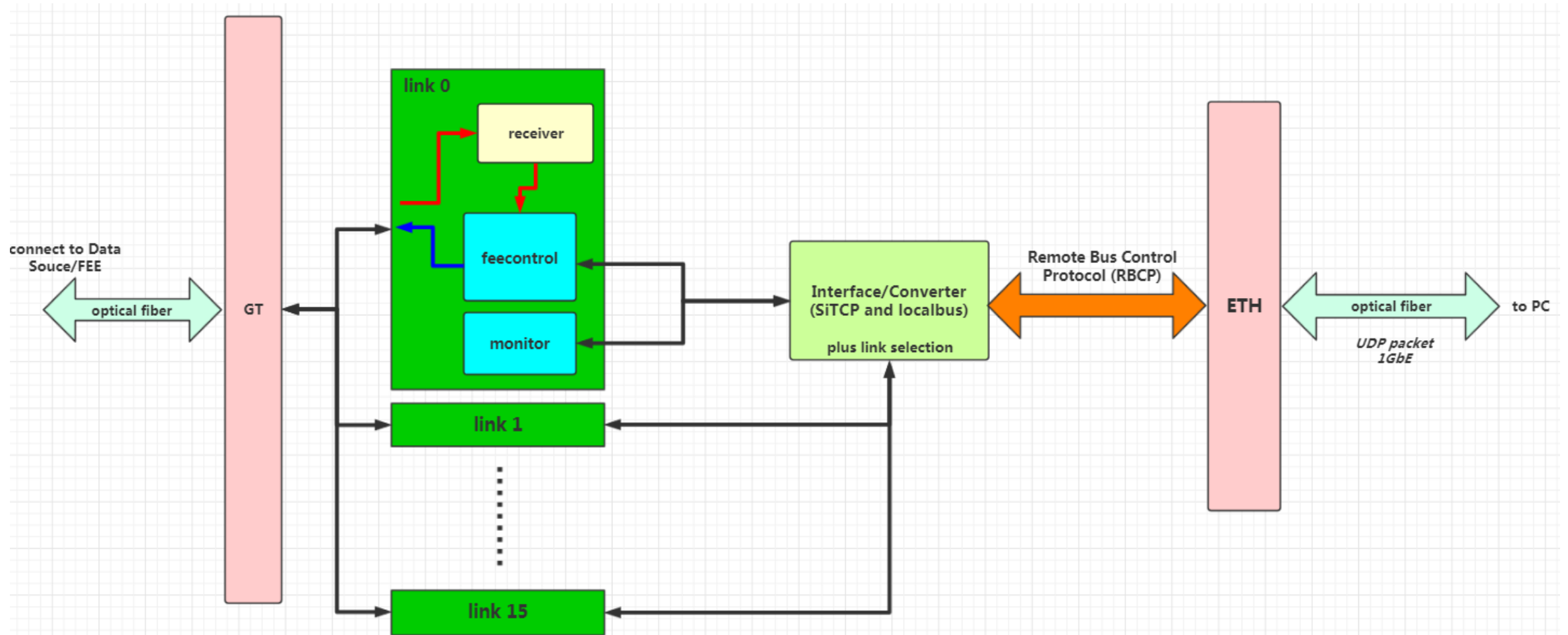
COPPER-like Data format based on 10 GbE(16 links)

- PC received data(1st event) is shown as right,
- COPPER event number and link event number are checked.
- Header of COPPER and link header and footer are checked.
- Event number are checked whether they are increased one by one.
- About 100 thousands events are received and checked, and data are correct.

Header { 00000000 7f ff 00 08 00 00 11 11 11 22 22 22 22
00000010 33 33 33 33 33 44 44 44 55 55 55 ff fa fa
00000020 00 00 01 20 00 00 00 12 00 00 00 12 00 00 00 12
00000030 00 00 00 12 00 00 00 12 00 00 00 12 00 00 00 12
00000040 00 00 00 12 00 00 00 12 00 00 00 12 00 00 00 12
00000050 00 00 00 12 00 00 00 12 00 00 00 12 00 00 00 12
Link 0 { 00000060 00 00 00 12 77 77 77 77 ff aa 00 00 00 00 00 00
00000070 00 00 00 00 00 00 00 00 87 65 43 21 00 00 00 00
00000080 ff ff ff ff 00 00 00 00 00 00 0f 00 01 02 03
00000090 04 05 06 07 08 09 0a 0b 0c 0d 0e 0f 10 11 16 17
000000a0 18 19 1a 1b 00 00 00 00 00 00 6a 0d ff 55 00 00
000000b0 ff aa 00 00 00 00 00 00 00 00 00 00 00 00 00 00
000000c0 87 65 43 21 00 00 00 00 ff ff ff ff 00 00 00 00
000000d0 00 00 00 0f 00 01 02 03 04 05 06 07 08 09 0a 0b
000000e0 0c 0d 0e 0f 10 11 16 17 18 19 1a 1b 00 00 00 00
000000f0 00 00 6a 0d ff 55 00 00 ff aa 00 00 00 00 00 00
00000100 00 00 00 00 00 00 00 00 87 65 43 21 00 00 00 00
00000110 ff ff ff ff 00 00 00 00 00 00 00 0f 00 01 02 03
00000120 04 05 06 07 08 09 0a 0b 0c 0d 0e 0f 10 11 16 17
00000130 18 19 1a 1b 00 00 00 00 00 00 6a 0d ff 55 00 00 00
00000140 ff aa 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00000150 87 65 43 21 00 00 00 00 ff ff ff ff 00 00 00 00
00000160 00 00 00 0f 00 01 02 03 04 05 06 07 08 09 0a 0b
00000170 0c 0d 0e 0f 10 11 16 17 18 19 1a 1b 00 00 00 00
00000180 00 00 6a 0d ff 55 00 00 ff aa 00 00 00 00 00 00
00000190 00 00 00 00 00 00 00 00 87 65 43 21 00 00 00 00
000001a0 ff ff ff ff 00 00 00 00 00 00 0f 00 01 02 03
000001b0 04 05 06 07 08 09 0a 0b 0c 0d 0e 0f 10 11 16 17
000001c0 18 19 1a 1b 00 00 00 00 00 00 6a 0d ff 55 00 00 00
000001d0 ff aa 00 00 00 00 00 00 00 00 00 00 00 00 00 00
000001e0 87 65 43 21 00 00 00 00 ff ff ff ff 00 00 00 00
000001f0 00 00 00 0f 00 01 02 03 04 05 06 07 08 09 0a 0b
00000200 0c 0d 0e 0f 10 11 16 17 18 19 1a 1b 00 00 00 00
00000210 00 00 6a 0d ff 55 00 00 ff aa 00 00 00 00 00 00
00000220 00 00 00 00 00 00 00 00 87 65 43 21 00 00 00 00
00000230 ff ff ff ff 00 00 00 00 00 00 0f 00 01 02 03
00000240 04 05 06 07 08 09 0a 0b 0c 0d 0e 0f 10 11 16 17
00000250 18 19 1a 1b 00 00 00 00 00 00 6a 0d ff 55 00 00
00000260 ff aa 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00000270 87 65 43 21 00 00 00 00 ff ff ff ff 00 00 00 00
00000280 00 00 00 0f 00 01 02 03 04 05 06 07 08 09 0a 0b
00000290 0c 0d 0e 0f 10 11 16 17 18 19 1a 1b 00 00 00 00
000002a0 00 00 6a 0d ff 55 00 00 ff aa 00 00 00 00 00 00
000002b0 00 00 00 00 00 00 00 00 87 65 43 21 00 00 00 00
000002c0 ff ff ff ff 00 00 00 00 00 00 0f 00 01 02 03
000002d0 04 05 06 07 08 09 0a 0b 0c 0d 0e 0f 10 11 16 17
000002e0 18 19 1a 1b 00 00 00 00 00 00 6a 0d ff 55 00 00
000002f0 ff aa 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00000300 87 65 43 21 00 00 00 00 ff ff ff ff 00 00 00 00
00000310 00 00 00 0f 00 01 02 03 04 05 06 07 08 09 0a 0b
00000320 0c 0d 0e 0f 10 11 16 17 18 19 1a 1b 00 00 00 00
00000330 00 00 6a 0d ff 55 00 00 ff aa 00 00 00 00 00 00
00000340 00 00 00 00 00 00 00 00 87 65 43 21 00 00 00 00
00000350 ff ff ff ff 00 00 00 00 00 00 0f 00 01 02 03
00000360 04 05 06 07 08 09 0a 0b 0c 0d 0e 0f 10 11 16 17
00000370 18 19 1a 1b 00 00 00 00 00 00 6a 0d ff 55 00 00
00000380 ff aa 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00000390 87 65 43 21 00 00 00 00 ff ff ff ff 00 00 00 00
000003a0 00 00 00 0f 00 01 02 03 04 05 06 07 08 09 0a 0b
000003b0 0c 0d 0e 0f 10 11 16 17 18 19 1a 1b 00 00 00 00
000003c0 00 00 6a 0d ff 55 00 00 ff aa 00 00 00 00 00 00
000003d0 00 00 00 00 00 00 00 00 87 65 43 21 00 00 00 00
000003e0 ff ff ff ff 00 00 00 00 00 00 0f 00 01 02 03
000003f0 04 05 06 07 08 09 0a 0b 0c 0d 0e 0f 10 11 16 17
00000400 18 19 1a 1b 00 00 00 00 00 00 6a 0d ff 55 00 00
00000410 ff aa 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00000420 87 65 43 21 00 00 00 00 ff ff ff ff 00 00 00 00
00000430 00 00 00 0f 00 01 02 03 04 05 06 07 08 09 0a 0b
00000440 0c 0d 0e 0f 10 11 16 17 18 19 1a 1b 00 00 00 00
00000450 00 00 6a 0d ff 55 00 00 ff aa 00 00 00 00 00 00
00000460 00 00 00 00 00 00 00 00 87 65 43 21 00 00 00 00
00000470 ff ff ff ff 00 00 00 00 00 00 0f 00 01 02 03
00000480 04 05 06 07 08 09 0a 0b 0c 0d 0e 0f 10 11 16 17
00000490 18 19 1a 1b 00 00 00 00 00 00 6a 0d ff 55 00 00
000004a0 ff aa 00 00 00 00 00 00 00 00 00 00 00 00 00 00
000004b0 87 65 43 21 00 00 00 00 ff ff ff ff 00 00 00 00
000004c0 00 00 00 0f 00 01 02 03 04 05 06 07 08 09 0a 0b
000004d0 0c 0d 0e 0f 10 11 16 17 18 19 1a 1b 00 00 00 00
000004e0 00 00 6a 0d ff 55 00 00 ff ff ff ff 00 00 00 00

Link 15 { trailer

Firmware structure-*Slow control*



Firmware structure: Slow Control

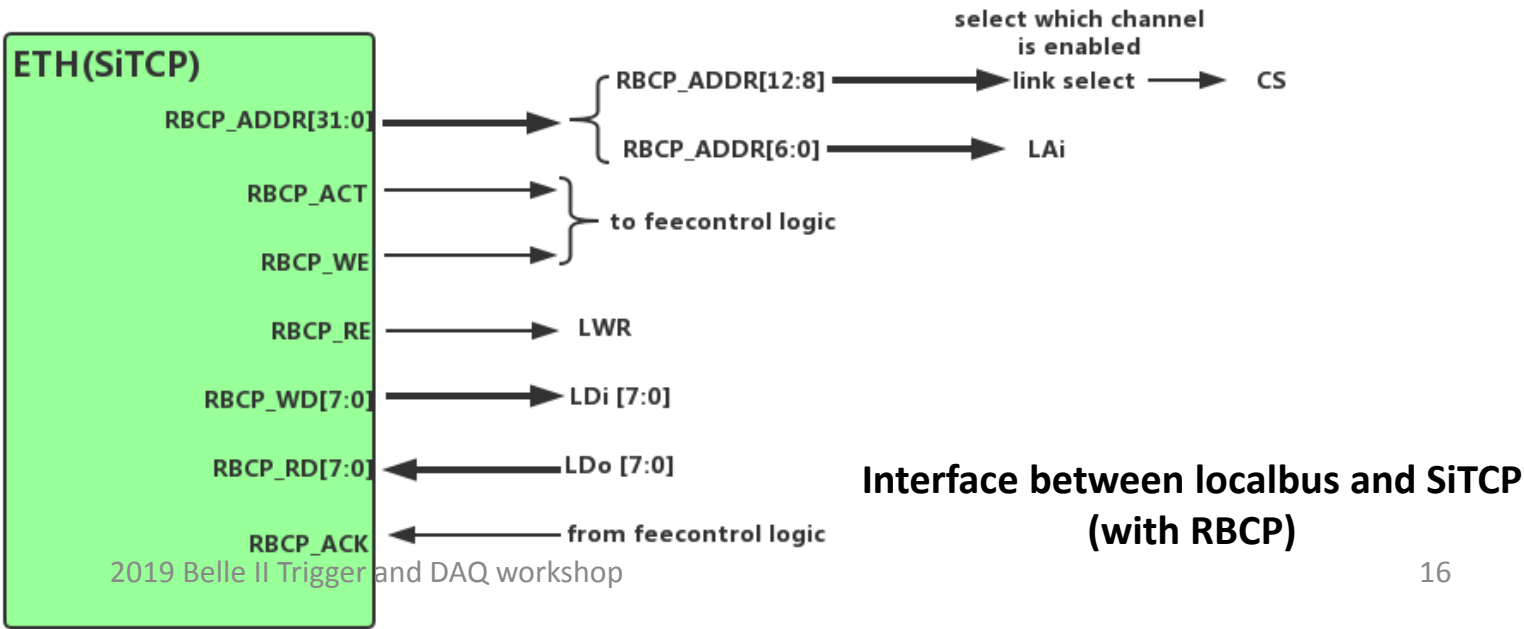
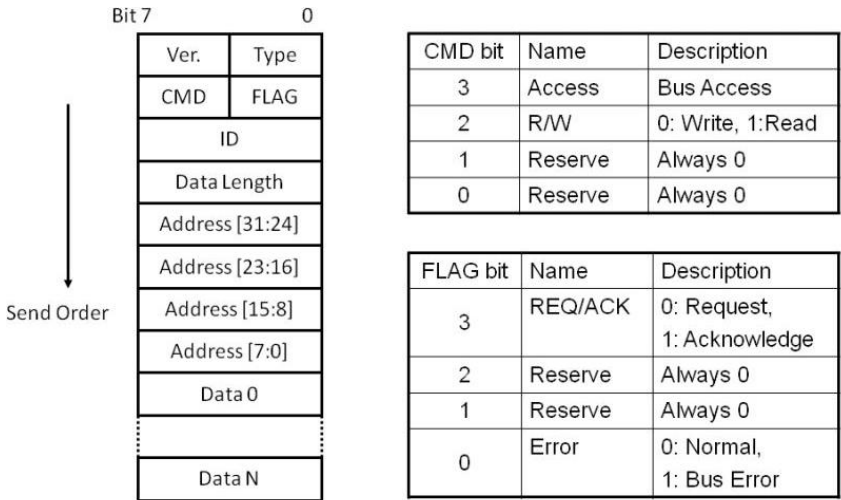
Interface between *localbus* and *SiTCP*

Signal name	I/O	Description
RBCT_ACT	O	Indicates the bus operating.
RBCT_ADDR[31:0]	O	Address in access
RBCT_WE	O	Write enable
RBCT_WD[7:0]	O	Write data
RBCT_RE	O	Read enable
RBCT_RD[7:0]	I	Read data
RBCT_ACK	I	Access response

RBCT signal description



UDP RBCP packet format



Slow control test result

Slow control

Main functions are realized and verified

--8 bit register read and write—A7D8

--32 bit register read and write—A16D32

--Stream write —*Stream*

```
SUN@SUN-PC /cygdrive/c/Users/SUN/Desktop/caopc_sitcpudp_new/RBCP_sample
$ ./rbcp.exe 192.168.10.16 4660
$ B2LDo -a -p delay 0x1
B2LDo: delay was set as: 0x01

$ B2LDo -b -p delay 0x2
B2LDo: delay was set as: 0x02

$ B2LDo -c -p delay 0x3
B2LDo: delay was set as: 0x03

$ B2LDo -d -p delay 0x43
B2LDo: delay was set as: 0x43
```

A7D8: Delay parameter was written and read back correctly

```
Administrator@PC-201707170902 /cygdrive/c/User
l_udp_tcp/B2linkTcpUdp
$ ./B2ldoTcpUdp.exe 192.168.10.16 4660

B2LDo$ setreg -c 0x0101 0x03050709

The register value was set as: 0x03050709
```

A16D32 example

```
/cygdrive/c/Users/Administrator/Desktop/B2linkTcpUdp
Administrator@PC-201707170902 /cygdrive/c/Users/Administrator/Desktop/B2linkTcpU
dp
$ ./B2ldoTcpUdp.exe 192.168.10.16 4660

B2LDo$ testa7d8 -a 1000

The error count is 0

B2LDo$ testa16d32 -a 0x0101 1000

The error count is 0

B2LDo$ testa7d8 -a 10000

The error count is 0

B2LDo$ testa16d32 -a 0x0101 10000

The error count is 0

B2LDo$ testa7d8 -b 100

The error count is 0

B2LDo$ testa7d8 -c 100

The error count is 0

B2LDo$ testa7d8 -d 100

The error count is 0

B2LDo$ testa16d32 -a 0x0101 100

The error count is 0

B2LDo$ testa16d32 -b 0x0101 100

The error count is 0

B2LDo$ testa16d32 -c 0x0101 100

The error count is 0

B2LDo$ testa16d32 -d 0x0101 100

The error count is 0

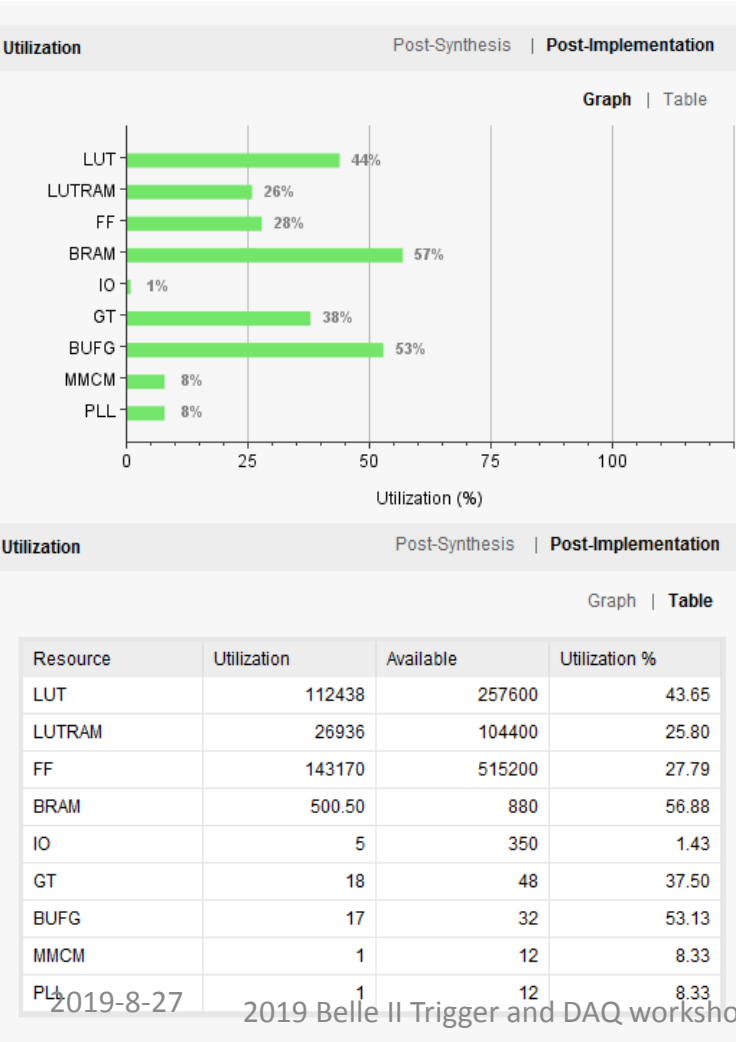
B2LDo$
```

Test slow control, A7D8 and A16D32,
up to 10000 times w/r, without error

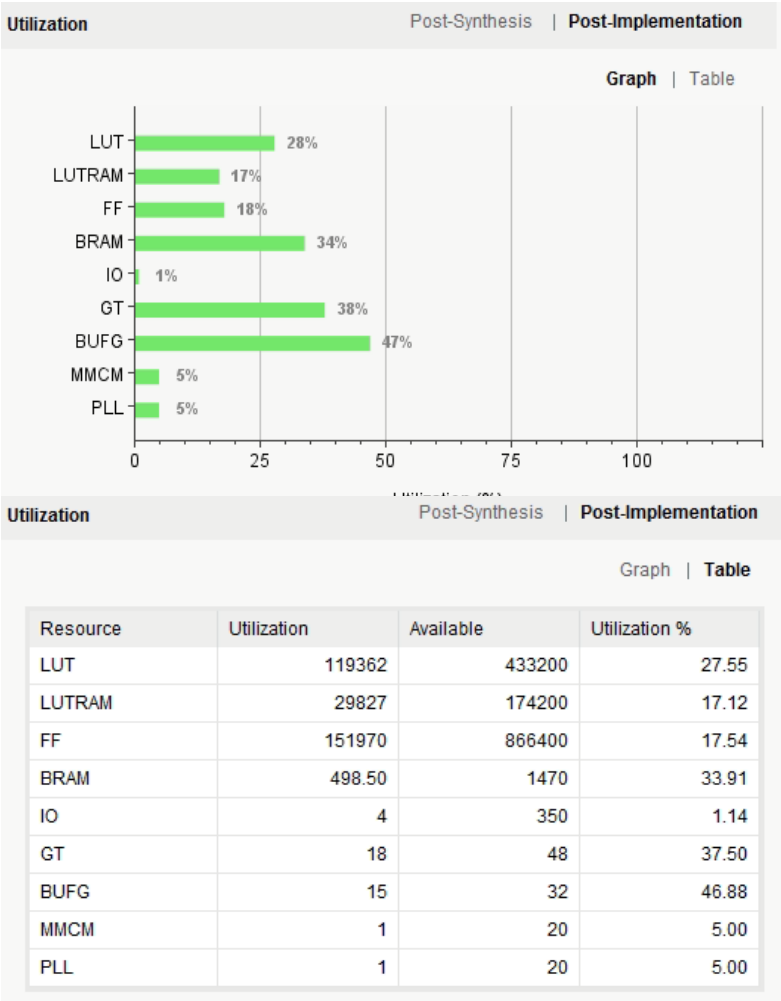
Resource utilization in CPPF

- 16 links version resource utilization in CPPF.
- BRAM is used 57% in old version of CPPF.
- And BRAM 34 % used in new version of CPPF.
- New version of CPPF based on xc7vx690t can provide enough BRAM for Data buffering.

Old CPPF
Device: Xc7vx415tffg1158-2



New CPPF for Belle II
Device: Xc7vx690tffg1158-2



Status of the IHEP Demo system

- Based on 10GbE(4 channels)

- Functions are based 4 inputs implementation of COPPER
- Data output to Event builder/readout PC via Optical Switch
- Four Slow control links in one CPPF
- TTD interface, BUSY handshake with FTSW

Done

Done

Done (simple CDC parameters)

Done based on SiTCP, For 10 GbE Waiting for new version of CPPF

- Data check function
 - checking event number
 - CRC and others not yet

Done

- Based on 10GbE(16 channels)

- Functions are based 4 inputs implementation of COPPER
- Data output to Event builder/readout PC via Optical Switch
- 16 Slow control links in one CPPF
- TTD interface, BUSY handshake with FTSW

Done

Done

Done (simple CDC parameters)

Done based on SiTCP, For 10 GbE Waiting for new version of CPPF

- Data check function
 - checking event number
 - CRC and others not yet

Done

Manpower and tasks

- Zhen-An LIU: Overall.
- Jingzhou ZHAO/Jia TAO: Main person for the implementation.
- Wenxuan GONG/Na WANG: Hardware modification and production.
- Hanjun KOU: readout via 1G/10G Ethernet implementation with SITCP, B2TT implementation.
- Pengcheng CAO: Slow Control and control firmware.
- Jianing SONG: Hardware testing.
- Two students from Fudan Uni. are also possible

Summary

- CPPF is the main board in IHEP Demo system for DAQ upgrade.
- New version of CPPF for Belle II is ready and under testing.
- Demo system at IHEP achieved success for 16 channels.
 - Based on 10GbE
- IHEP proposal could meet all requirement
 - Open, scalable, upgradable, re-configurable hardware platform
 - Suitable for future FEE and DAQ networking upgrade also
- Join test in KEK could start to plan.