Summary of the DAQ Session of FSP Workshop

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The goal of the FSP workshop was to find a way for the rescue of the low-momentum pion clusters in the pixel detector, PXD. This will require the incorporation of the hit information from the silicon strip detector, SVD, and the reconstruction of tracks from these two types of detectors. To do this, we will need to change the data processing chain of the PXD.

One important point in the consideration of the possible solution is the expected data rate of the full PXD. Current beam background projection takes into account the detector operation in Belle 2 and scales the background rate with the luminosity. This allows us to estimate an average event size of 100 kB/s at luminosity of $2 \cdot 10^{35}$. It will correspond to the data rate to around 3 GB/s with nominal 30 kHz trigger rate and luminosity of $2 \cdot 10^{35} cm^{-2} s^{-1}$. It puts the PXD data rate to the SVD level. This data rate does not fully take into account effects associated with detector and front-end electronics damage due to abnormal beam loss events, which are negligible at the current conditions.

With the above-mentioned requirements, several options were considered for the upgrade of the read-out chain. The DAQ group considers integration of the PXD data flow similarly to other detectors more expensive now. The more realistic option is keeping the PXD data flow separate from the remaining DAQ and merge PXD data, reduced with HLT decision and regions-of-interests, into the main data stream in the event builder 2 as it is done in the current system. The PXD will continue to use the local data taking infrastructure, known as "BonnDAQ", for detector calibration.

We plan to evaluate a possibility to identify low-momentum pion clusters using track reconstruction and classification of cluster using machine learning algorithms. Since algorithms used in the cluster rescue are software algorithms, we must first bring data to the memory of the computer where these algorithms are executed. To accomplish this, two new FPGA-based cards will be added to the read-out chain.

The first card, XCV35P-2 or XCV37P-2, will process raw data and associate adjacent hits in the pixel detector with clusters effectively offloading this functionality to hardware. While this card has a PCIe interface, we do not plan to use it, because change of firmware, which is expected to happen often during commissioning, will require long downtime due the necessity to reboot the host computer.

The second card, PCIe40, is installed in the computer to receive data from the clustering engine and write them to memory. While the PCIe40 is already used by TOP and KLM detectors for data read-out, its operation has shown that development and operation of the card requires an expert from the DAQ group. Because the environment of the PXD read-out chain is different from other detectors, for example different protocols and data rates will be used, the firmware of the card will have to be adapted by DAQ group to be used in the PXD setup. This was raised as a concern during the discussion.

Another issue, raised during the discussion, concerns read-out path of the SVD data. One of the possibilities would be to read a copy of data from the event builder 1 over Ethernet.

Another possibility is reading a copy of data from the event builder 1 over Ethernet. This solution uses a standard Ethernet interface, therefore reading data by computer is straight forward. However, the implementation of this solution depends on the performance of the SVD read-out computers and further discussion with the DAQ group is needed. The upgrade of the SVD read-out to the PCIe40-based system is planned for summer shutdown 2022.

According to a DAQ expert, the event builder 2 will also profit from the new read-out chain, because it will reduce the number of data sources thus reducing the load on the event builder process.