PXD Read for Slow Particle Tracking

Igor Konorov

Institute for Hadronic Structure and Fundamental Symmetries (E18)

TUM Department of Physics

Technical University of Munich

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Motivation

1. 20 us integration time of PXD => pileup will cause high detector occupancy and produce big amount of data

2. PXD data reduction will be performed by preserving hits from ROIs
   - ROIs are extrapolated track coordinates in PXD
   - Tracks are reconstructed in CDC and SVD by HLT without PXD information

   Is SVD ONLY track reconstruction included in HLT?

3. Procedure will lead to loss of hits produced by slow particles < 100 MeV

PXD Occupancy and Data Rate

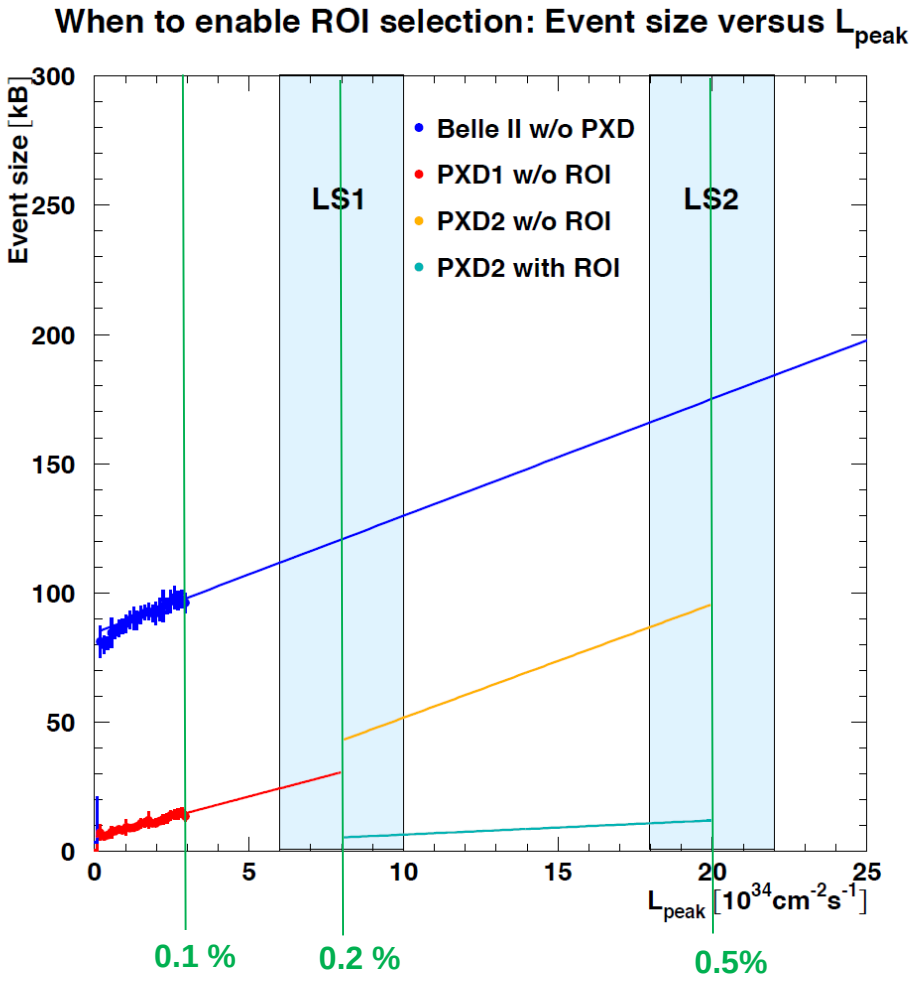
Detector occupancy in 2021 runs

- 0.1 % => 15 kB/ev => 150MB/s @ 10kHz before HLT

Expectations before LS2 @ $2 \cdot 10^{35}$

- 0.5 % => 100 kB/ev => 3 GB/s @ 30kHz before HLT

Expected that fraction of PXD data wo ROI will grow from 10% to 60% to compare to all other detectors before LS2



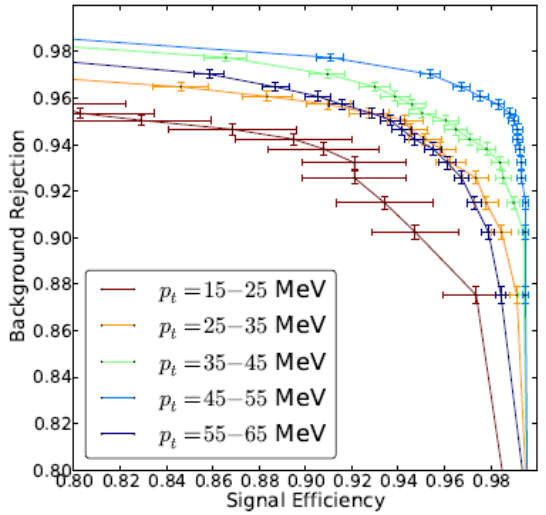
Cluster Analysis Cluster Rescue

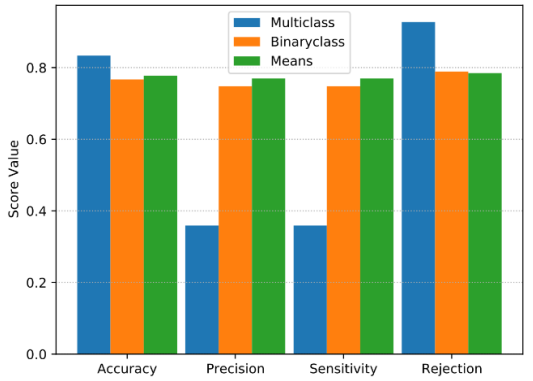
Identification of Low Momentum Pion by Cluster shape and cluster charge

- Steffen Bähr Karlsruher , KIT
  - Full cluster reconstruction + NN
- Johannes Bilk, Timo Schellhaas, Giessen Uni.
  - Convolution NN
  - Support Vector Machine

Simulation results about 80% efficiency of cluster rescue with MC data
How well MC can reproduce real results ?

- Detector response
- Background





CNN reaches 78% precision (efficiency) and 79% rejection (for multi-class case).

Johannes Bilk

Alternative approach

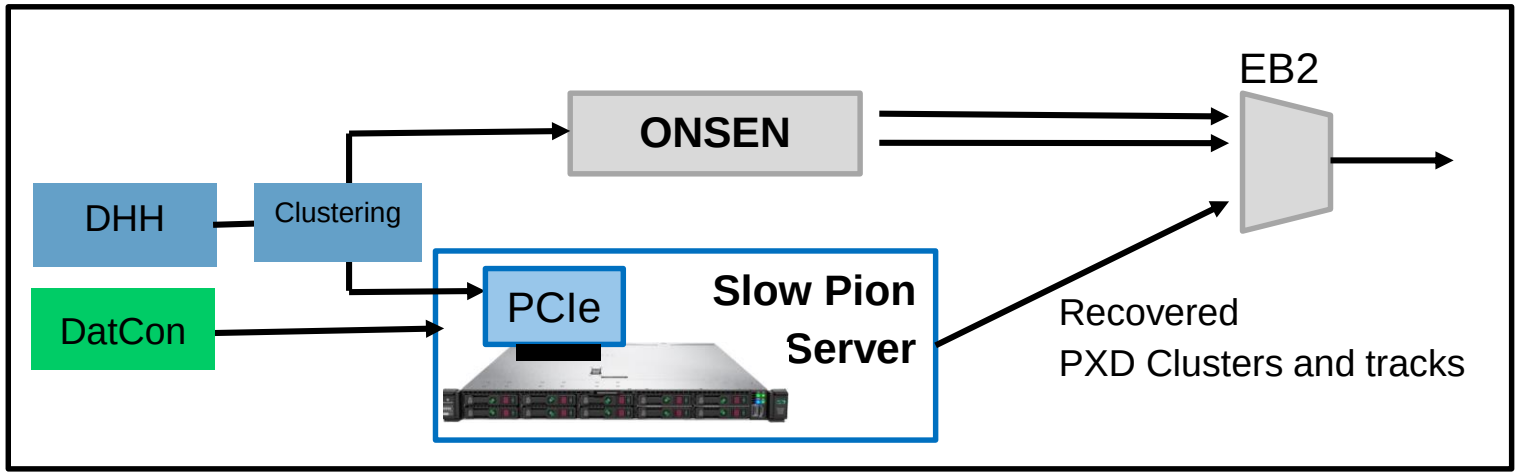
- Preserve 100% of PXD data, no ROI
  - If HLT rejects 90% of data then PXD data will grow from 0.2 => 4 PB/year by LS2

- Reject hits/clusters after slow pion tracking : PXD Clustering => SVD+PXD ONLY tracking

Data Flow I

Input : DHH provides PXD data in a form of clusters to speed up track reconstruction algorithms

1. Standalone pion track reconstruction



Slow pion server

- BASF2 track reconstruction optimized for fast reconstruction

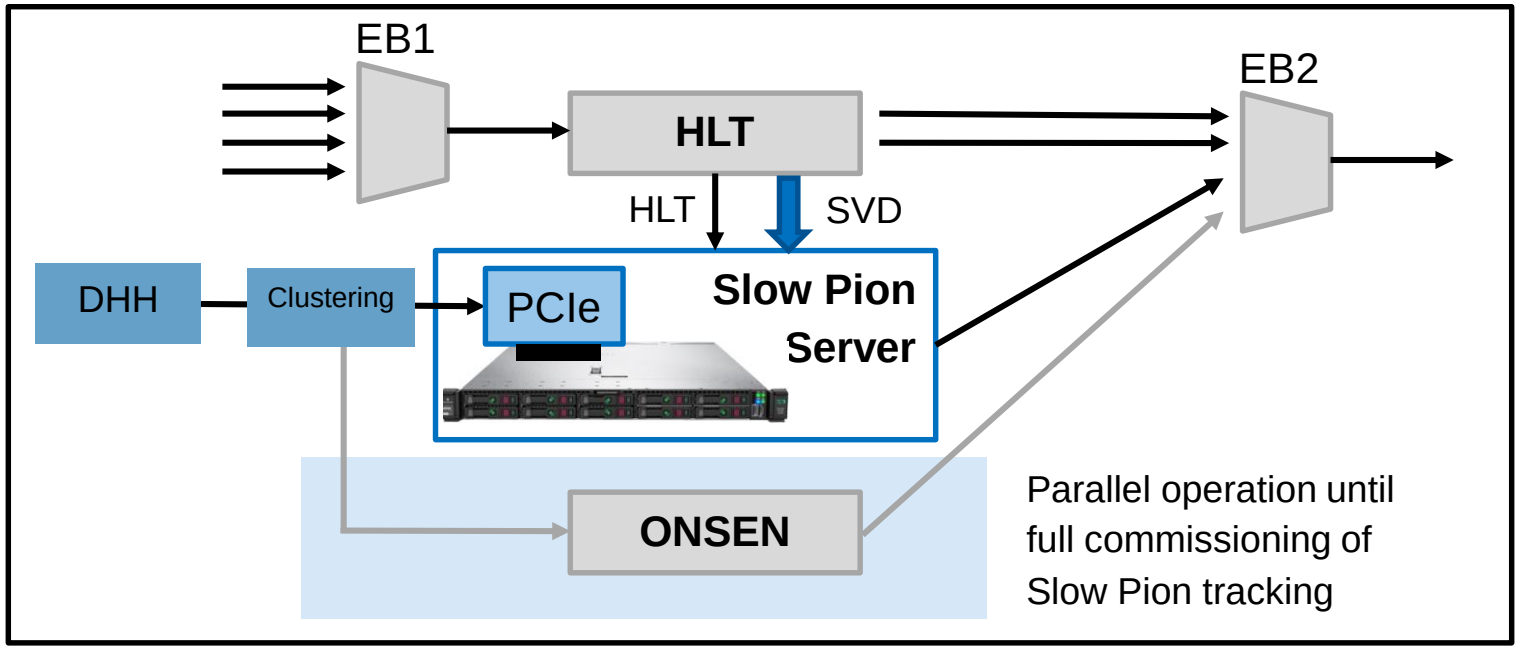
Advantage :

- Integration wo affecting current system

Disadvantage :

- Can DATCON be used for providing SVD information?
- Non standard SVD data source

Data Flow II



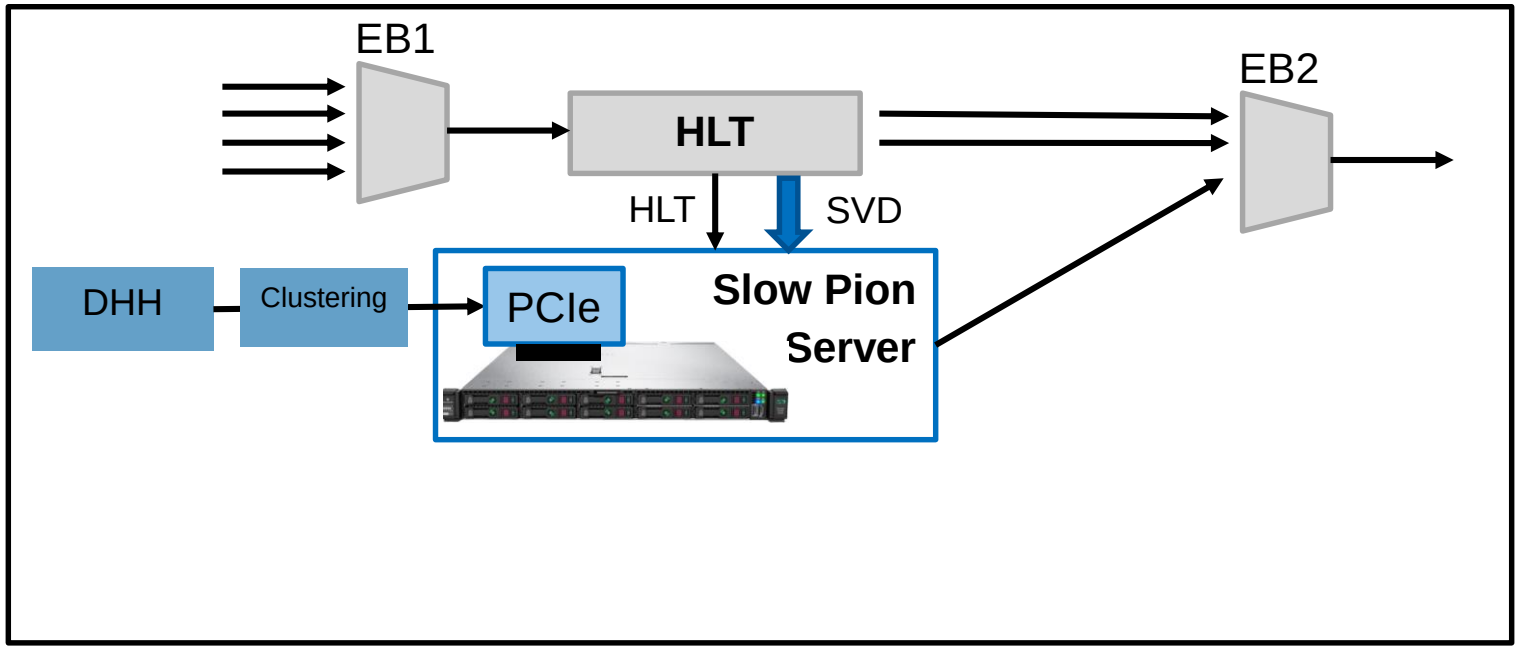
Slow Pion Server

- 128-256 GB RAM
- 10/25 GEthernet
- BASF2 tracking optimized for fast reconstruction

Advantage :

- Overcome ONSEN memory limit
- Standard data flow
- Minimum hardware

Data Flow III



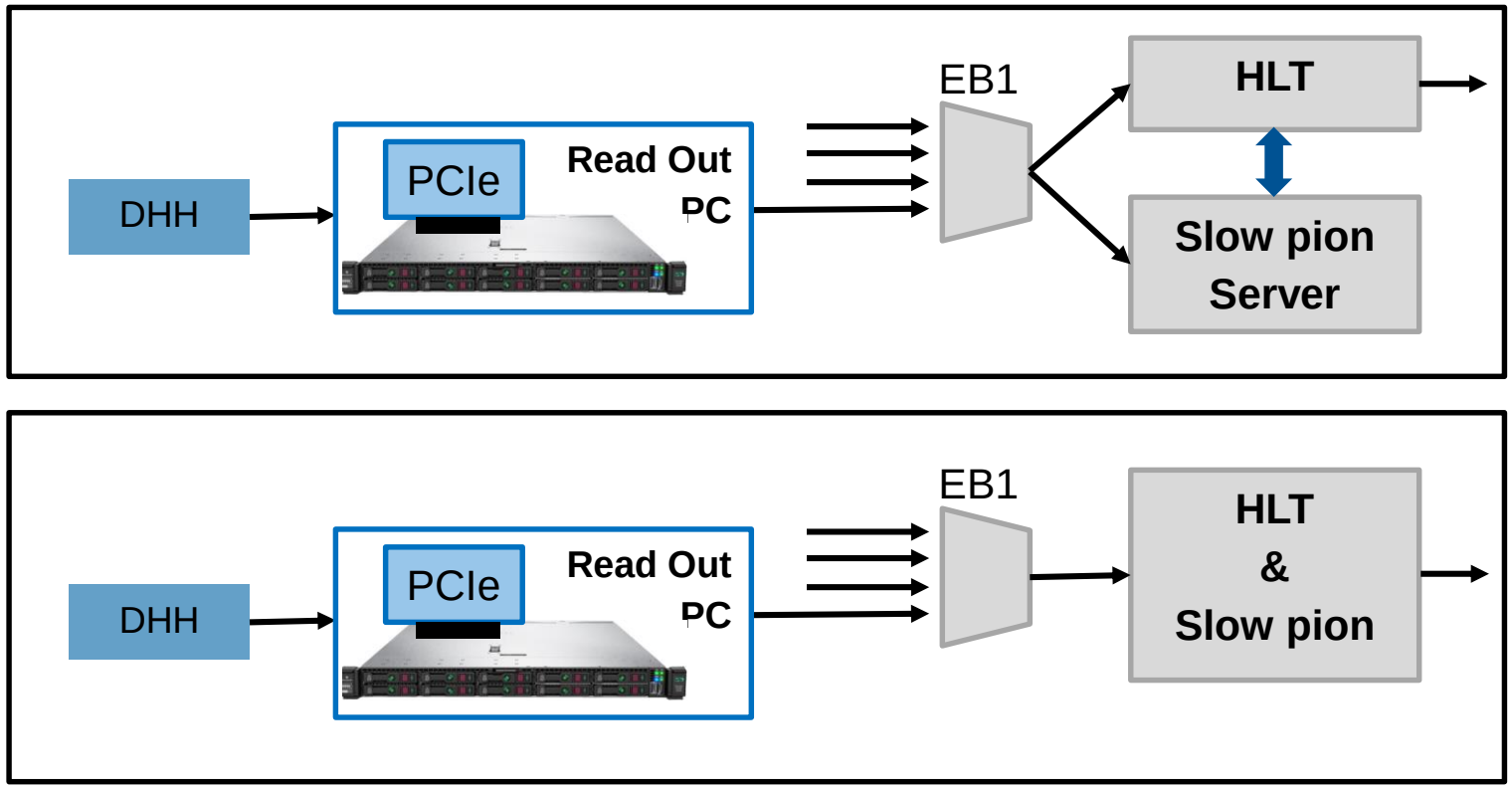
Slow Pion Server

- 256 GB RAM to buffer PXD data
- 10/25 GEthernet
- BASF2 tracking optimized for fast reconstruction

Advantage :

- Overcome ONSEN memory size limit
- Standard data flow

Data Flow IV



Advantage :

- Overcome limited memory in ONSEN
- Standard data flow and data processing infrastructure
- **No EB2**
- If PXD collaboration and DAQ group approves it can be considered for PXD2 installation **wo slow pion track reconstruction**

Disadvantage :

- Higher data rate
- PXD latency to be compensated

Advantage for both : overcome limited ONSEN memory size and allow to extend HLT processing time

HARDWARE

FPGA Card for Clustering

PCIE Card from Alpha-Data

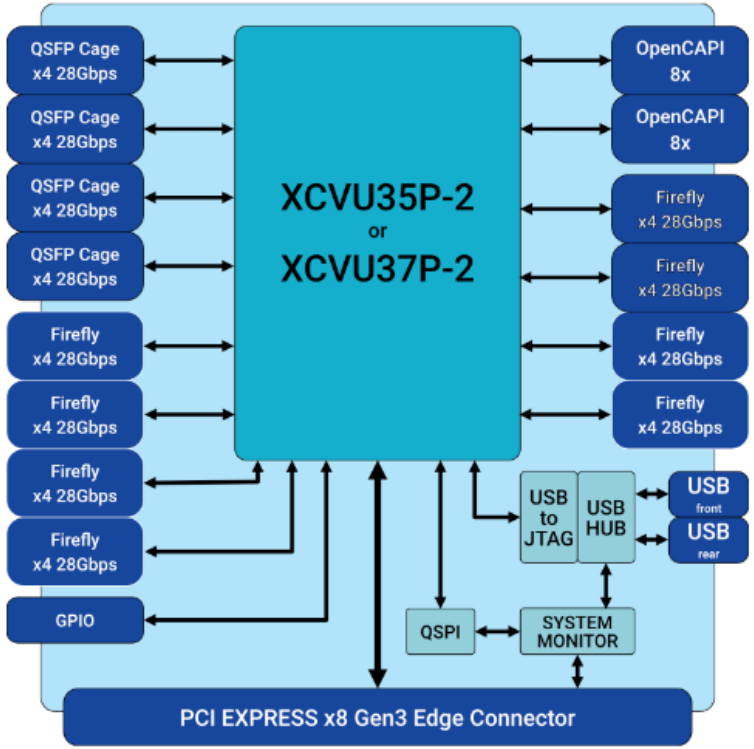
- XCV35P-2/XCV37P-2
- 48/64 high speed links 16-28 Gbps
- 2x 4GB HBM Gen2 memory (32 AXI Ports provide 460GB/s Access Bandwidth)
- 6x PCI Express x16 Gen3 / x8 Gen 4 cores (CCIX Capable)
  - To be used as additional serial links

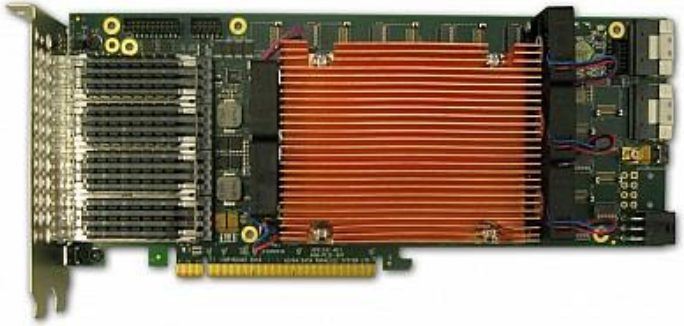
XCV37P vs Virtex6-130T

- LUT 1300k/75k = ~20
- FF 2600/160k = ~16
- Speed gain 400MHz vs 200MHz => 2

} ~36 times bigger

- One card will be sufficient for full PXD clustering and event building
- Will be available for tests in December



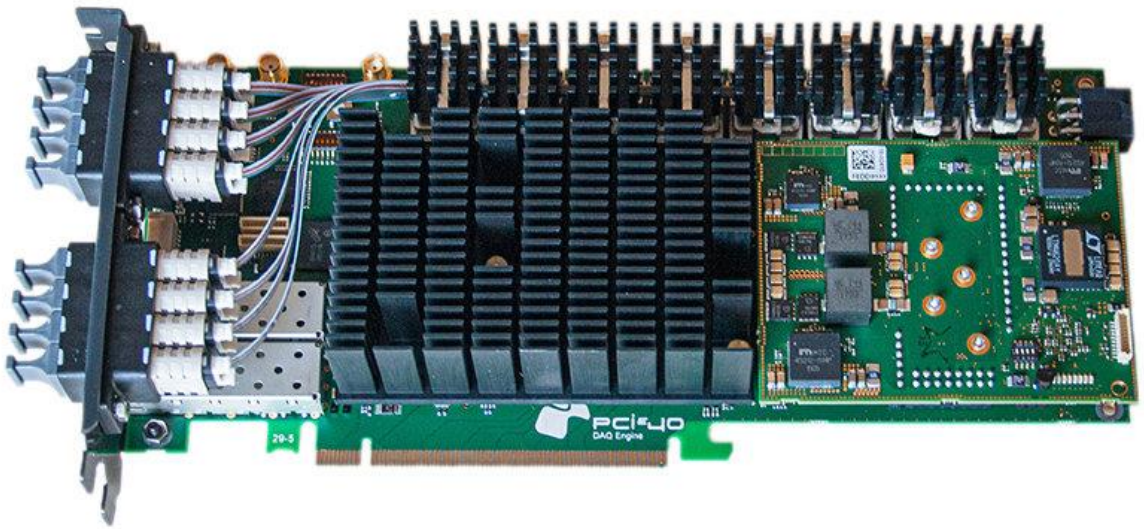


Igor Konorov

PCIE40 for PC Interface

PCIE40 Interface to PC

- 8 links@10Gbps from clustering FPGA card
- Serial interface type to be discussed
- 10 GB/s DMA performance
- Unified Belle2 readout



Summary and conclusions

- Four schemes to upgrade of PXD read out for further integration of slow pion track reconstruction
- Most promising scenario is to include PXD data in EB1
- Hardware is available and feasible for first step of integration
- Next step : evaluate presented scenarios with PXD and DAQ groups

THANK YOU

SPARE SLIDES

DHH Data Splitter

DHC
- 2x2 links @6.5 Gbps

ONSEN
- 2x4 links @6.5 Gbps

Clustering FPGA
- 4 links @6.5 Gbps