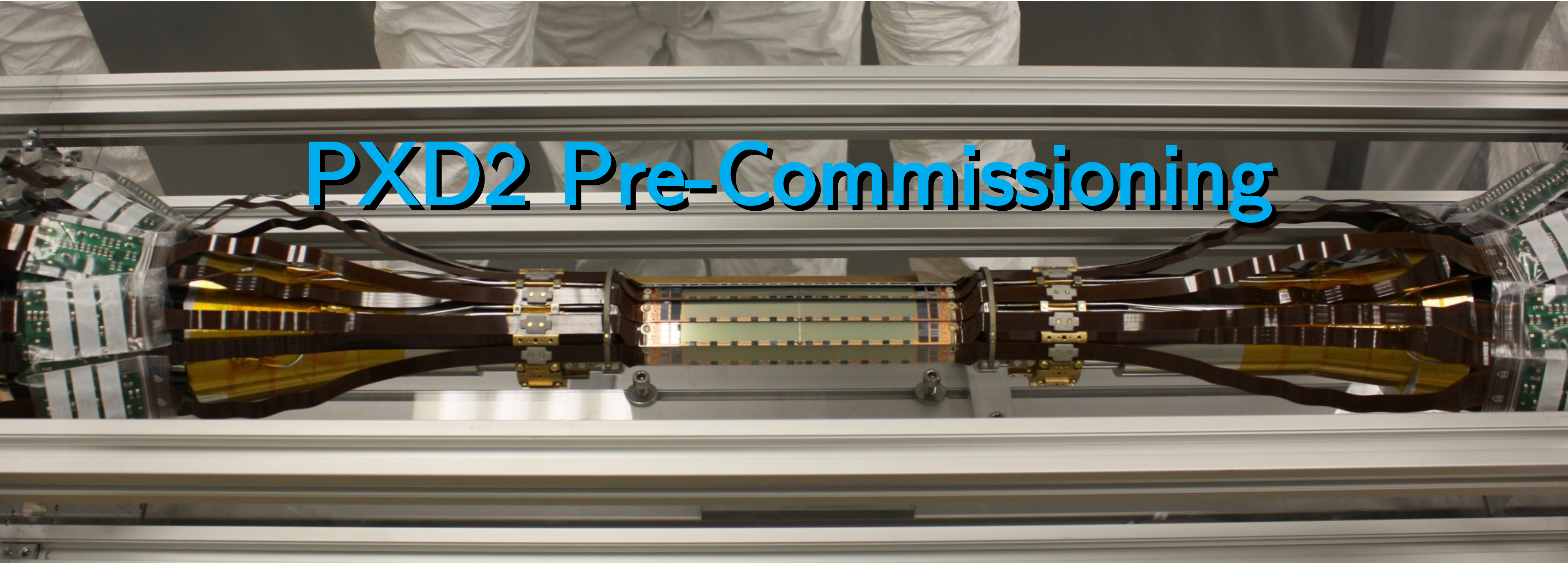
PXD2 Pre-Commissioning



Anselm Baur (DESY)

Belle II Germany Meeting, Munich, Sept. 20th 2022

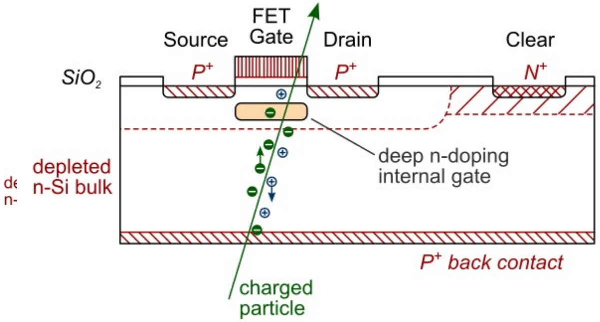
DEPFET

DEPFET Working Principle

- **p-channel** MOS**FET** sits on top of a fully **depleted Si bulk**
- **Internal gate** below FET gate
- Free **electrons drift** to internal gate → O(ns)
- Internal gate charge **amplifies source-drain current**

$$g_q = \frac{\partial I}{\partial q} \approx 500 \, \frac{\text{pA}}{e^-}$$

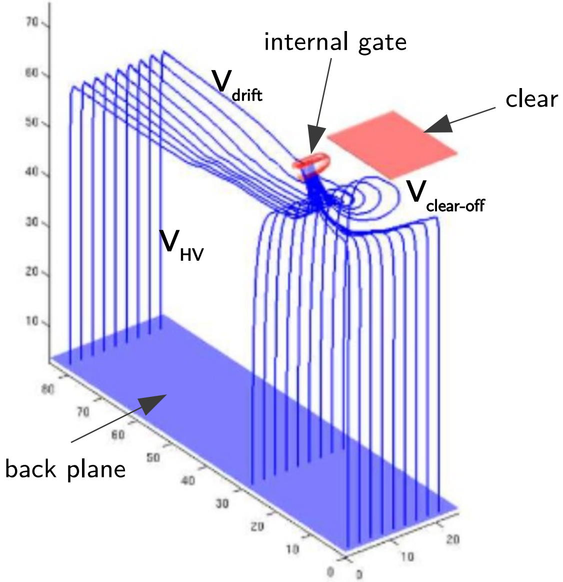
- **Clear mechanism** to empty internal gate



Source: *https://doi.org/10.1016/S0168-9002(03)01802-3*

Operating DEPFET

- DEPFET sensor biasing: **11 voltages** with complex cross-dependencies
- Voltages **dominant impact** on charge collection:
  V_{HV}, V_{drift}, and $V_{clear\text{-}off}$



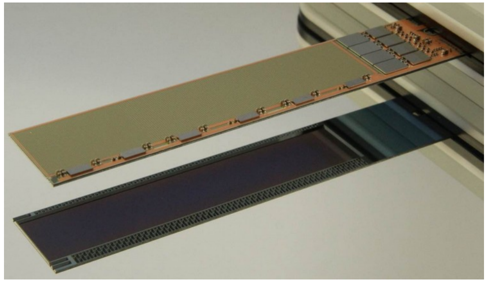
Characteristics

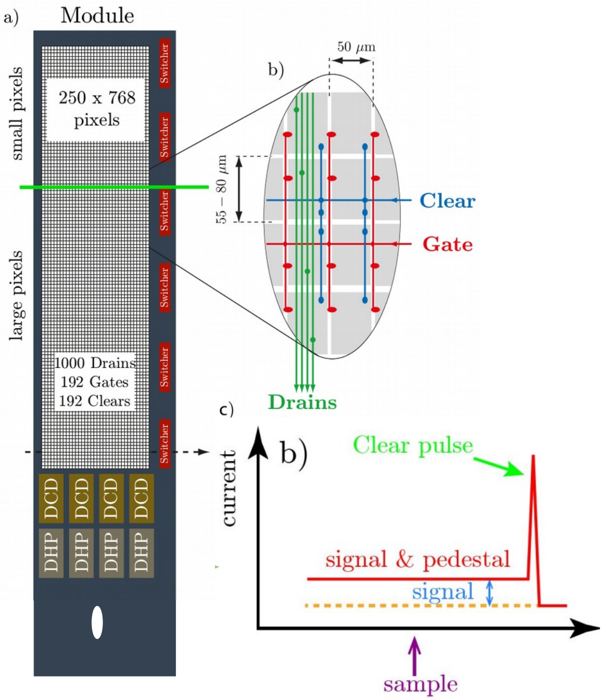
- High **signal/noise ratio** (low internal capacities)
- **Charge storage** → can be read out at any time
- **Thin** sensor (75 µm)
- Low **material budget**
  → ideal for low momentum measurements
  (< 2GeV, Coulomb (multi-) scattering dominant contribution)

PXD Modules and PXD Ladders

Module Properties:

- **250 x 768** (192 000) **pixels** per module
- **50 x 55-85 μm²** (varies in z-direction)
- **Whole module** consists self supporting **Si**
- 4 types of modules **inner**-, **outer**-, -**forward**, -**backward**
- **Readout** and **control ASICs** at end of sensor area and on the balcony



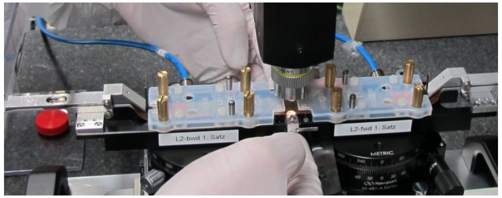


Module Readout:

- **Switcher**: initiates **readout** and **clear** of **4 rows** simultaneously
- **Drain current digitizer** (DCD): converts analog drain currents in digital values **[0, 256] ADU**
- **Data handling processor** (DHP): DCD/Switcher configuration, and triggered readout
- **Zero suppressed readout out** on DHP: hit when **signal** > **pedestal** + **threshold**
- **Readout cycle: 20 μs** in rolling shutter mode

PXD Ladder:

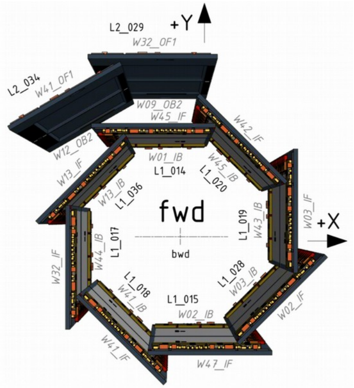
- Forward and backward **module glued together** at short end to a **ladder**

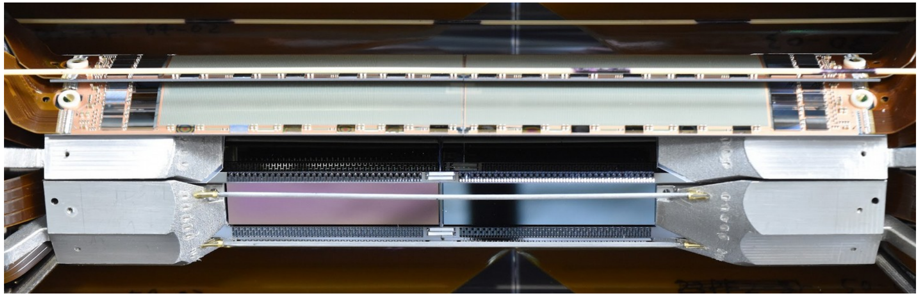


PXD1

PXD1:

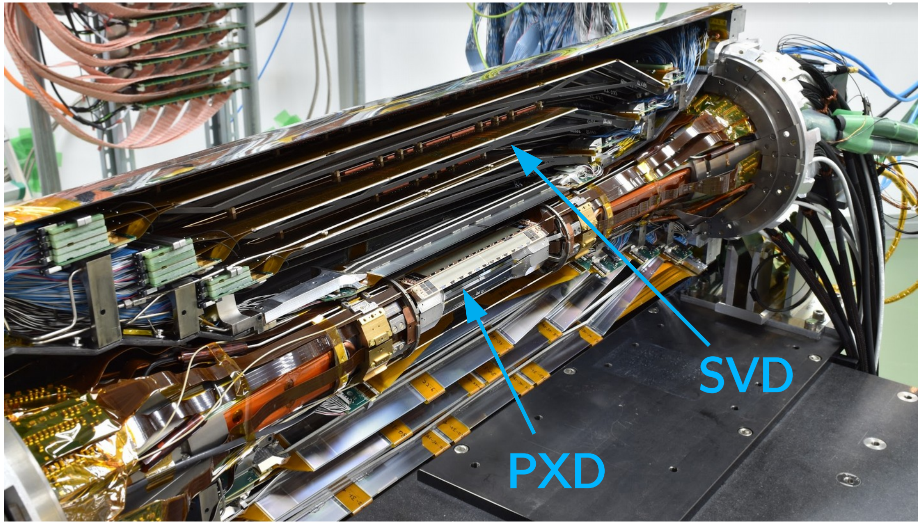
- **Was installed** 2018 – 2022 in Belle II at KEK
- **Layer 1: 15/16** modules working
- **Layer 2:** equipped with **2 ladders** covering dead L1 module





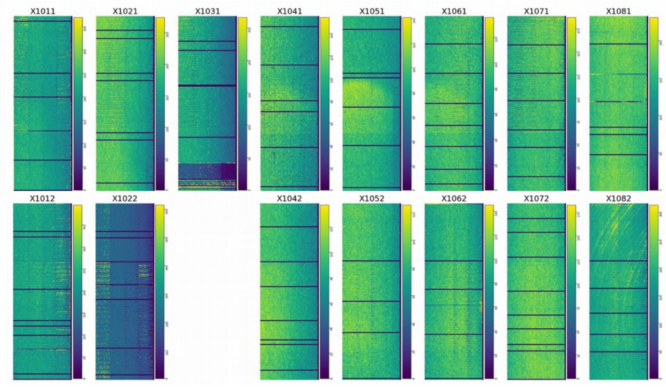
Belle II Vertex Detector:

- **PXD**: 2 layers, **SVD**: 4 layers
- **Mounted** on a 2 layer Be **beam pipe**

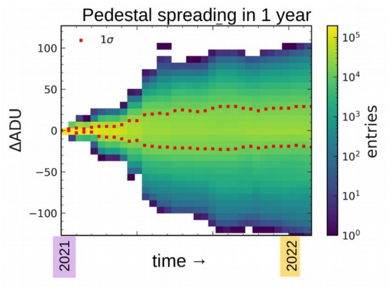


PXD1 Aging:

- Suffered from **high instantaneous radiation doses**
  - ~ 150 dead gates, 1 unstable switcher region
- **Pedestal aging** already visible (pedestal currents drifting apart)
- **Regions** with **lower efficiencies** appear → pedestal compression, DCD gain



Exp: 26; Run: 1968 (latest physics run before LS)



M. Konstantinova

Advantage of Completed 2 Layer PXD

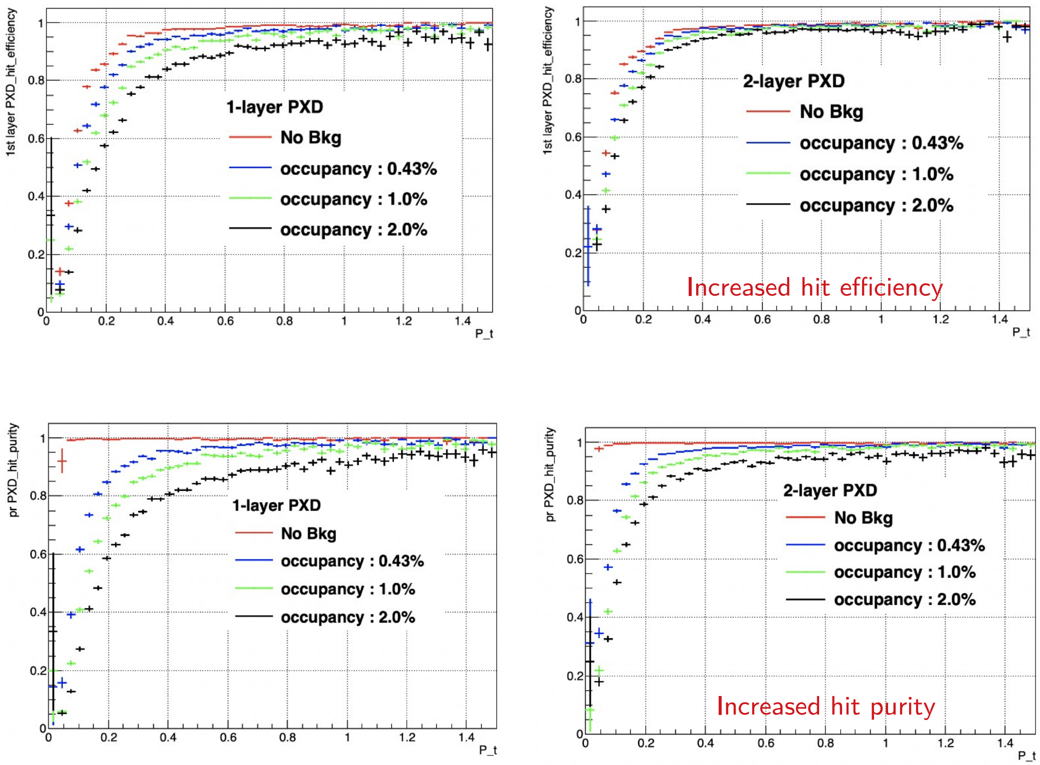
MC Studies:

- 10k **BBbar** events
- Detector simulation with **2 PXD layers**
- **Track reconstruction** using standard tracking chain
- **Figures of Merit**
  - Fraction of MC hits found in the reconstructed track

$$\boxed{\text{hit efficiency} = \frac{\mathrm{N_{mc\_hits\_in\_reco\_track}}}{\mathrm{N_{hits,mc\_track}}}}$$

  - Fraction of MC hits in the reconstructed track hits (how much background was picked up?)

$$\boxed{\text{hit purity} = \frac{\mathrm{N_{mc\_hits\_in\_reco\_track}}}{\mathrm{N_{hits,reco\_track}}}}$$



Yubo Han, Feb. 15th 2022

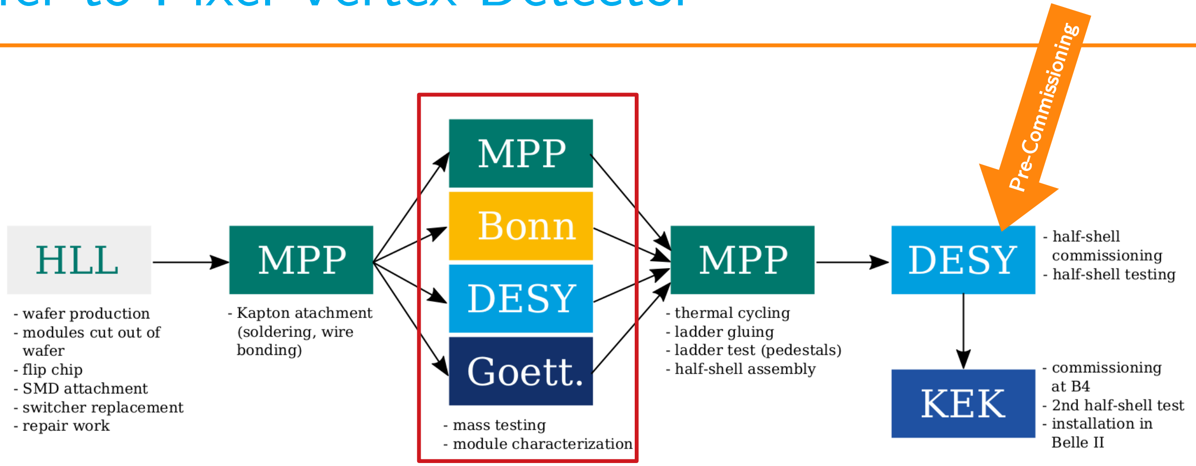
2 Layer PXD:

- **higher probability** to **select correct PXD hits** in 1st PXD layer **at higher background** levels
- No direct influence on impact parameters in x-y (L1 highest impact)

From Wafer to Pixel Vertex Detector

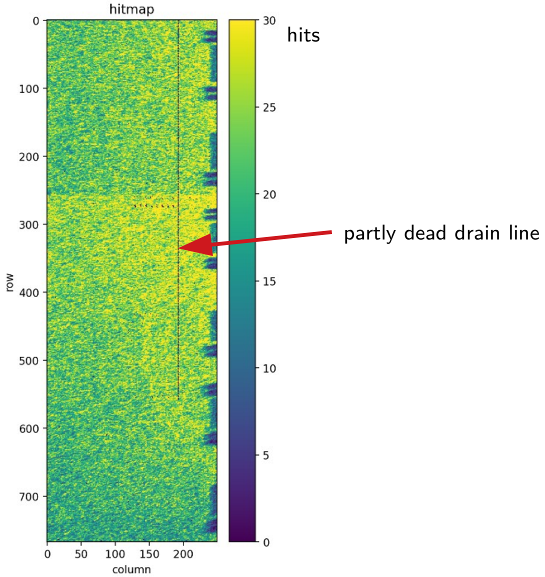
Steps:

- Modules are **built** at HLL and MPP
- **Tests/characterization** at several test sites
- **Ladder gluing** an **Half-shell assembly** at MPP
- **Pre-commissioning** at DESY
- **Final Commissioning** at KEK



Module Testing and Characterization (Mass-Testing):

- **First power up** of the module
- Checking **functionality** of **pixel matrix**
- Determining **operation parameters**
- Tuning of the **analog/digital converter**
- Optimizing **pedestal compression**
- Maximize **charge collection** and optimize **homogeneous pixel response**



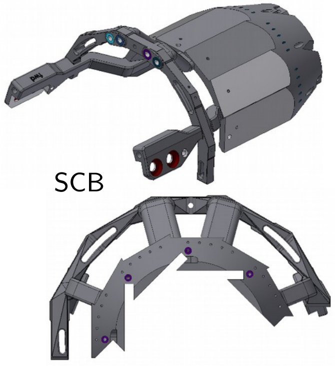
Grading of Modules:

- During 4 years of testing, **scans** and **parameters adjusted** over time
- Preliminary **grading proposal** was **never applied** to **all tested modules**
- **Working point** optimization not uniform
- **Number** of **working pixels** as strongest FOM

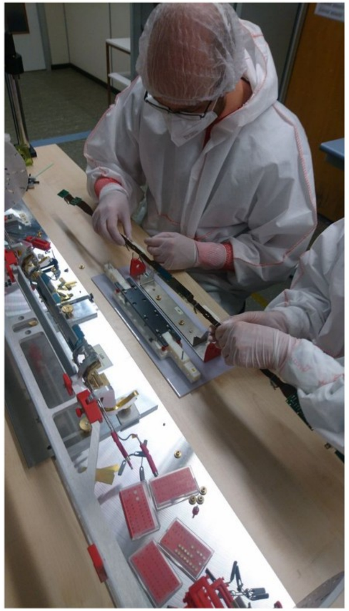
PXD2 Half-Shell Assembly at MPP

Ladder Mounting

- Aligned **Support Cooling Blocks** (SCBs) **held by** a **rotation device**
- **Mylar foil** between SCB and ladder
  → electrical isolation
- **Carbon tubes** installed in between SCBs (fixed on one side)
- **Ladder by ladder mounted** on the SCBs
- First **4 inner layer** (L1) ladders, then **6 outer layer** (L2) ladders

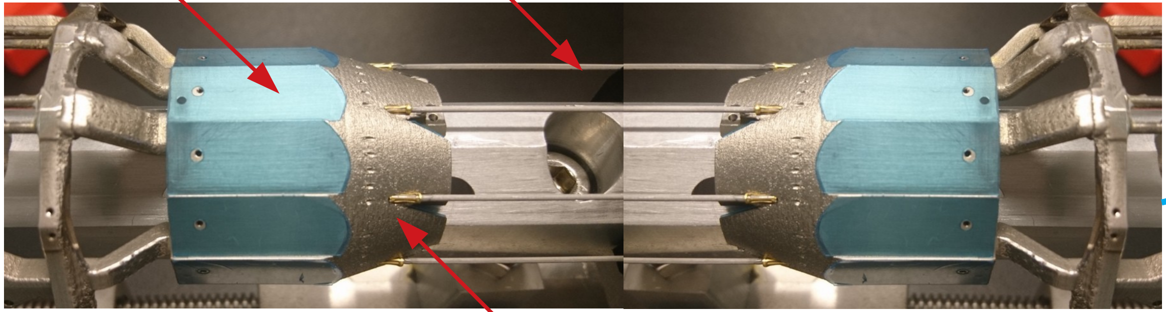


SCB

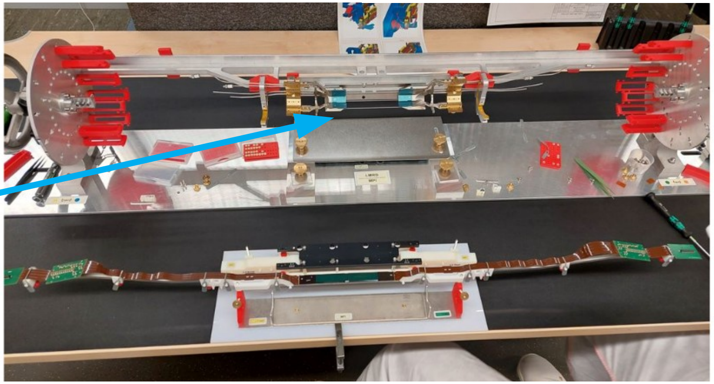


Electrical isolating foil

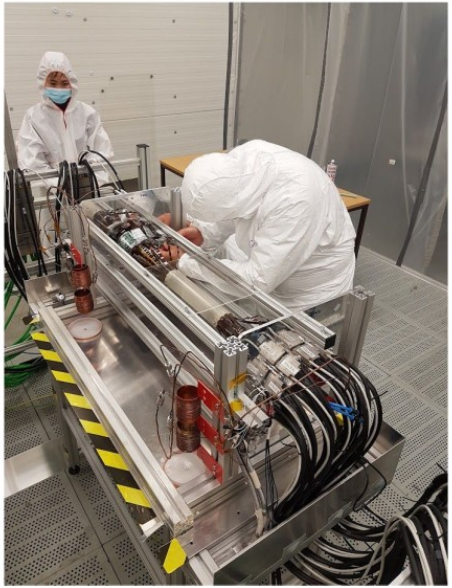
Carbon Tube (N2 Cooling)



SCB



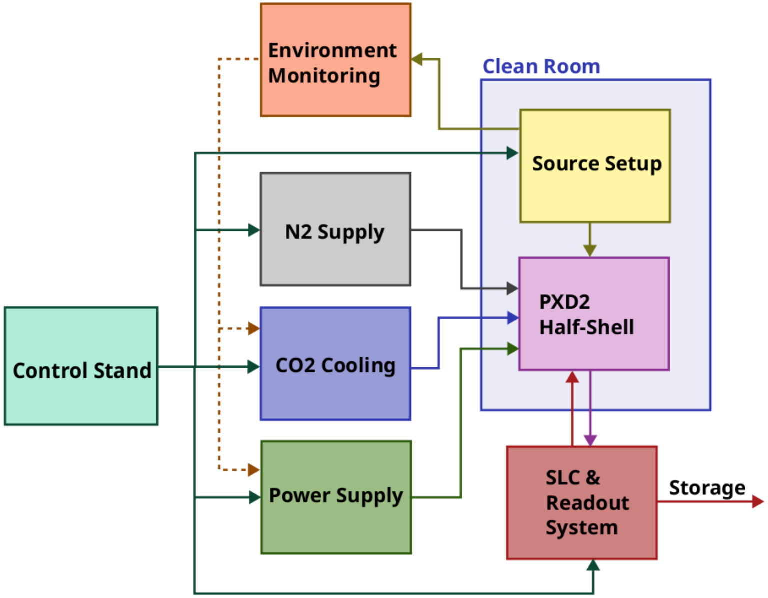
1st PXD2 Half-Shell at DESY



Half-Shell Test Stand at DESY

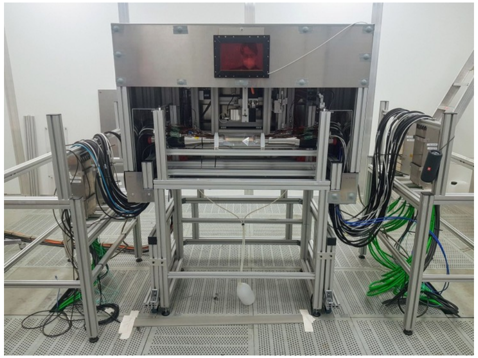
Test Setup:

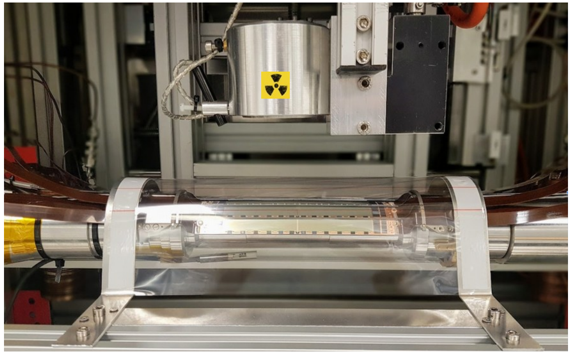
- Full **DAQ readout chain** to operate modules
- **CO2 cooling** of the HS in a monitored low humidity volume
  - HS power consumption: 190 W (~9 W/module)
  - CO2 temperature: 0 – 15 °C (KEK -20°C)
- **N2**: matrix cooling and dry volume
- Half-Shell operation **limited by number of available power supplies** → operate ½ HS at once



Tests and Measurements:

- Full **electrical test** if all **ladders** still **functional** after mounting
- **Source measurements** using Sr90 source new
  - Pixel hit efficiency, noise, …
  - Examining cross-talk between modules
  - Crosscheck performance with mass-testing results
- **Stress-tests**: undergo several cooling cycles and thermal states with the half-shell





1^{st} Half-Shell

Status:

- All 20 modules **fully functional**
- **Basic-calibrations** and **source scan** finished
- Discovered **2 broken ladders** (later more!)

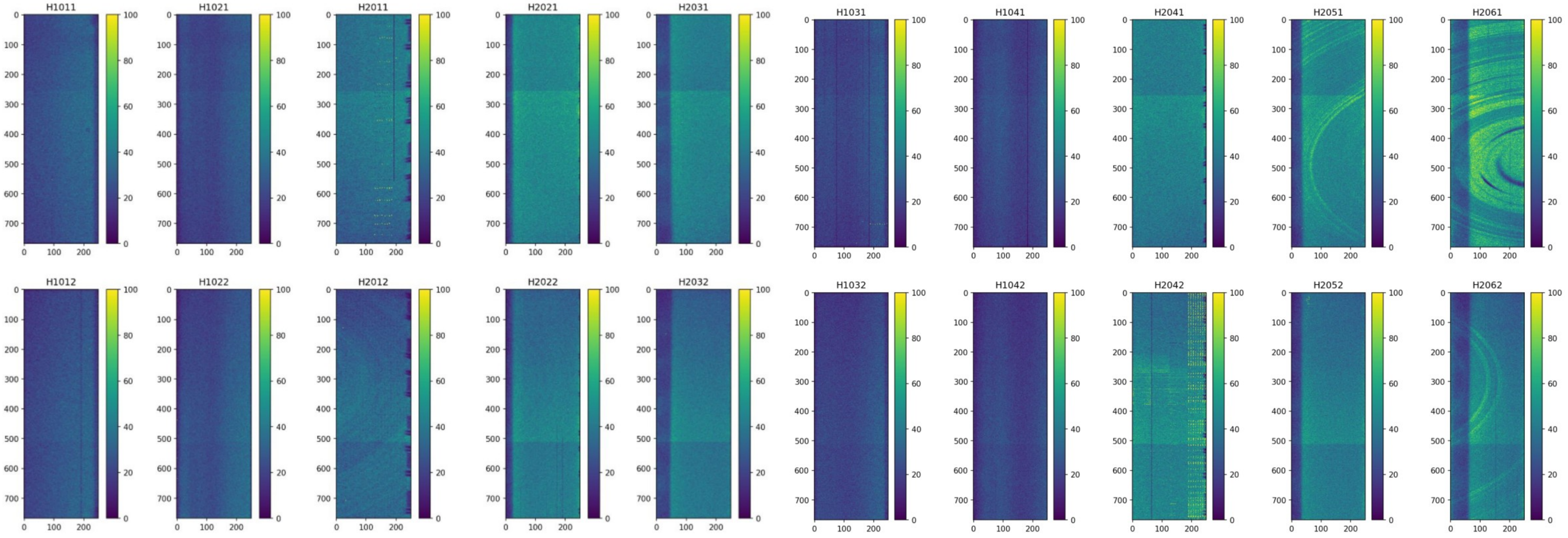
Source Scan:

- **Optimize** DEPFET **biasing voltages** for maximal charge collection
- Scan 204 voltage settings

Measurement

- **HV**: -48V $\rightarrow$ -72V
- **Drift**: -3V $\rightarrow$ -6V
- **Clear-off**: 2V $\rightarrow$ 4V
- 15 min measurements

Sr90 hitmaps (re-measure hit efficiencies, tune working point)



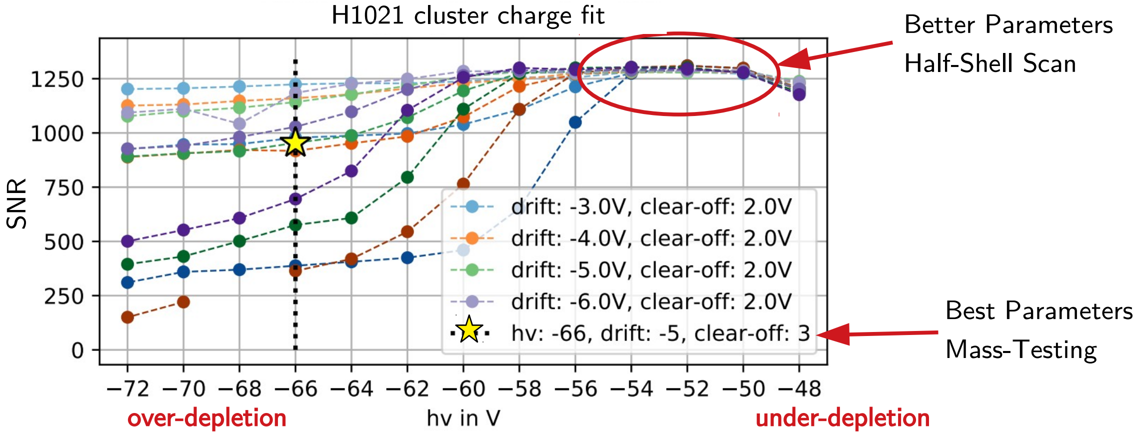
Source Scan Analysis

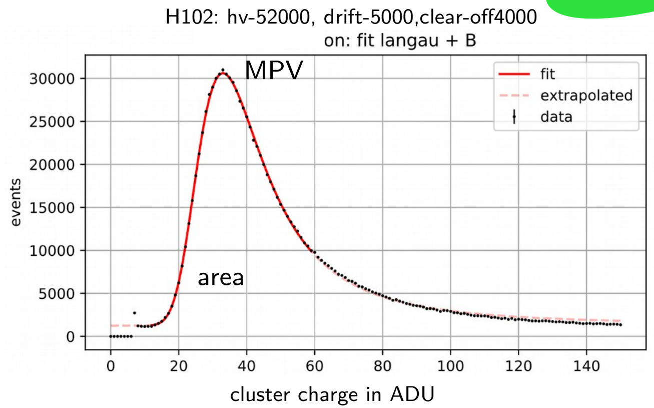
Work in Progress

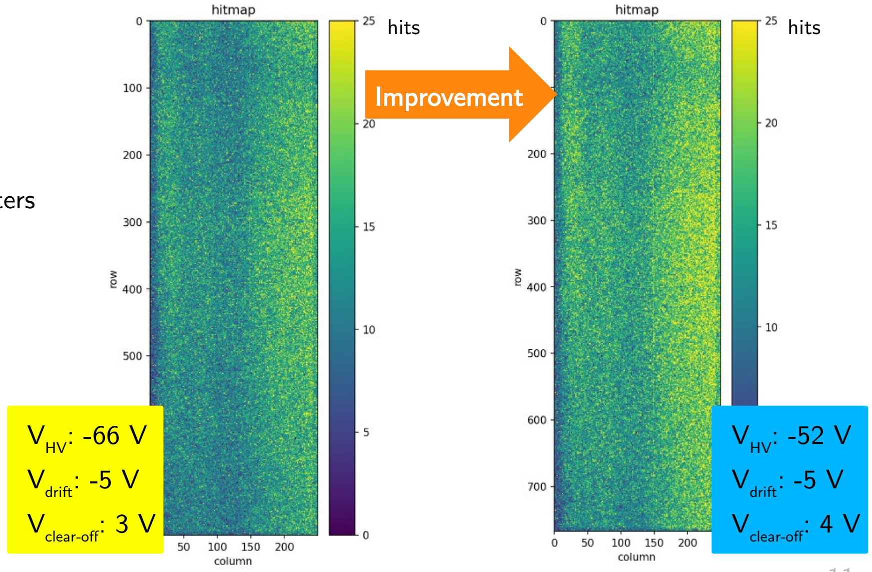
Fitting Cluster Charge Distribution:

- **LanGau Fit** (Landau convoluted with Gaussian read-out noise)
- Defining **Figure of Merit**:

$$SNR = \frac{\text{MPV}}{\text{noise}_{\text{pedestal}}} \cdot \frac{\text{area}}{1000}$$







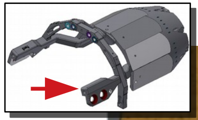
Conclusion:

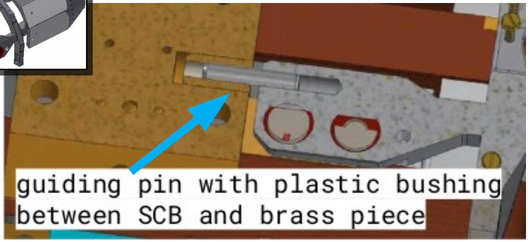
- Optimal **parameters** determined during **mass-testing partially not optimal** for several modules

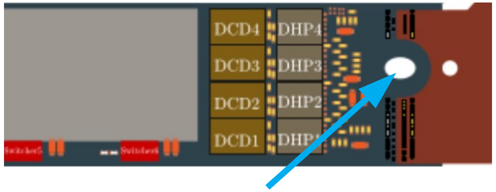
Damage on 1st Half-Shell

Half-Shells Designed to Cope With Thermal Stress:

- Forward SCB not fixed on BP $\rightarrow$ **guiding/sliding pins**
- Forward modules have **elongated hole**



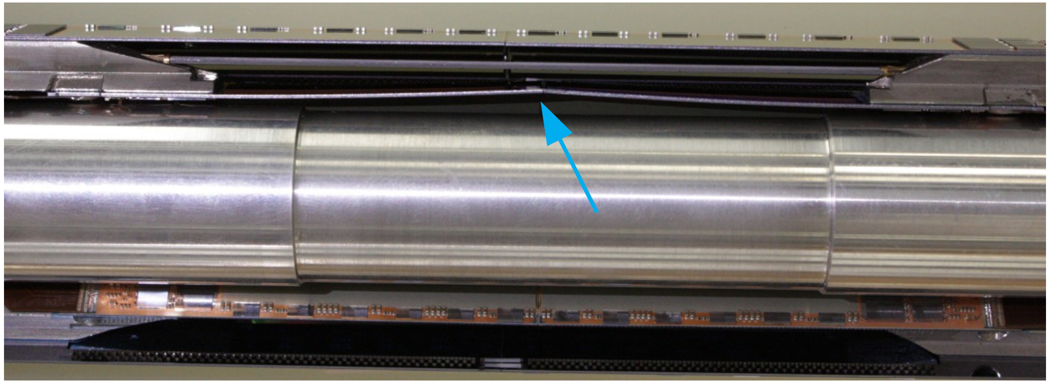




elongated hole which allows
ladder to move longitudinal

After Testing 1st Half-Shell:

- **2 broken inner ladders** L1a, L1b
- **Kink height** of ~**1.5 mm**
  - Equivalent thermal expansion of Si at ~140 K (this we did not have)
  - Ladder were still under tension, relaxed when releasing screws
- **Outer ladders not affected**
- **Unclear** if L1a and L1b **still functional**



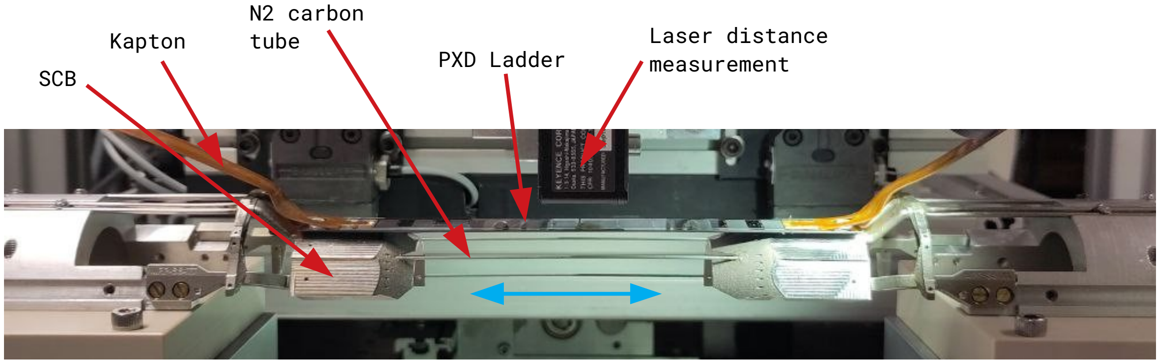
Possible Causes (Combination?):

- S.th. **prevented SCB from gliding** under thermal/mechanical stress
- Ladder **tightening torque** too high $\rightarrow$ **no module gliding**
- Explanation of large kink, an **asymmetric** process must have **periodically** enhanced stress $\rightarrow$ **accumulated bending**
- Influence of massive **Al beam pipe mockup**
  (Al ~10 times higher thermal expansion than Si)
- **Glue looses strength** at ~**60 °C** under stress (tests at MPP)
- Incident: once **CO2 cooling broke down** in forward SCB
  (ASIC temperatures up to 80-90 °C for a few seconds)

How to Continue

Further Program:

- 2nd HS **pre-commissioning on hold**
- **Mechanical tests** ongoing/in preparation:
  - screw tightening torque → ladder gliding
  - SCB mechanical gliding
  - thermal conduction depending on tightening torque
  - influence Al dummy beam pipe
- **Consultation** of retired expert from MPP (PXD mechanical design)



Repair 1st Half-Shell:

- **2 good** L1 ladders for replacement
- **1 more** L1 ladder can be **glued** from good modules
- **Risk analysis**

→

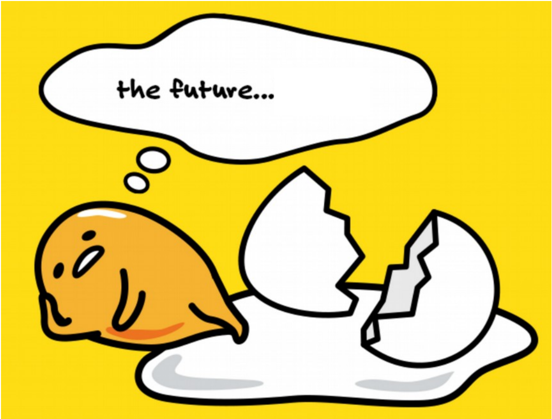
Impact on Time Schedule:

- How fast/easy we can **repair/modify 1st HS**
- How fast/easy we can **apply modification to 2nd HS**
- **Fact: we miss the estimated October target!**
- **Target: PXD2 commissioning during LS1**

Summary

PXD1:

- Served us well over 4 years: **high precision, good efficiency**
- **Aging** already **visible**
- **2nd PXD layer:**
  - Will **increase** the **hit efficiency** and **hit purity** for **higher background levels** for low momentum particles in layer 1
  - Provides **redundancy** in case of **L1 aging**



s.th. like: “don’t give up”

PXD2 Status:

- **Both PXD Half-Shells** assembled
- **Functional tests** and **scans** with **1st HS finished**
  $\rightarrow$ all 20 modules were functional
  $\rightarrow$ source scan analysis ongoing for working point optimization
- 1st HS: **2 broken inner ladders** (L1a, L1b) discovered
- 2nd HS **commissioning** on **hold**
- Large number of **tests ongoing** at MPP, DESY, Bonn

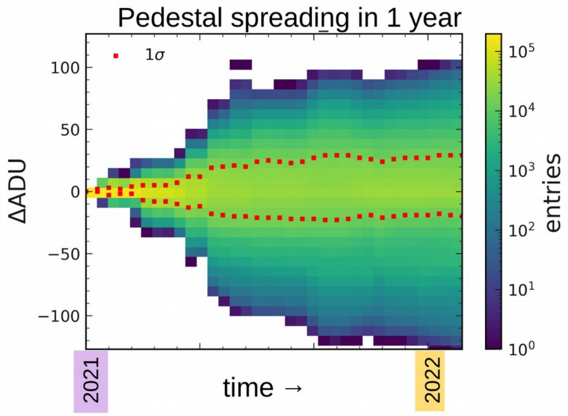
Outlook:

- Find the **cause** of the problems and **solution**
- **Repair** 1st Half-Shell, (and **modify** 2nd Half-Shell)
- **Impact on time schedule $\rightarrow$ to be determined after further studies**

Backup

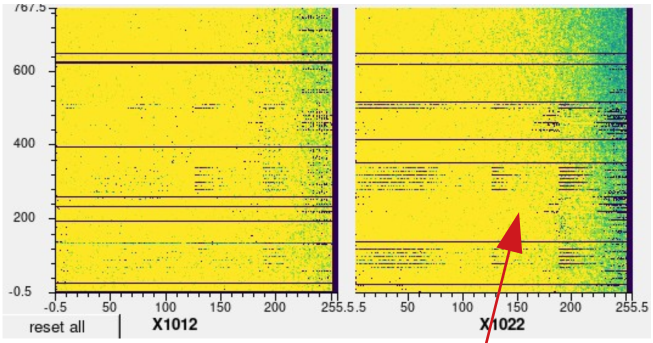
Pedestal Aging

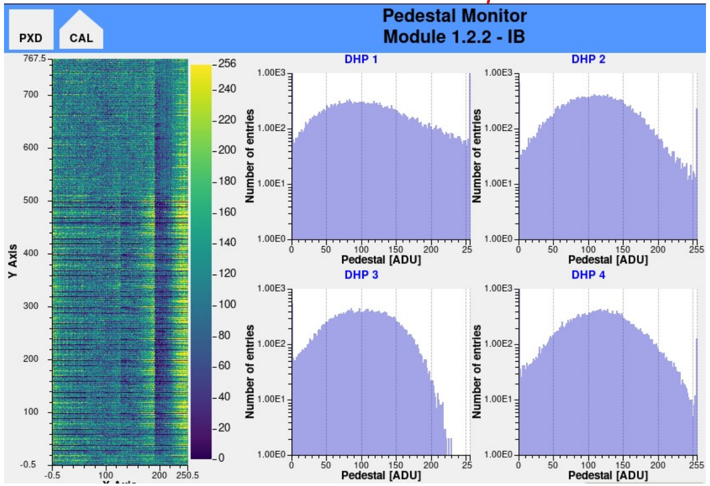
- Pedestals slowly drifting out of dynamic range
- Regions with deteriorated efficiency appear
- Periodic pattern visible



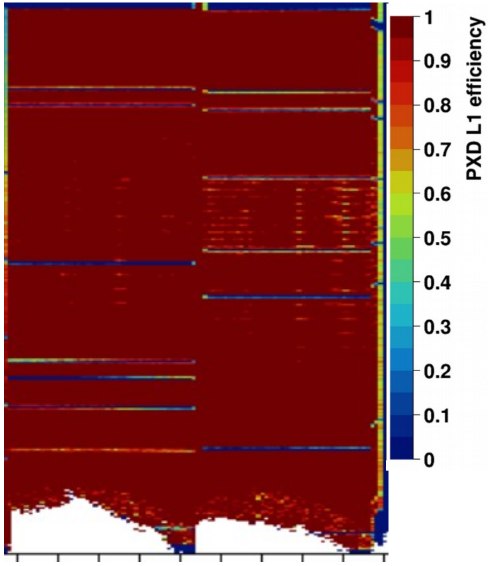
M. Konstantinova

Hitmap



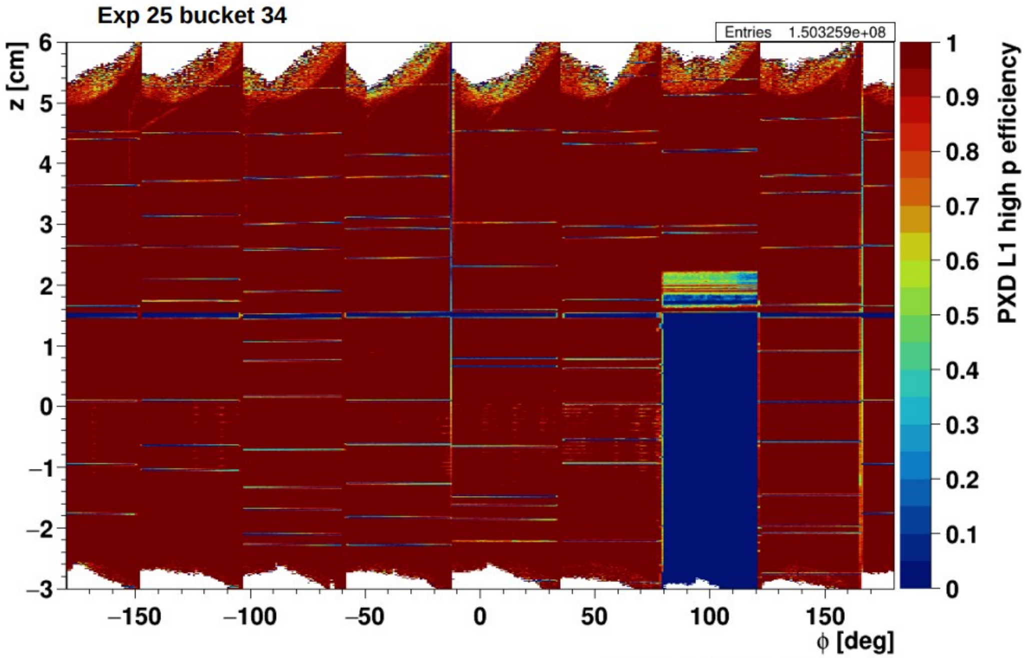


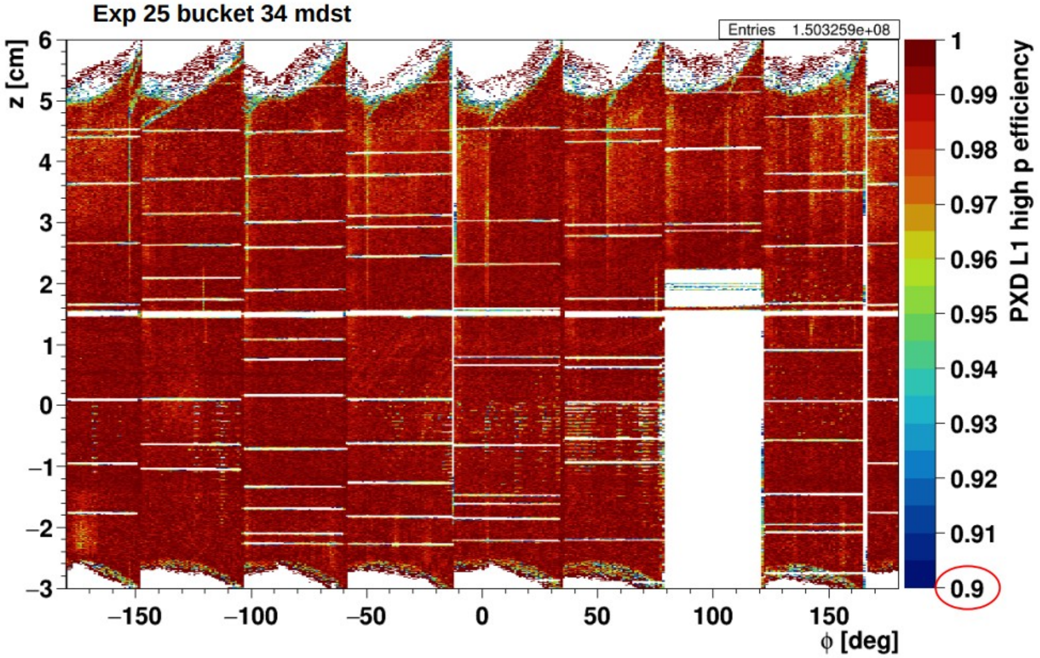
Efficiency Map



D. Pitzl

PXD1 Efficiency May 2022





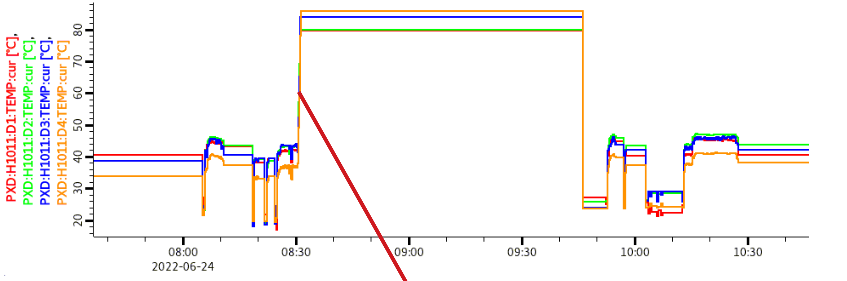
sick switcher in 1.3.1

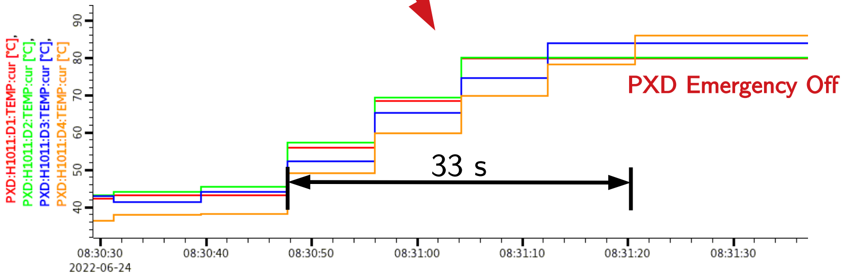
https://indico.belle2.org/event/7369/contributions/38514/attachments/17757/26404/Pitzl-2022-07-eff.pdf

MARCO Cooling Incident

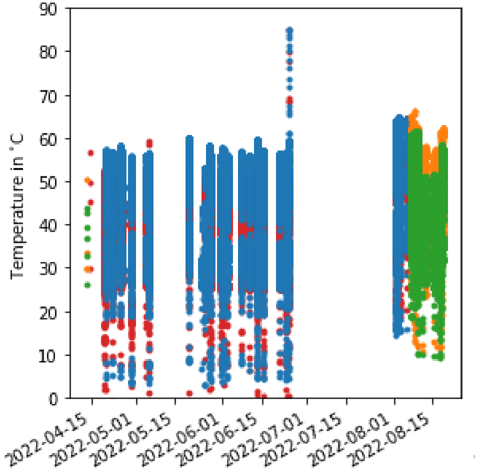
Cooling Incident Friday June 24th:

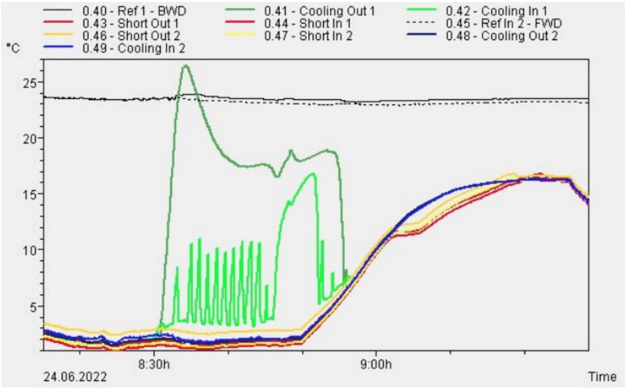
- During operation the CO2 cooling in FWD line broke down
- DHP temperatures increased rapidly
- Modules shut of after approx. 33 s
- Tried to stabilize MARCO
  - Warm up, higher flow
- Afterwards issues to power on modules due to dhp-io voltage to high
  - This anyhow prevent us to power the modules
  - DHI power off did not work
  - Can also be seen when dhp-core voltage is shut down before dhp-io
- Elog: https://elog.belle2.org/elog/PXD-Commissioning-DESY/136





- DHP temperatures of all modules divided by:
  - if, ib
  - of, ob



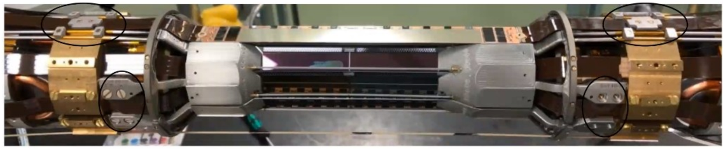


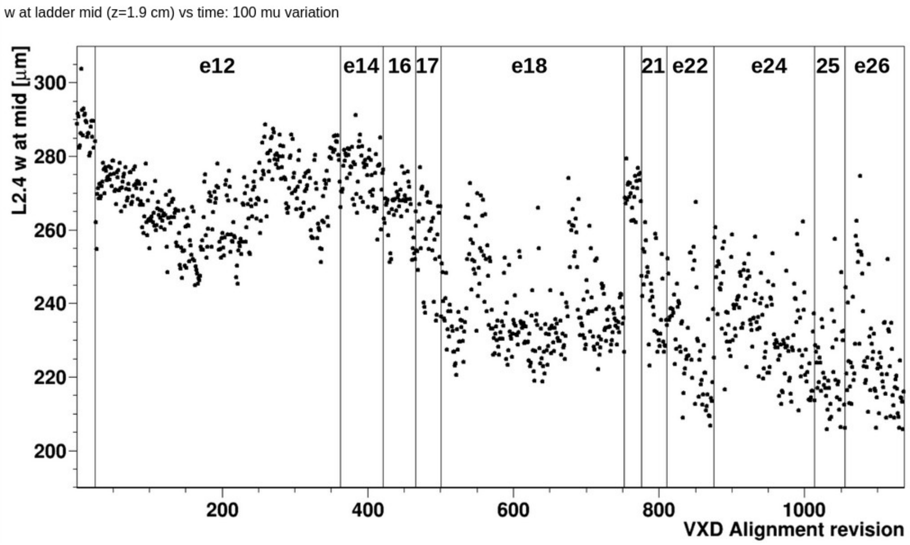
PXD1 SCB Tilt

Beam Pipe Temperature

- Beam currents heat up beam pipe
- Cooling pipes are fixed at SCB
- SCB is tilt by this fixation and the beam pipe extension
-

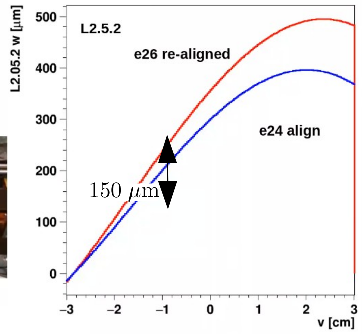
LS1: avoid overconstrained fixations

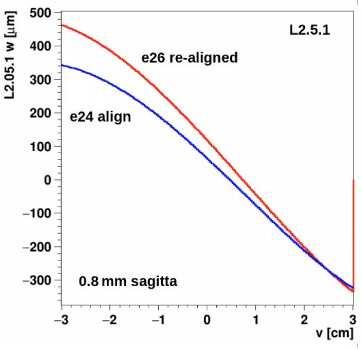




L2.5 alignment

- w = up from sensor surface
  - nominal: w = 0
  - L2.5 already had tilt and bow
- e26 run 1699:
  - extra tilt and shift
  - fixpoints at ends





L2.4 2022 vs 2019

- w = up from sensor surface
  - ideal: $w = 0$
- official hierarchical sensor and ladder alignment
  - proc13 and prompt