Introduction to the ONSEN System and Discussion of ONSEN ROIs

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Belle II Germany Meeting

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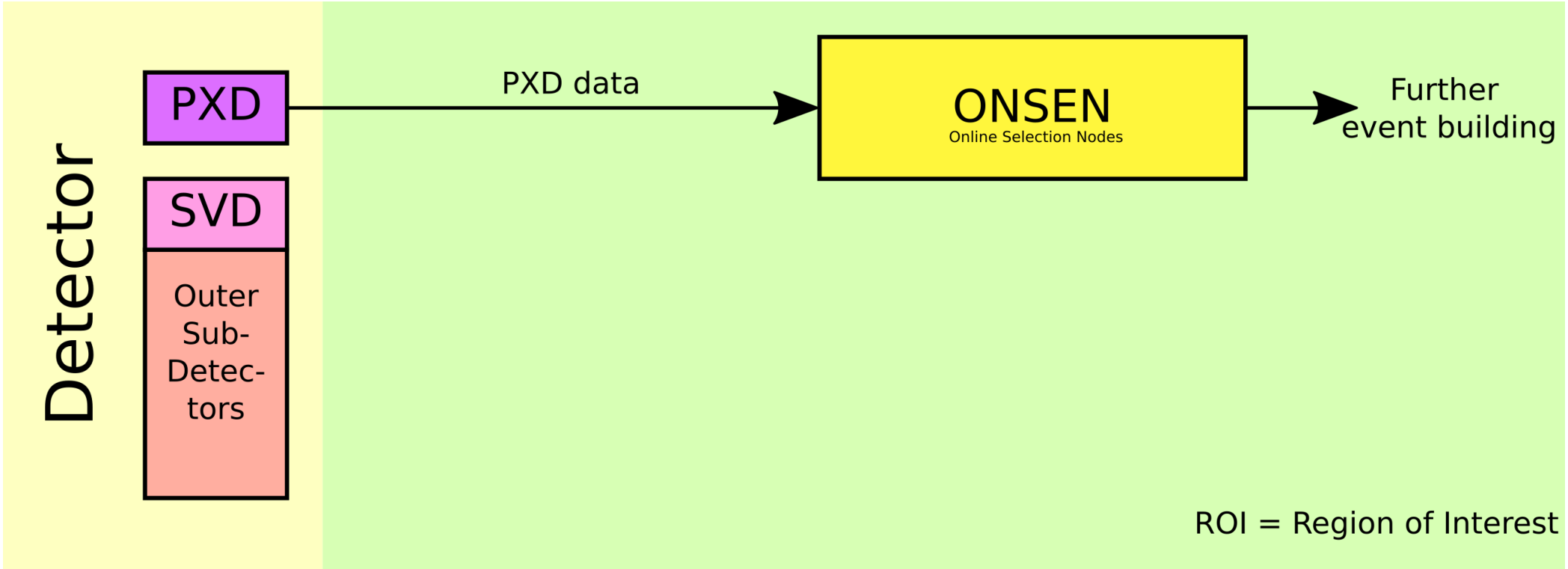
Functionality



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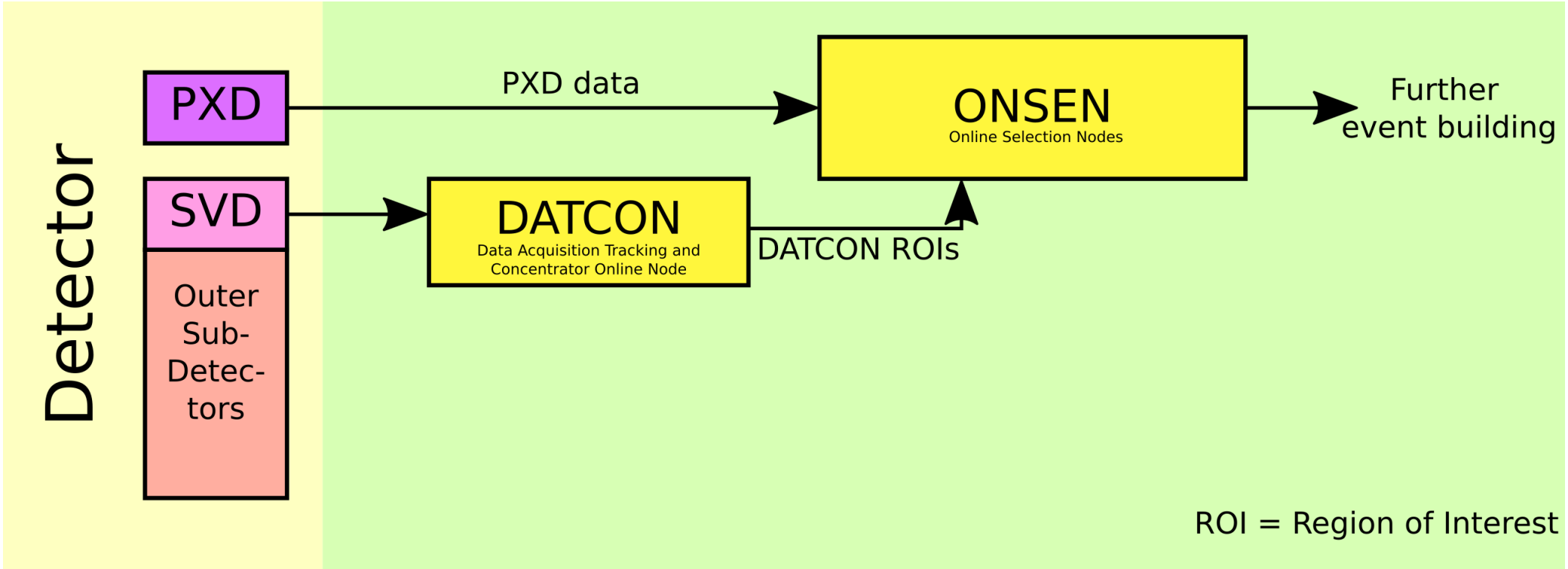

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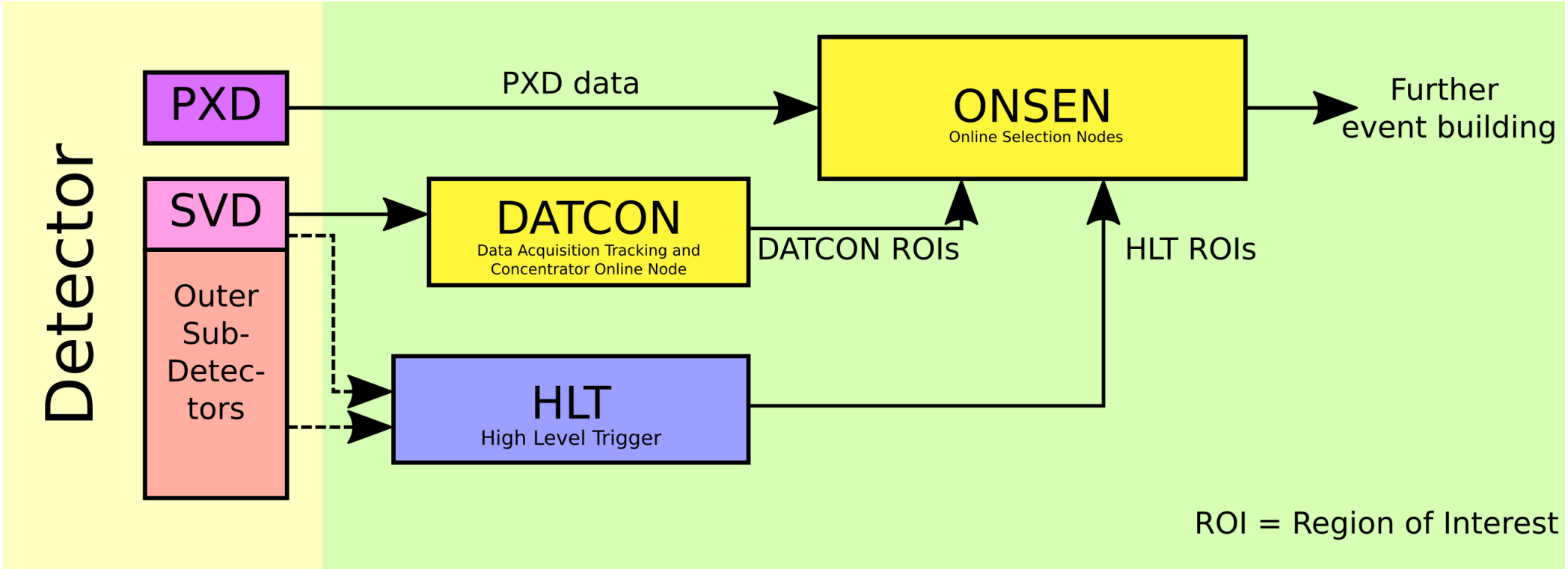

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- Further functionality:
  - Load balancing
  - Calculating occupancy for monitoring
  - Catch data errors (continue running)
  - Coordinate transform
  - Automatic link recovery

Hardware

- Field Programmable Gate Array (FPGA)
  - 1-bit data storage (Flipflops)
  - Logical gates

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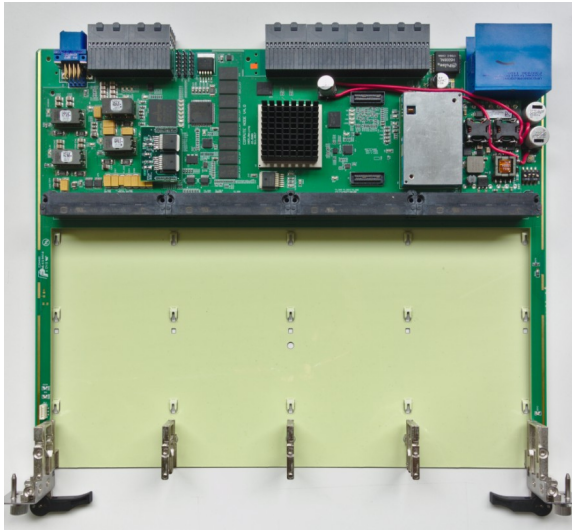

Compute Node Carrier Board (CNCB)

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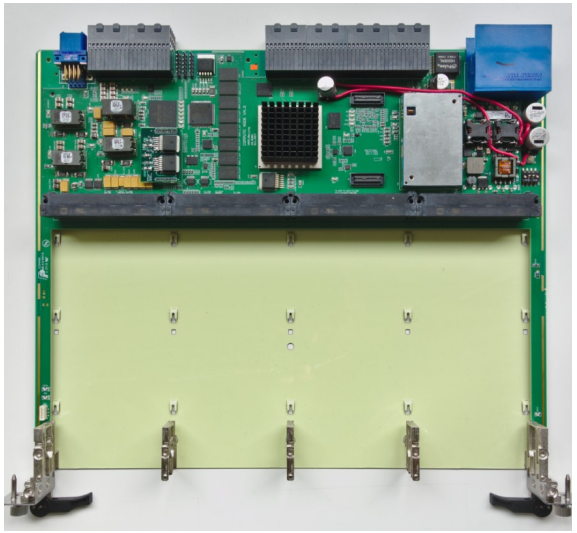
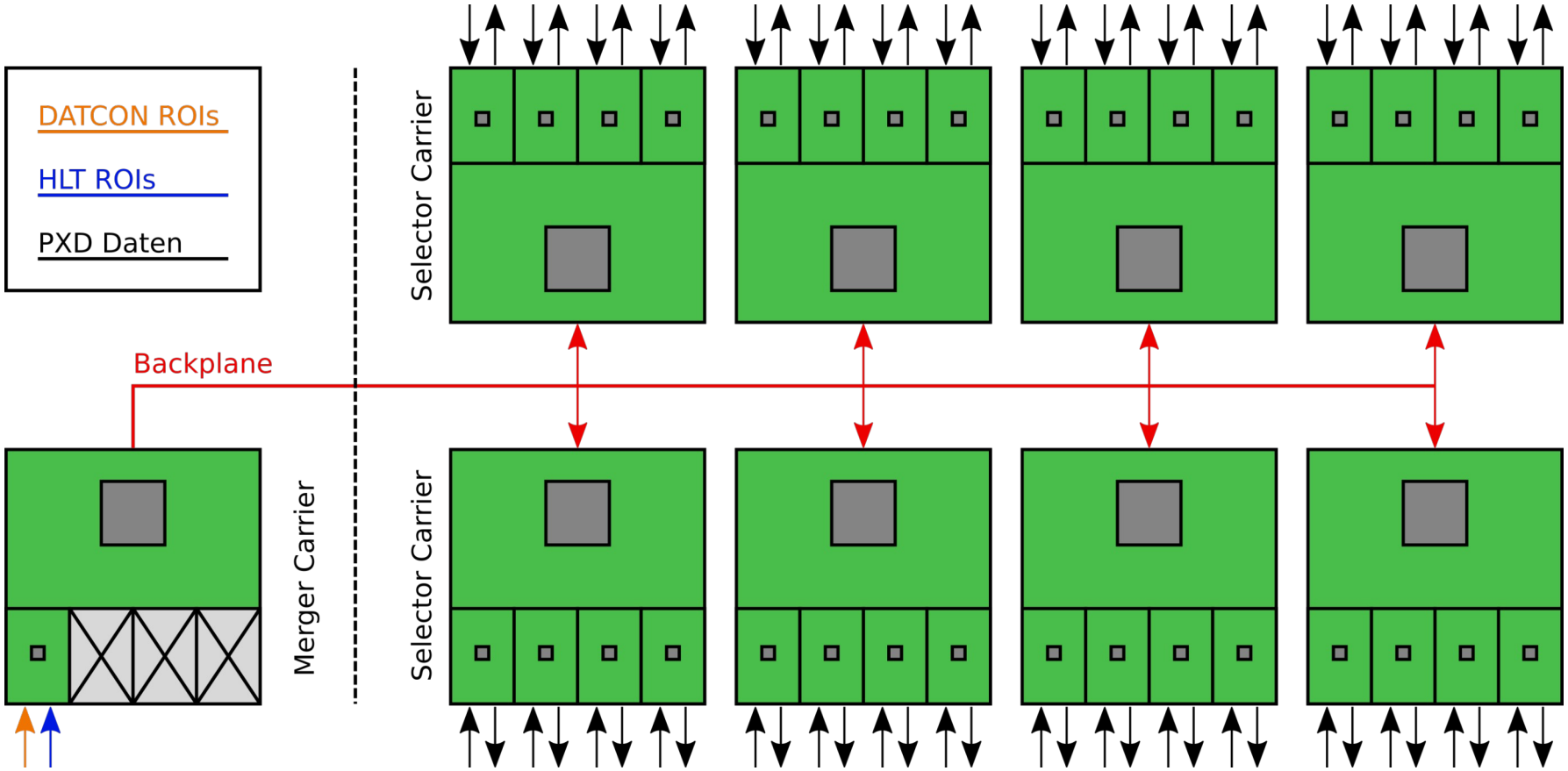


Compute Node Carrier Board (CNCB)

Advanced Telecommunication Computing Architectures (ATCA) Shelf

Hardware Setup



Defective Hardware

- 4 broken AMCs

Name	xFP-V4-2-10
Problem	Shuts down after power up
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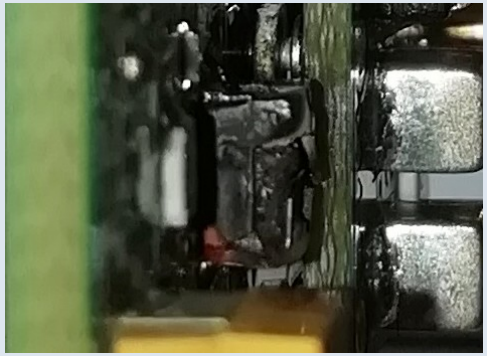
Remark	Voltage to high	Functional with an alternative bitstream	

Defective Hardware

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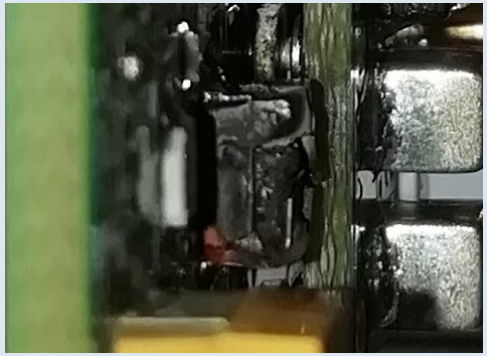
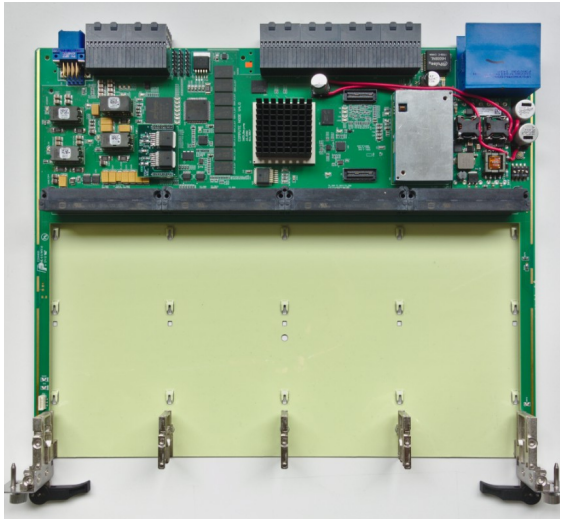
Name	xFP-V4-2-10	xFP-V4-2-34	Unnamed Board	xFP-V4-2-04
Problem	Shuts down after power up	Broken connection to memory	Broken Transistor	Link connection fails
Remark	Voltage to high	Functional with an alternative bitstream		Broken mechanism to hold the transceiver

Merger Carrier Spare Development

- Compute Node Carrier Board (CNCB) v4.0
  - Newer FPGA (Kintex UltraScale) with about 10 times the resources
  - Compatible with current ONSEN setup
  - Two prototype board existing
  - Newer programming environment (Vivado)
  - Faster links (6.125 Gbps → 16.3 Gbps)

CNCB v4.0



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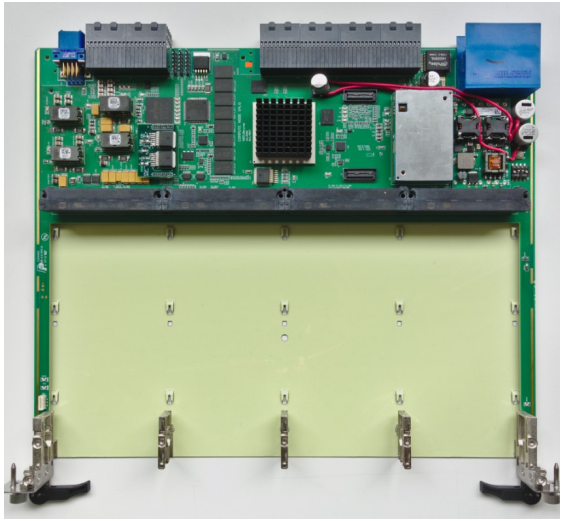

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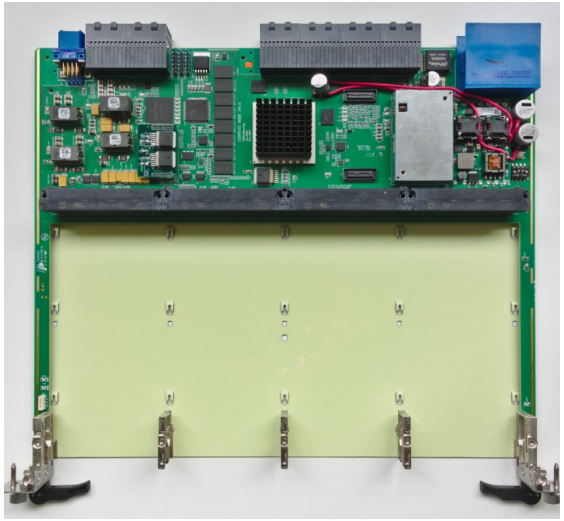

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- Firmware adjustments
  - Implemented custom IP cores
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  - Link layer protocol converts from Aurora to AXI Stream by implementing wrappers
- Firmware is functional for the Merger Carrier
- Adding additional interrupts of the Belle II Format Handler core
- Next step: Updating firmware of the Selector Carrier

Replacement of ONSEN?

- ONSEN links are operated at 6.125 Gbps
- New Carrier board supports up to 16.3 Gbps
- New Belle II DAQ system (PCIe40) will support up to 10 Gbps, but Belle2link standard is 2.54 Gbps
- ONSEN system full fills requirements of maximum luminosity
  - 20 Gbytes/s bandwidth at 3% occupancy
  - 30 kHz trigger rate
- No need to be replaced by PCIe40

New Idea: ONSEN Self-ROIs

- Slow pion rescue (see talk by Johannes Bilk)
- Master thesis by Stephanie Käs showed that 80% slow pion efficiency and 80% slow pion purity can be achieved with decision tree of only 3 variables
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- Modify Selector AMC firmware
  - Look for pixels with high pixel value (~230 or higher)
  - Generate ONSEN ROI (at least 3x3 matrix) around the pixel
  - No external ROI from HLT
  - Disadvantage: Requires processing PXD data twice

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- Calculated in 200 frames
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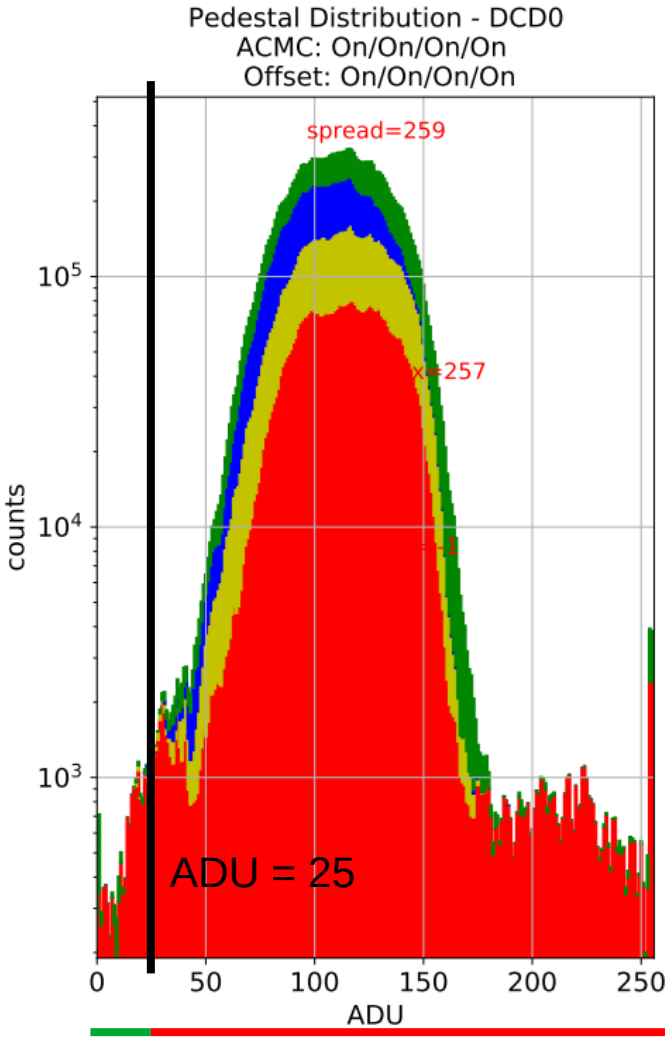
- Only a small number of pixel are able to produce high pixel values
- Problem: Pedestal distribution will influence significantly ROI efficiency

DHP 1
DHP 2
DHP 3
DHP 4



Conclusion and Remarks

- ONSEN (Online Selection Nodes) is FPGA based PXD data reduction system
- 4 defective AMCs and development of spare Merger Carrier (CNCB v4.0)
- Implementation of ONSEN ROIs to rescue slow pions → Generate 3x3 matrix around high pixel values
- Offset calibration may impede ONSEN ROIs
- Very few resources left on the Selector AMC FPGA
- Current configuration is very stable