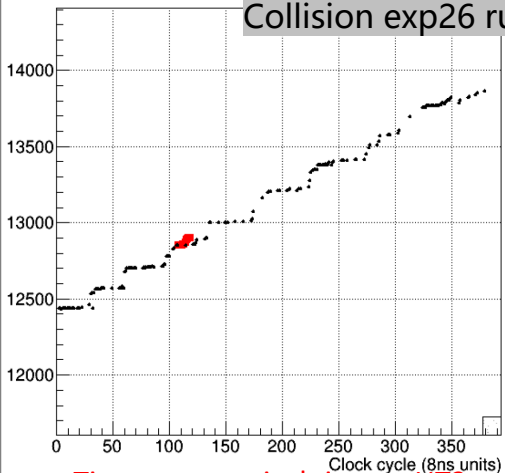# TOPTRG Status
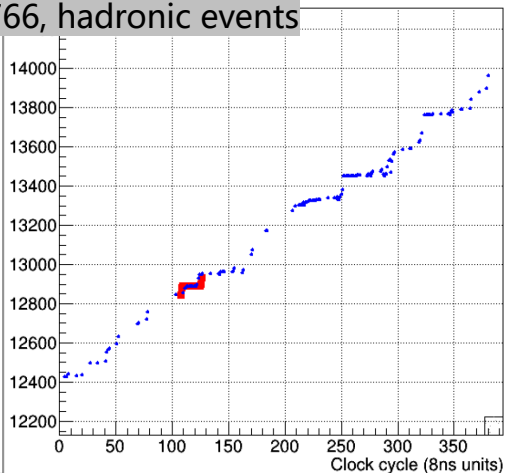
Tianping Gu, Erfei Wang, Vladimir Savinov

University of Pittsburgh

Nov. 30th, 2021

Collision exp26 run 766, hadronic events

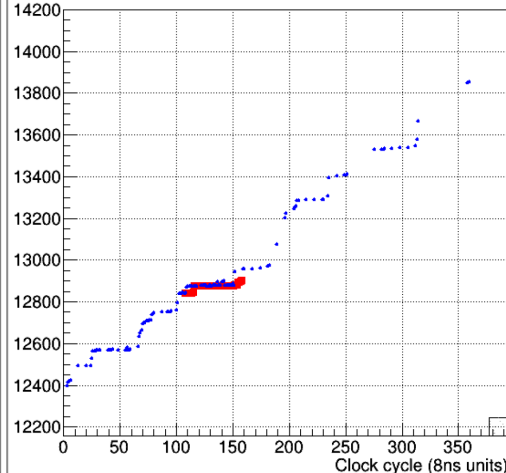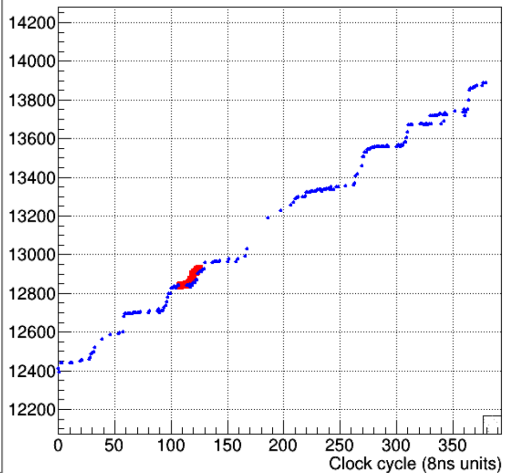Slot 2 : TOP / TRG / L1 / iSim TOP / iSim TRG hits: 11 / 175 / 0 / 0 / 2191

Slot 5 : TOP / TRG / L1 / iSim TOP / iSim TRG hits: 20 / 142 / 83 / 0 / 1850

Slot 1 : TOP / TRG / L1 / iSim TOP / iSim TRG hits: 18 / 214 / 46 / 0 / 2845

Slot 15 : TOP / TRG / L1 / iSim TOP / iSim TRG hits: 51 / 132 / 55 / 0 / 2396

Timestamp arrival time at UT3

Timestamp value (photon arrival time on PMT, 2ns)

Clock cycle (8ns units)

TOP TRG core problem statement

TOP trigger path is almost saturated with timestamps:

TOP FEE operates with very low trigger thresholds which are deemed necessary for PID performance. These thresholds are also used to generate trigger timestamps.

In contrast to TOP main readout, TOP TRG does not have feature extraction to filter out electronic noise, pulses of abnormal shapes and small amplitude signals.

Beam backgrounds affects TOP TRG timing in two ways:

- t0s based on bckg overwrite the one made for signal
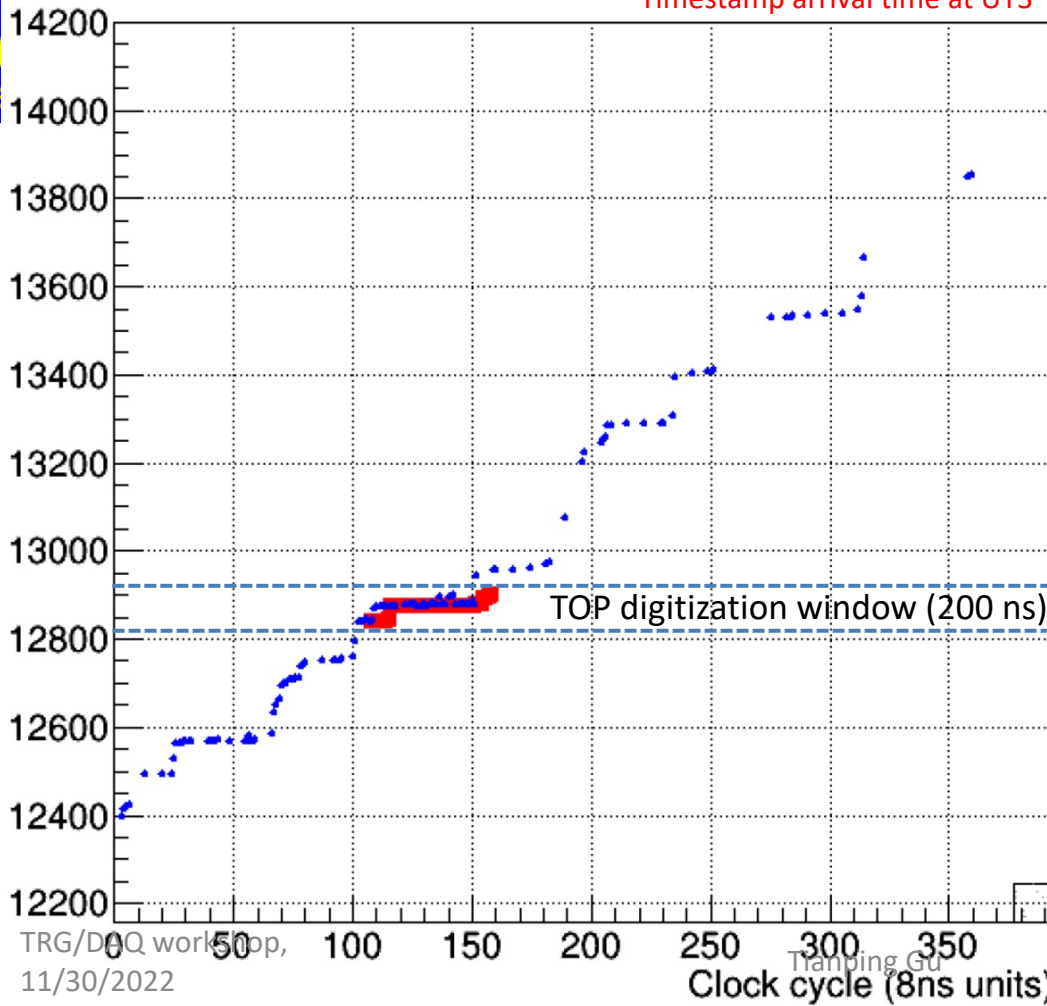- t0s based on bckg from wrong slots contaminate the combined t0

Possible solution:

- Require matching with CDC 2D tracks.

- Choose a relatively narrow timing window (e.g., [100,200]) to exclude slot decisions based on background.

2

Timestamp arrival time at UT3

Collision data exp/run 26/766:

Red: TOP main readout hits

Blue: TOP TRG waveform readout timestamps

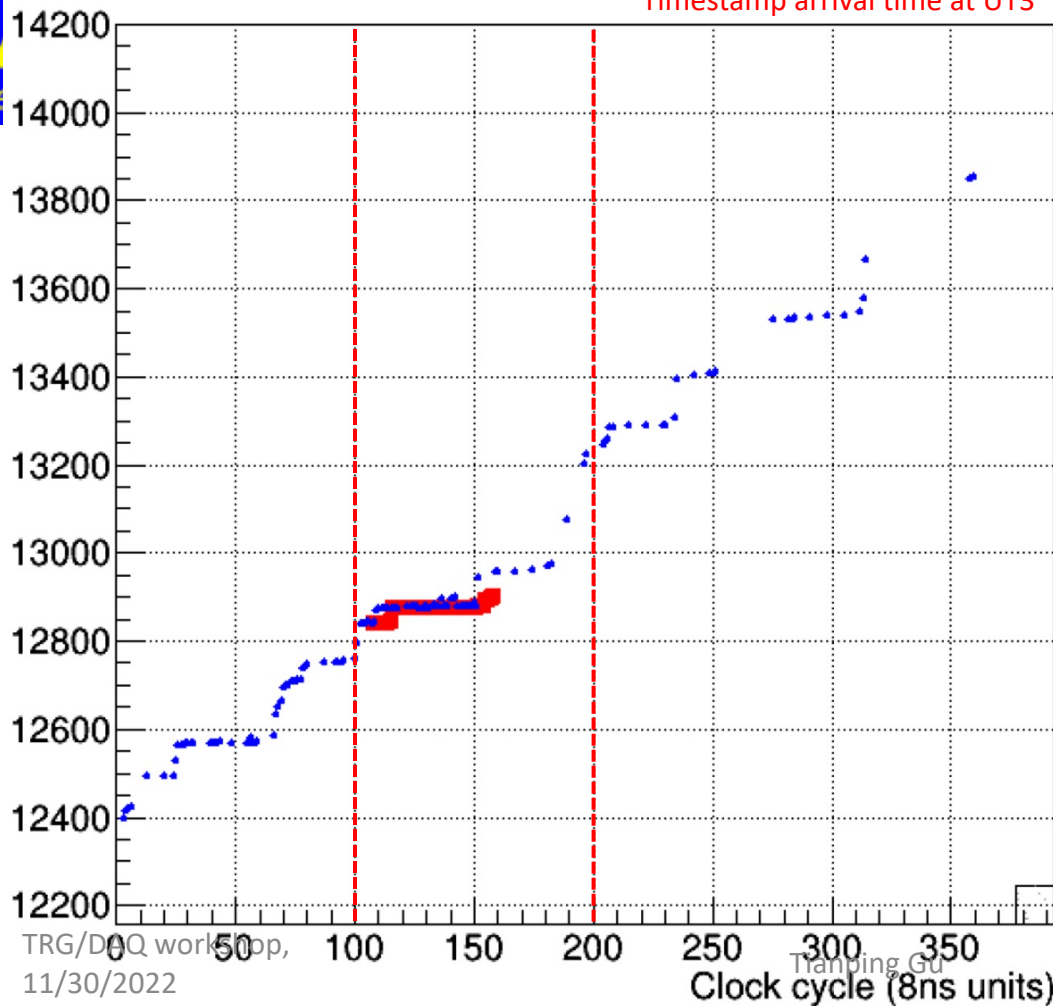TOP main readout has a very narrow digitization window (200 ns) w.r.t. GDL L1 decision.

This is why TOP main readout does not suffer from beam-related background, while TOP TRG does.

Almost each horizontal sequence of timestamps on this plot represents a burst of photons from beam-related background. These photons arrive at PMT in the same narrow interval of times. They differ from collision-related photons primarily by multiplicity.

Tianping Gu

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Timestamp arrival time at UT3

Collision data exp/run 26/766:

Red: TOP main readout hits

Blue: TOP TRG waveform readout timestamps

Currently, TOP TRG makes its timing decisions completely independently of ECL and CDC.

Therefore, in contrast to TOP main readout, TOP TRG is unable to reject background timestamps using digitization window w.r.t. the actual L1 decision.

We choose a narrow clock cycle window (e.g., between 100 and 200 clock cycles) to exclude slot-level background-based timing decisions.

This is an approximation for CDC-TOP TRG-level matching, grlcdc bits could be set to "high" for 200 clock cycles when there is a track pointing at a slot.

CDC-TOP matching

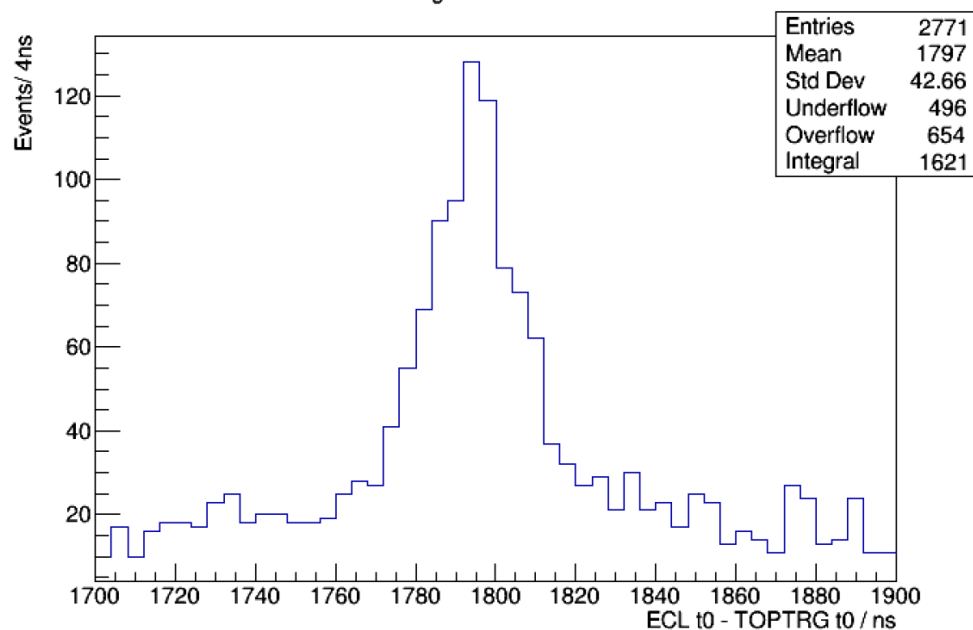Performed offline simulation for several slot-level and combined algorithms:

1.
Slot-level: maximum loglikelihood in the fixed timing range [100,200]. (logL threshold cut)
Combined: average of slot-level decisions with CDC 2D TRG track matching.
To be sent to GDL: this combined decision.

2.
Slot-level: maximum loglikelihood in the fixed timing range [100,200]. (logL threshold cut)
Combined: slot-level decision with the most hits with CDC 2D TRG track matching.
To be sent to GDL: this combined decision.

3.
Slot-level: generate slot-level decision on every clock cycle. (logL threshold cut)
Combined: average of slot-level decisions for the same clock cycle with CDC 2D TRG track matching.
To be sent to GDL: combined decision with the largest number of slot-level decisions.

4.
Slot-level: generate slot-level decision on every clock cycle. (logL threshold cut)
Combined: slot-level decision with the most hits of the same clock cycle with CDC tracks matching.
To be sent to GDL: combined decision with the largest number of slot-level decisions.

Approach 1: exp26 run 766, hadronic events

ECL t0 - TOPTRG t0 using TOPTRG waveform with CDC tracks

Entries	2771
Mean	1797
Std Dev	42.66
Underflow	496
Overflow	654
Integral	1621

Collision exp26 run 766, hadronic events
Loglikelihood threshold: 10000000 (equivalent to ~15 timestamps)
Physics region (waveform readout clock cycles): [100, 200]
TOP TRG trigger waveform used in simulation
TOP-CDC matching is required for slots included in the algorithm
Figure of merit: TOP TRG timing w.r.t. ECL timing

Approach 1:

Slot-level timing decisions: maximum loglikelihood in the fixed timing range [100,200]. (logL threshold cut)

Combined timing decision: average of slot-level timing decisions with CDC 2D TRG track matching.

For higher beam-related background, the timing resolution worsens significantly (compared, e.g., with lower-background exp24).
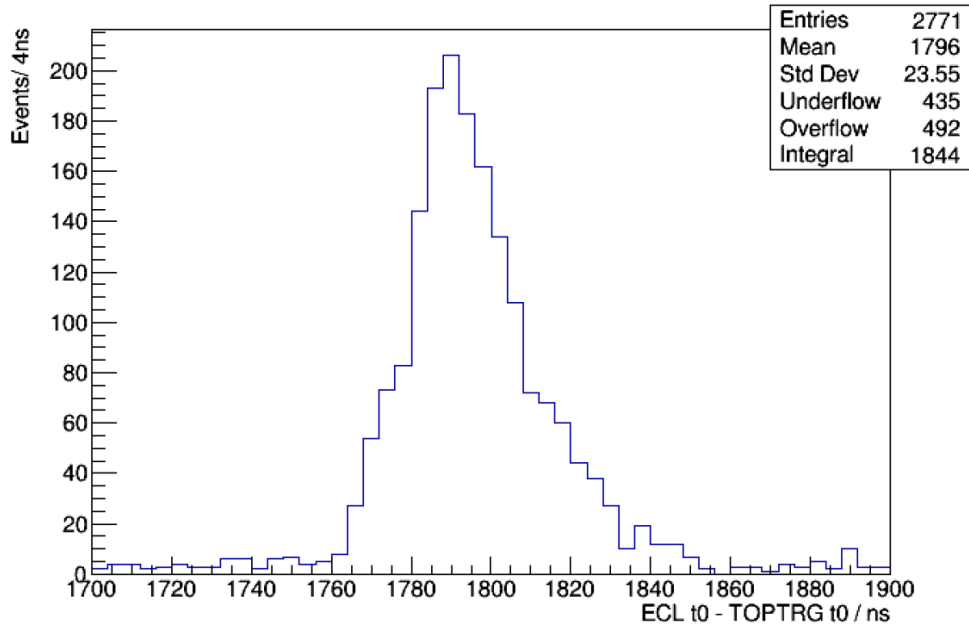
TOP TRG efficiency:
Fraction of events where (ecl_timing-top_timing) ∈ [1700,1900]
1621/2771 = 58.5%

Approach 2: exp26 run 766, hadronic events

ECL t0 - TOPTRG t0 using TOPTRG waveform with CDC tracks

Entries	2771
Mean	1796
Std Dev	23.55
Underflow	435
Overflow	492
Integral	1844

Collision exp26 run 766, hadronic events
Loglikelihood threshold: 10000000 (equivalent to ~15 timestamps)
Physics region (waveform readout clock cycles): [100, 200]
TOP TRG trigger waveform used in simulation
TOP-CDC matching is required for slots included in the algorithm
Figure of merit: TOP TRG timing w.r.t. ECL timing

Approach 2:

Slot-level timing decisions: maximum loglikelihood in the fixed timing range [100,200]. (logL threshold cut)
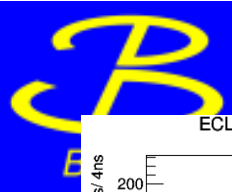
Combined timing decision: slot-level decision with the most timestamps with CDC 2D TRG track matching.

Use the slot t0 with most hits instead of average of all slot t0s
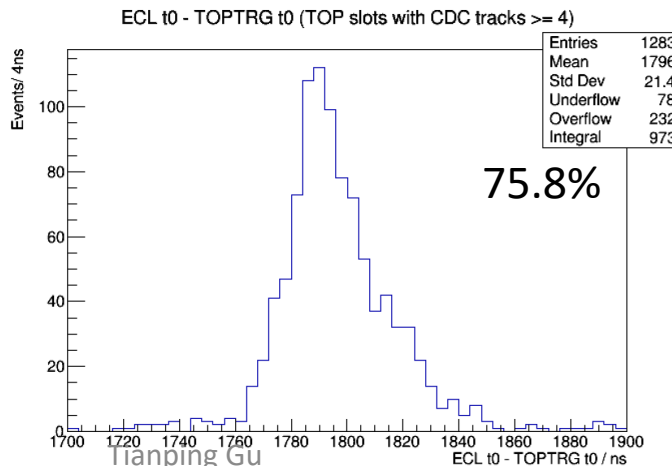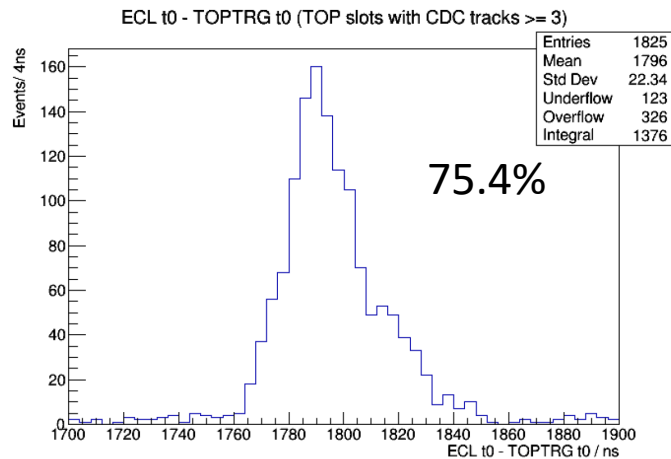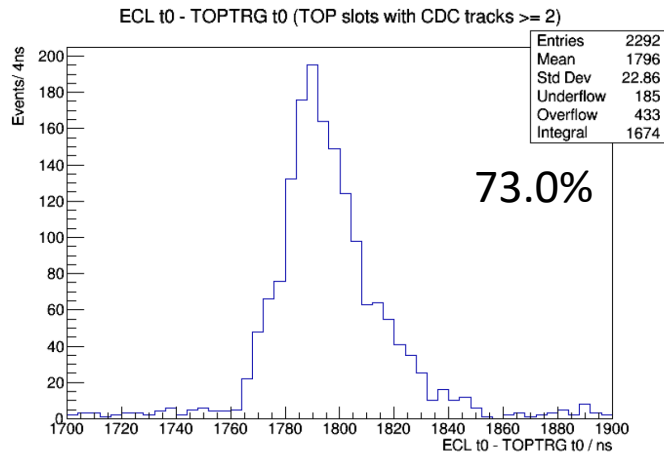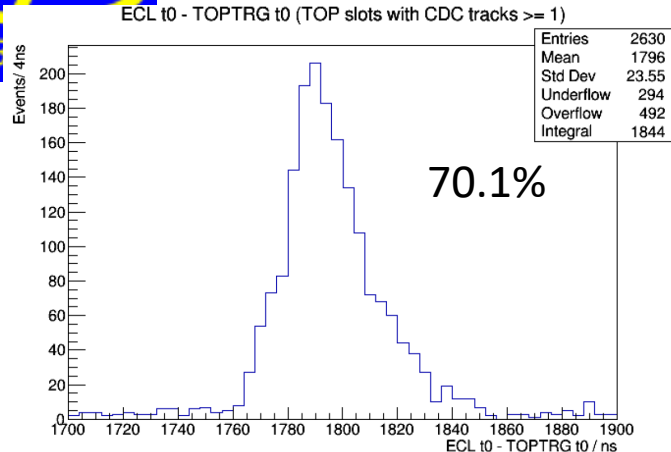=> suppress background

Efficiency: 1844/2771 = 66.5%
RMS: ~ 24 ns, Resolution: ~ 15 ns
Resolution improves significantly

Approach 2: exp26 run 766, hadronic events with high particle multiplicity

- Collision exp26 run 766 hadronic events
- Loglikelihood threshold: 10000000 ~15 hits
- Physics region: [100, 200]

TOP TRG t0 distributions for events which have more than n TOP slots with CDC tracks pointing to.

Efficiency for high-multiplicity hadronic events ~75%
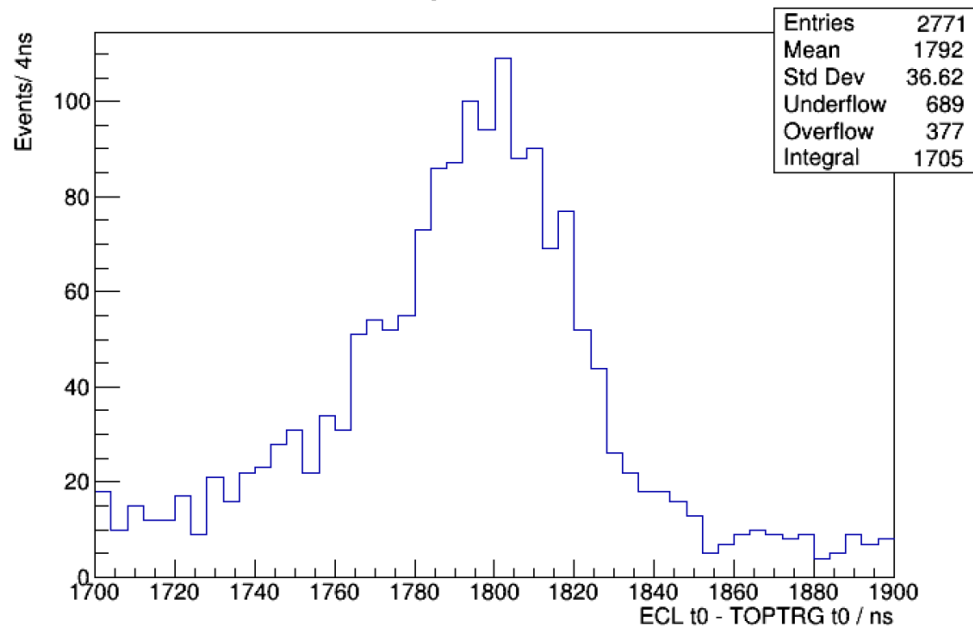RMS: ~ 22 ns
Resolution: ~ 13 ns

ECL t0 - TOPTRG t0 using TOPTRG waveform with CDC tracks

Entries	2771
Mean	1792
Std Dev	36.62
Underflow	689
Overflow	377
Integral	1705

Collision exp26 run 766, hadronic events
Loglikelihood threshold: 10000000 (equivalent to ~15 timestamps)
Physics region (waveform readout clock cycles): [100, 200]
TOP TRG trigger waveform used in simulation
TOP-CDC matching is required for slots included in the algorithm
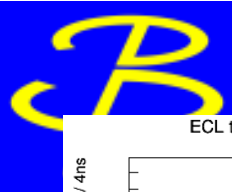Figure of merit: TOP TRG timing w.r.t. ECL timing

Approach 3:

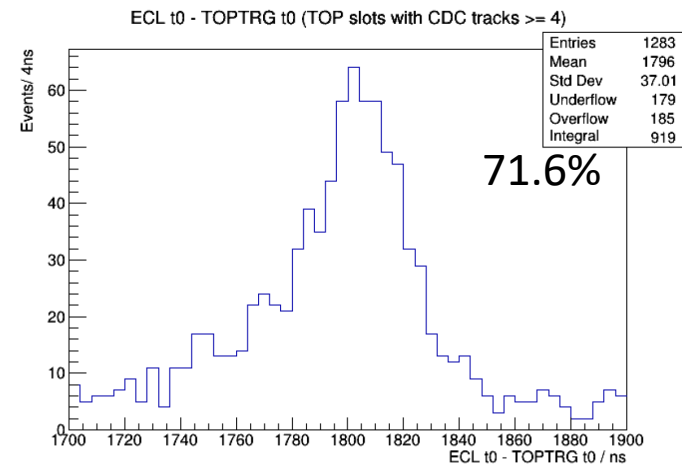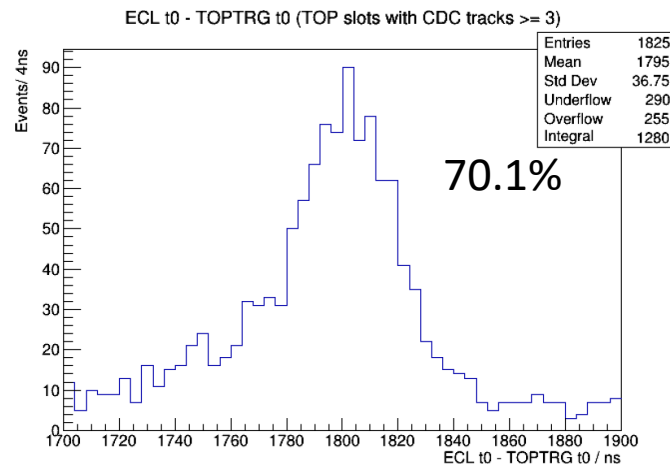Slot-level timing decisions: generate slot-level decision on every clock cycle. (logL threshold cut)

Combined timing decision: average of slot-level timing decisions made on the same clock cycle with CDC 2D TRG track matching.

To be sent to GDL: a combined timing decision with the largest number of slot-level timing decisions

Efficiency: 1705/2771 = 61.5%

- Collision exp26 run 766 hadronic events
- Loglikelihood threshold: 10000000 ~15 hits
- Physics region: [100, 200]

TOP TRG t0 distributions for events which have more than n TOP slots with CDC tracks pointing to.

Efficiency for high-multiplicity hadronic events ~70%
Bad resolution

11/30/2022

Approach 4: exp26 run 766, hadronic events

ECL t0 - TOPTRG t0 using TOPTRG waveform with CDC tracks

Entries	2771
Mean	1803
Std Dev	30.86
Underflow	592
Overflow	358
Integral	1821

Collision exp26 run 766, hadronic events
Loglikelihood threshold: 10000000 (equivalent to ~15 timestamps)
Physics region (waveform readout clock cycles): [100, 200]
TOP TRG trigger waveform used in simulation
TOP-CDC matching is required for slots included in the algorithm
Figure of merit: TOP TRG timing w.r.t. ECL timing

Approach 4:

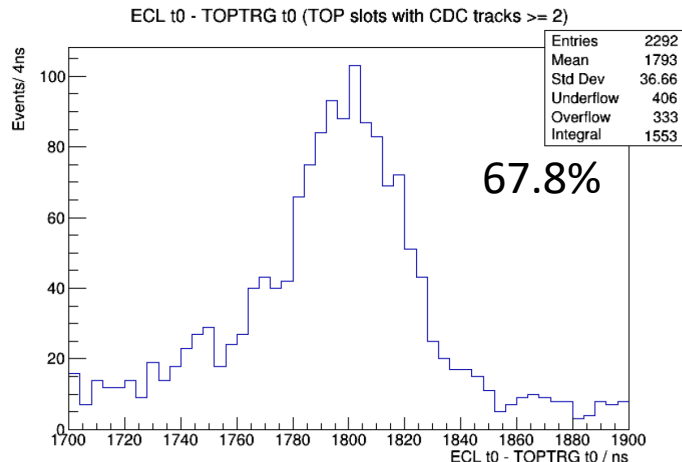Slot-level timing decisions: generate slot-level decision on every clock cycle. (logL threshold cut)
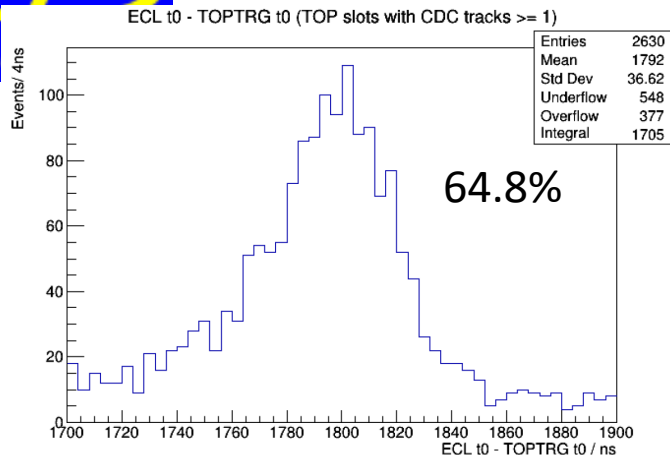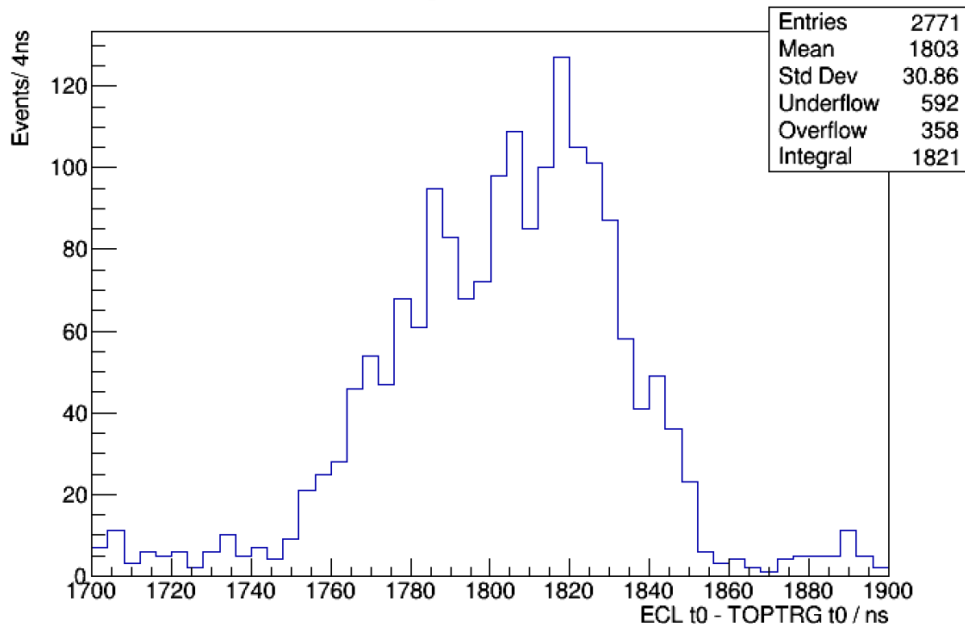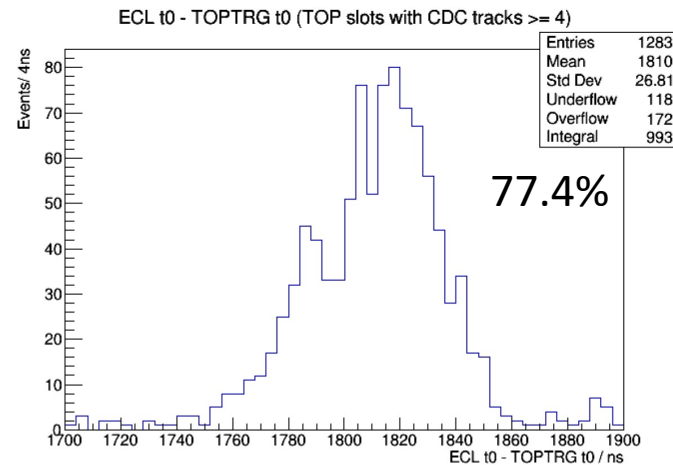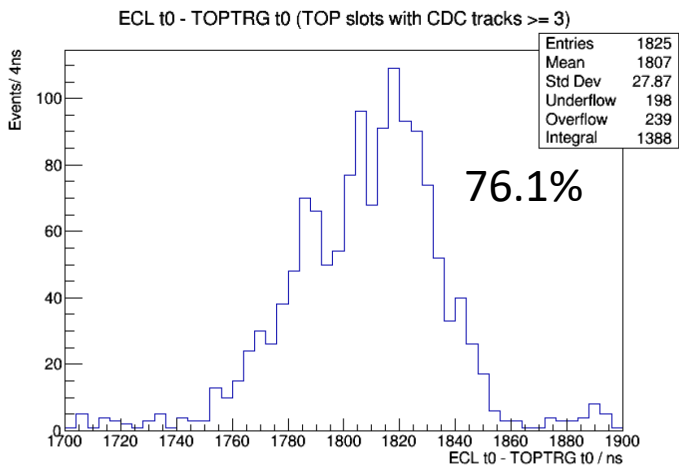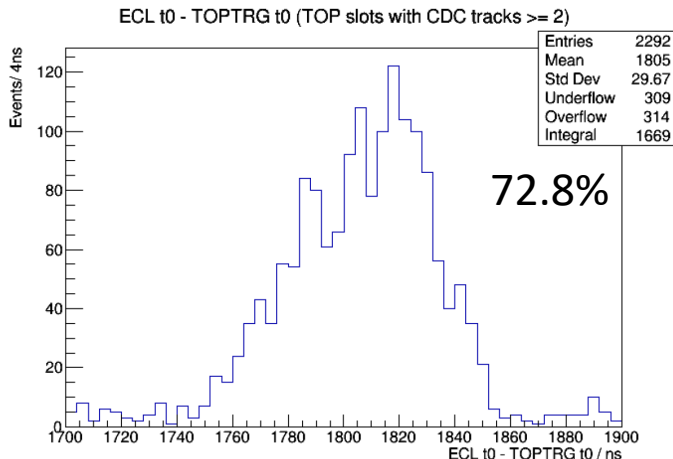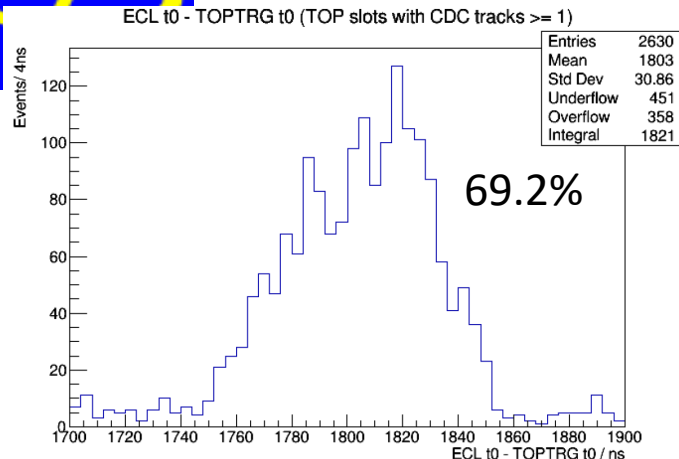
Combined timing decision: slot-level timing decision with the most hits made on the same clock cycle with CDC 2D TRG track matching.

To be sent to GDL: a combined timing decision with the largest number of slot-level timing decisions

Efficiency: 1821/2771 = 65.7%

ECL t0 - TOPTRG t0 (TOP slots with CDC tracks >= 1)

Entries	2630
Mean	1803
Std Dev	30.86
Underflow	451
Overflow	358
Integral	1821

69.2%

ECL t0 - TOPTRG t0 (TOP slots with CDC tracks >= 2)

Entries	2292
Mean	1805
Std Dev	29.67
Underflow	309
Overflow	314
Integral	1669

72.8%

ECL t0 - TOPTRG t0 (TOP slots with CDC tracks >= 3)

Entries	1825
Mean	1807
Std Dev	27.87
Underflow	198
Overflow	239
Integral	1388

76.1%

ECL t0 - TOPTRG t0 (TOP slots with CDC tracks >= 4)

Entries	1283
Mean	1810
Std Dev	26.81
Underflow	118
Overflow	172
Integral	993

77.4%

- Collision exp26 run 766 hadronic events
- Loglikelihood threshold: 10000000 ~15 hits
- Physics region: [100, 200]

TOP TRG t0 distributions for events which have more than n TOP slots with CDC tracks pointing to.

Efficiency for high-multiplicity hadronic events ~76%.

Resolution is worse than in approach 2.

11/30/2022

Summary of CDC-TOP matching studies

- Offline simulation performed for several slot-level and combined algorithms.
- Currently, the best results obtained using approach 2
  (using timing from the slot with the largest number of timestamps):

  Efficiency for hadronic events: ~67%
  Efficiency for high-multiplicity hadronic events: ~75%
  (ECL-TOP) timing resolution for hadronic events: ~15 ns
  (ECL-TOP) timing resolution for high-multiplicity hadronic events: ~13 ns

Discussion:
- Agreed to use approach 2 as tentative CDC-TOP matching algorithm.
- Agreed to stream all TOPTRG slot decisions to GRL and perform matching at GRL.
- Agreed on TOPTRG -> GRL data format, send slot-level info to GRL (T0, hit number, flag).

TOPTRG->GRL data format

Flags for slot-t0:
1bit * 16slots = 16bits

Number of hits: range [0,255]
8bits * 16slots = 128bits

Slot-t0: range [0,46080] / 2ns
16bits * 16slots = 256bits
MSB 11 bits are common for all slots (reject slot-t0 outside 32*2=64ns window),
11bits + 5bits * 16slots = 91bits

However, MSB 11 bits should be sent from both UT3s for validation.

Total: 16+128+91(+11) = 235(246)bits

GTH 8 lanes from TOPTRG to GRL:
5Gbps: 256bits/127MHz

bit	0	1	2	3	4	5	6	7
[0:7]	Flag slot 1-8							
[8:15]	Hit numbers slot 1							
[16:23]	Hit numbers slot 2							
[24:31]	Hit numbers slot 3							
[32:39]	Hit numbers slot 4							
[40:47]	Hit numbers slot 5							
[48:55]	Hit numbers slot 6							
[56:63]	Hit numbers slot 7							

bit	0	1	2	3	4	5	6	7
[64:71]	Hit numbers slot 8							
[72:79]	MSB 11 bits of slot T0							
[80:87]	T0 slot 1-8							
[88:95]								
[96:103]								
[104:111]								
[112:119]								
[120:127]	Spare 5bits							

Porting TOPTRG to UT4

Utilization	Post-Synthesis	Post-Implementation	
		Graph	Table
Resource	Utilization	Available	Utilization %
LUT	255502	1074240	23.78
LUTRAM	3240	231840	1.40
FF	401987	2148480	18.71
BRAM	159.50	3780	4.22
IO	178	702	25.36
GT	45	76	59.21
BUFG	32	1800	1.78
MMCM	3	30	10.00

Power **Summary** | On-Chip

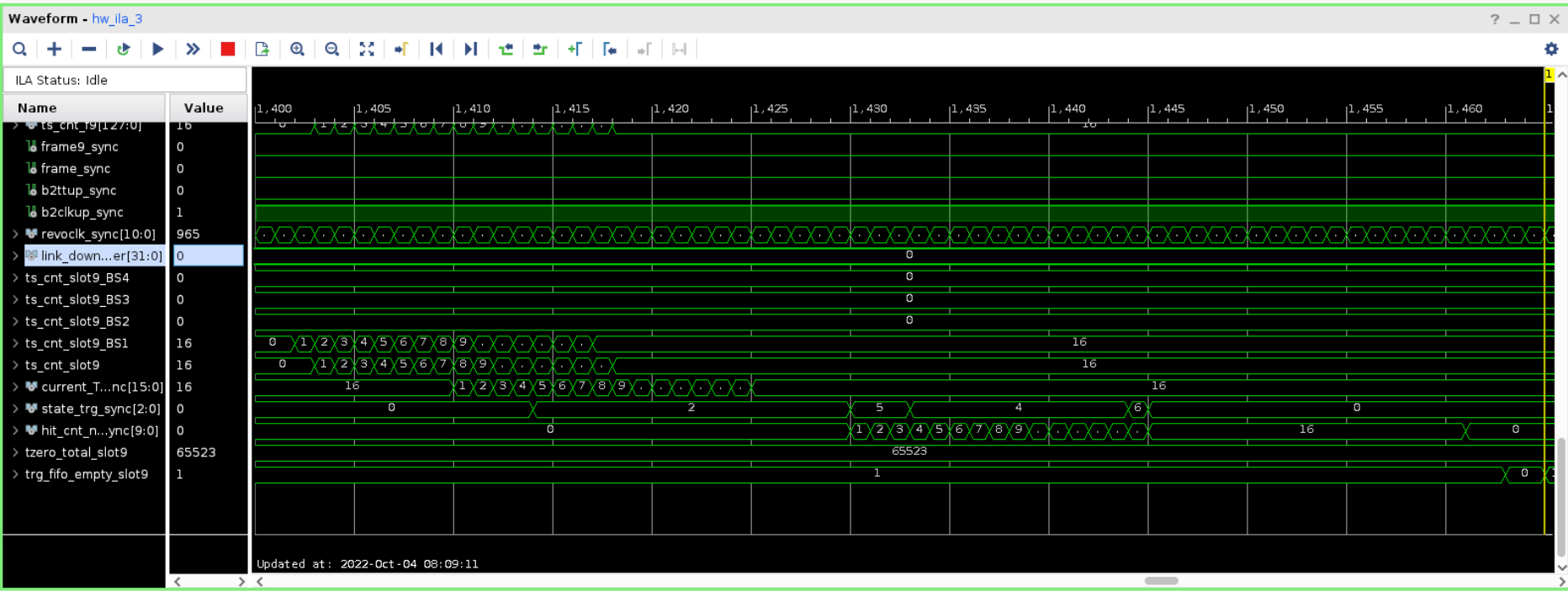|	
Total On-Chip Power:	22.809 W
Junction Temperature:	43.1 °C
Thermal Margin:	56.9 °C (66.0 W)
Effective θJA:	0.8 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report

Successfully ported all major parts of TOPTRG to UT4, e.g., core decision logic, TOPFEE data link, GRL/GDL link, VME, Belle2link.

Tested core logic on UT4 at KEK using test generator / pulser.
Plan to add fans in E-hut and turn on UT4s to test VME and Belle2link,
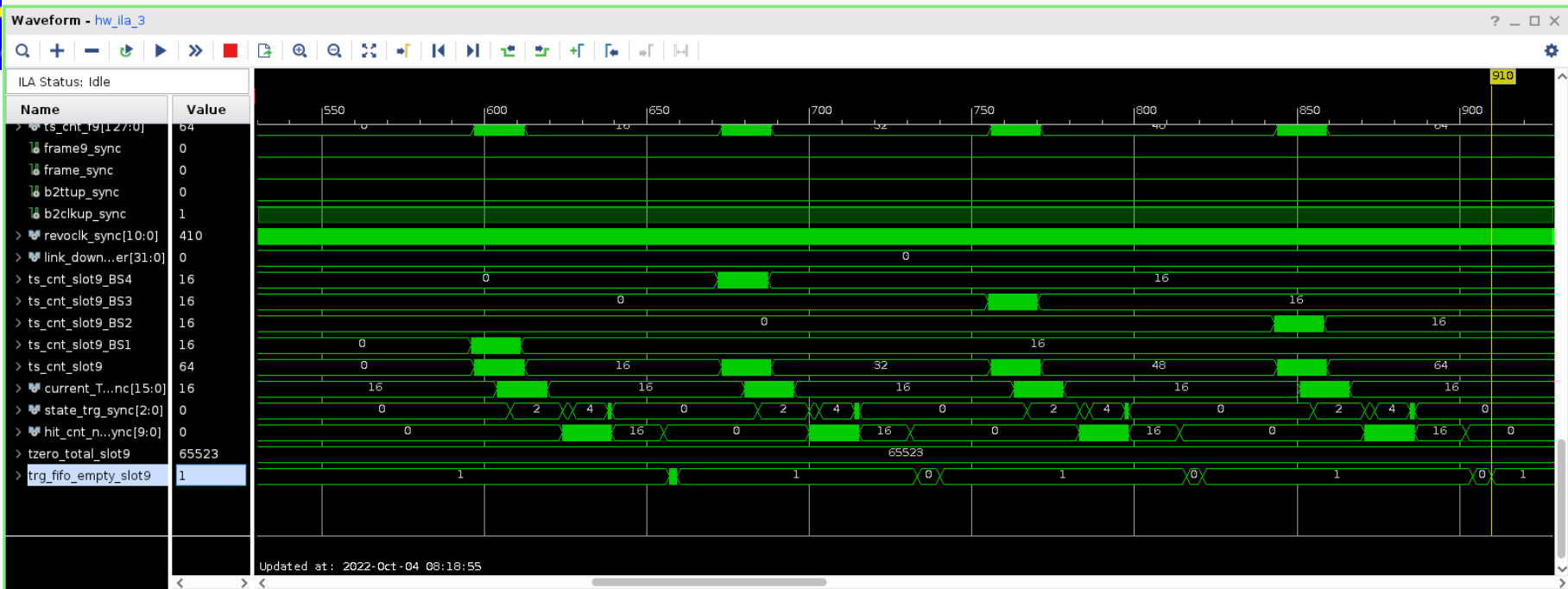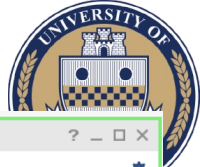Check the slot-level data streamed to GRL.

SCROD test generator : s09a generates 16 timestamps.
TOPTRG receive 16 timestamps and generate the t0 decisions correctly.
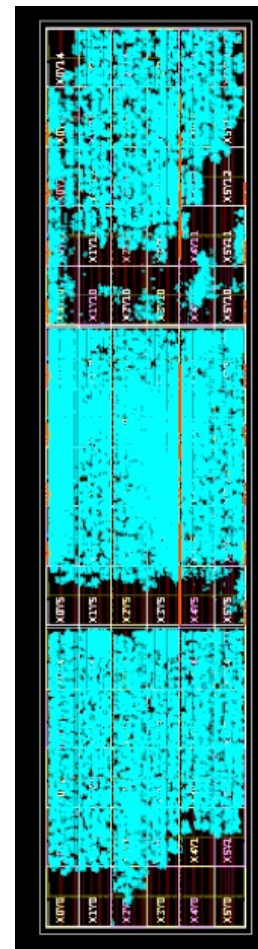
TOPFEE -> TOPTRG data link (slot 9)

SCROD test generator : each boardstack generates 16 timestamps.
TOPTRG receive 4 bunches of timestamps and generate the t0 decisions respectively.

Tianping Gu

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Summary

- Performed offline simulation for several slot-level and combined timing algorithms using trigger readout data.
- Investigated the TOP TRG efficiency for hadronic events of relatively high charged particle multiplicity.
- Plan to stream all TOPTRG slot decisions to GRL and perform matching at GRL.

- Successfully ported all major parts of TOPTRG to UT4, e.g., core decision logic, TOPFEE data link, GRL/GDL link, VME, Belle2link.

- Next steps:
- Add fans in E-hut and turn on UT4s to test VME, Belle2link and check the slot-level data streamed to GRL.
- Work on implementing CDC-TOP matching logic on GRL