Status on UT4 ETM

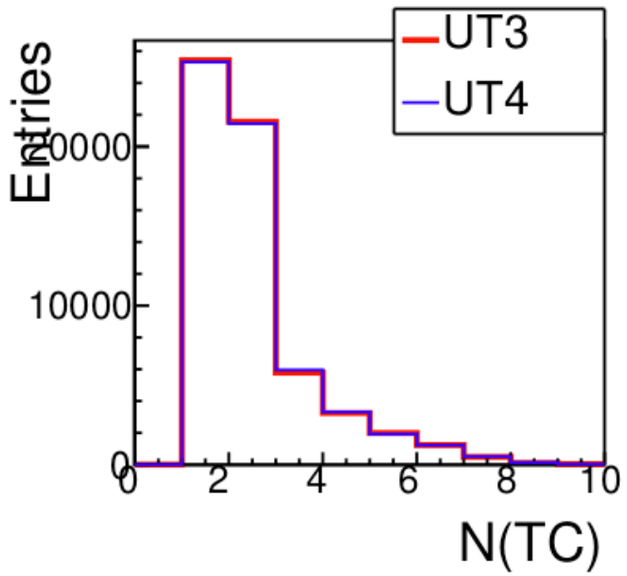
2022/10/05
TRG/DAQ workshop
Y.Unno

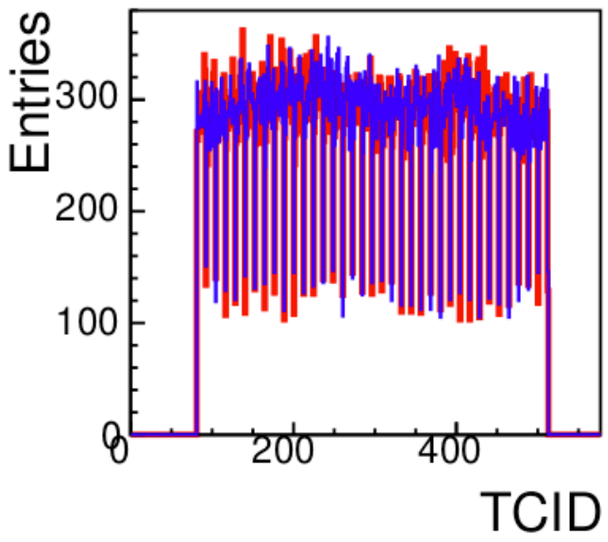
ETM to UT4 from UT3

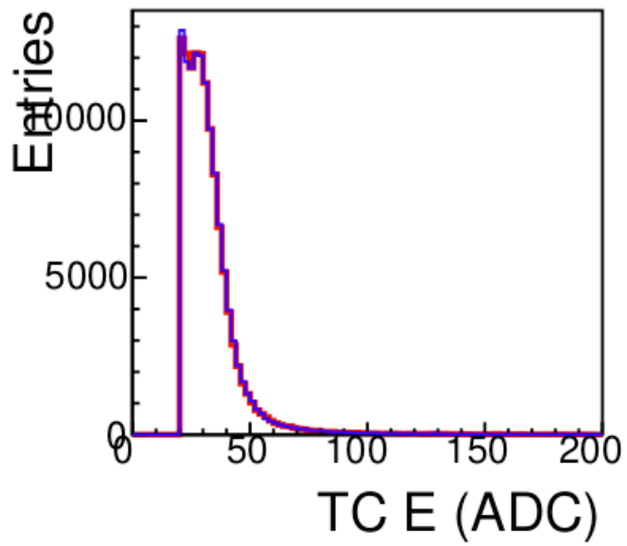
- Resource usage of UT3 ETM is around 70% and getting hard to have new logic
  - Compile time is >10 hours to get bit steam file without timing error
- Borrowed two VU160 UT4, using one at e-hut and another at B2 test bench.
- Optical links
  - configuration
    - 7 GTH for 7TMM GTX with 5Gbps
    - 1 GTH for B2L GTP with 2.5Gbps
    - 1 GTY for GDL with 5Gbps
    - 1 GTY for GRL with 5Gbps
  - Status
    - Data transmissions of all links are found to be OK, and stable once link is up
    - Link up for TMMs fails sometimes when FW is rebooted and need to send reset signal
    - Latencies are not checked in detail yet
    - B2L readout with UT4 and UT3 w/o problematic logic are consistent
- VME interface changed to design developed by HanWook
  - Need to update local software and SLC

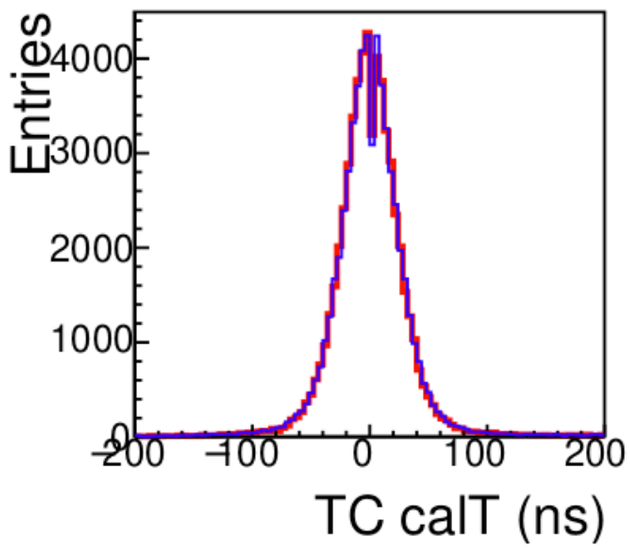
ETM to UT4 from UT3

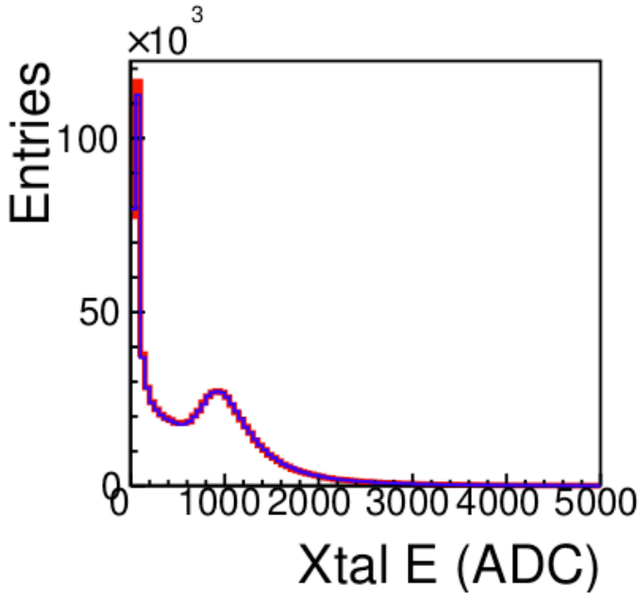
- Local cosmic runs with UT3 and UT4 by sending trigger to FTSW64 from RJ45
  - ICN logic is excluded from firmware in this test.

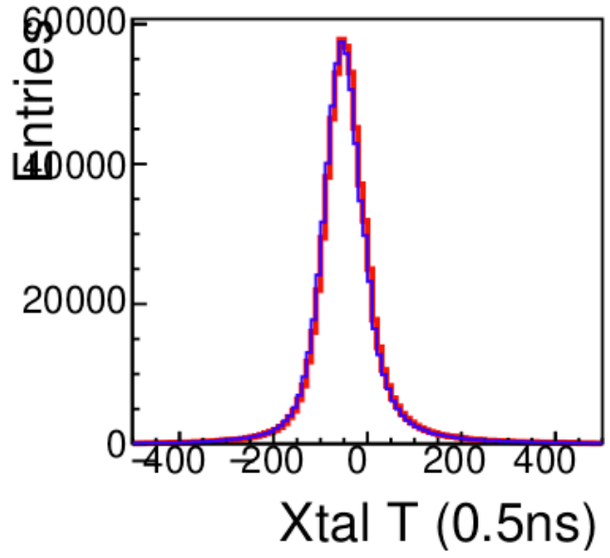












- The results are consistent

Two timing errors on UT4 ETM

- All logics were implemented, but timing errors in b2tt and clustering logic
  - So far, ignoring the error in b2tt with set_fualse_path
  - There was same timing error in clustering logic on UT3 ETM
    - Avoided with smartexplorer for UT3, but failed on UT4 ETM
    - Considering to tackle when we move to UT4

Timing err with Idelayctrl

- Timing error in b2tt

Summary	
Name	Path 147
Slack	-2.755ns
Source	map_b2tt/gen_useextclk0.map_clk/clr_ictrl_reg/C (rising ed
Destination	map_b2tt/gen_useextclk0.map_clk/gen_ictrl1.map_ic/RST (

- How Xilinx manuals say about idelayctrl for ultrascale ?
  - One manual says in section of idelayctrl

    At least one of these design elements must be instantiated when using IDELAYE3 or ODELAYE3.

  - Other manual says in sections of idelaye3 and odelaye3

    - COUNT mode:
      - There is no need to use an IDELAYCTRL component because the delay line is used in the uncalibrated state without voltage and temperature compensation.

    - In b2tt, idelaye3 and odelaye3 use only COUNT mode
- Timing violation disappeared after deactivating idelayctrl in b2tt
  - instantiate idelayctrl and apply set_false_path is another way to avoid timing err
  - In case of TIME mode in idelaye3 and odelaye3, idelayctrl needs to be instantiated
- Check if data to GDL and B2L data are reasonable or not, with cosmic run
  - If no problem was found, keep excluding idelayctrl

Timing err with Idelayctrl

- Why only I encountered timing error in b2tt ?
  - I don't know usage of clk, and src, xdc files of other TRG members
  - Timing error does not depend on clk src(RJ45 or clock generator).

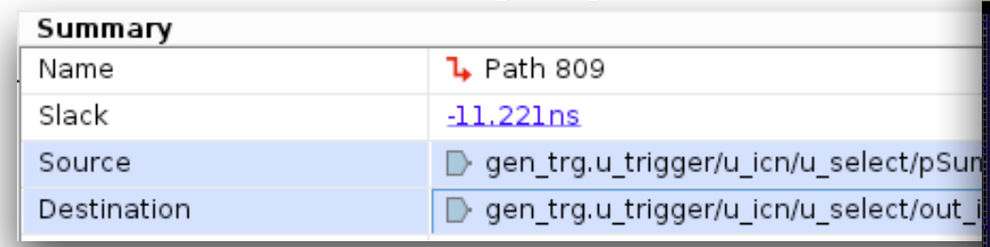
- In GDL case,
  - Timing constraint was not properly required in xdc file
    - create_clock -period 7.874 … [get_ports RJ_CLKP(0)] <= wrong
    - create_clock -period 7.874 … [get_ports RJ_CLKP[0]] <= correct

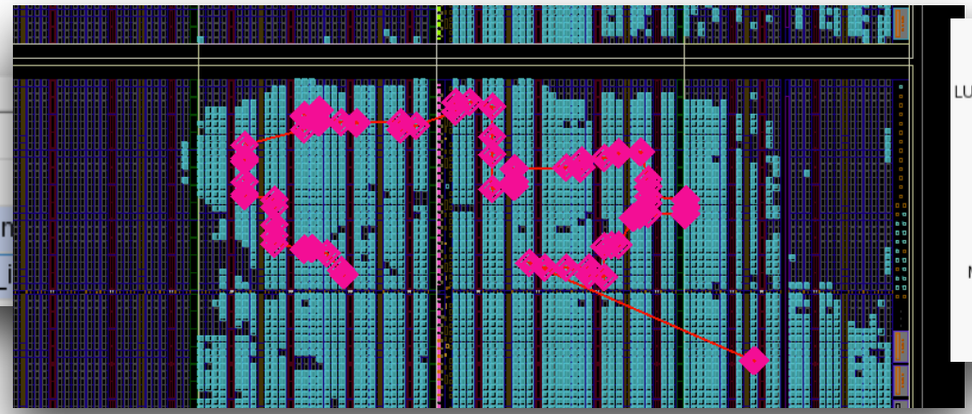
- To avoid timing error
  - pass init value '0' to USEICTRL in generic map of b2tt to deinstantiate idelayctrl
  - (Or use set_fualse_path for idelayctrl in xdc file if idelayctrl is instantiated)

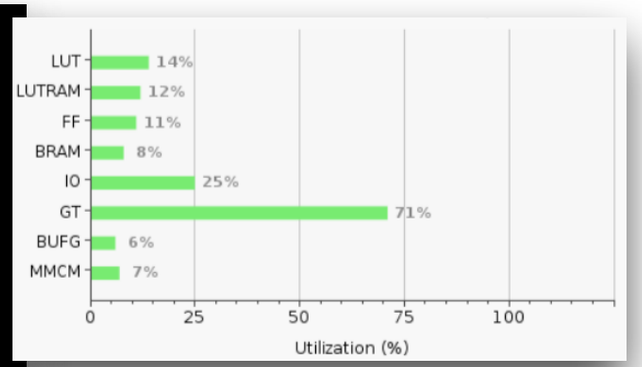
- I think Nakazawa-san will provide updated version of b2l.vhd

Timing error in cluster logic

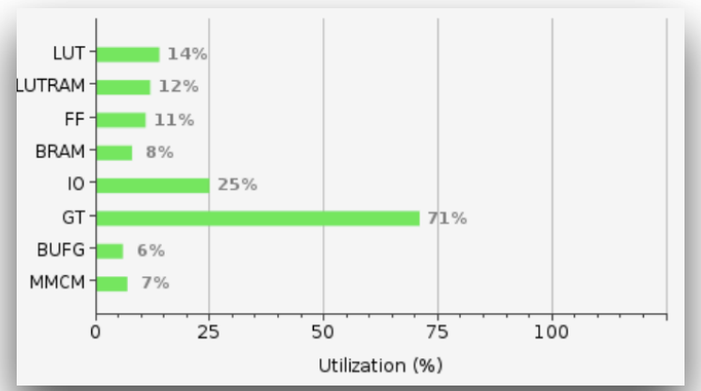
- Error at clustering logic





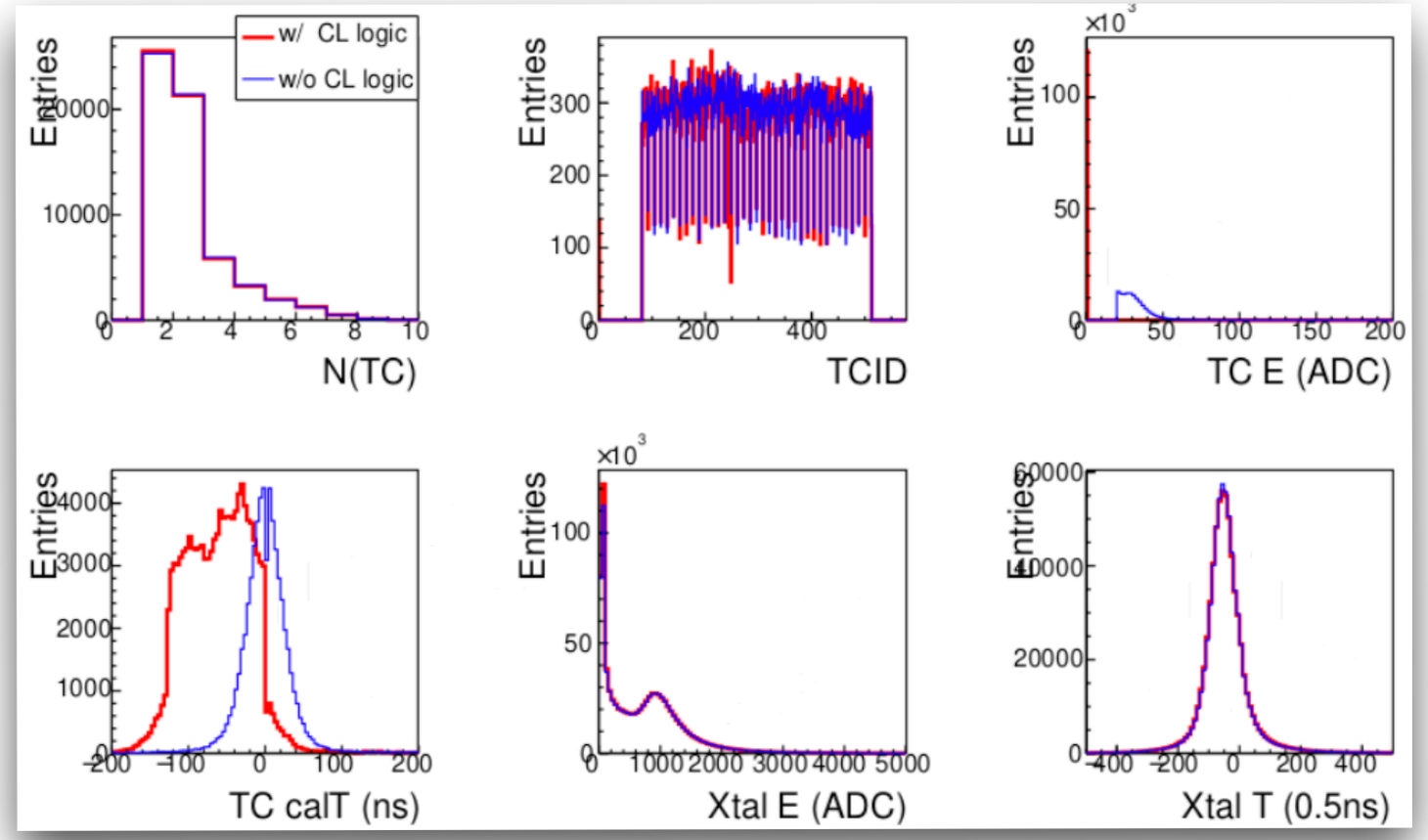


- Old logic
  - (1)prepare data(position/timing/energy) of 576 cluster candidates
  - (2)576 candidate to 6 clusters in one clock <= this caused timing error
- New logic
  - (1)prepare data(position/timing/energy) of 576 cluster candidates
  - (2)567 candidates to 6 clusters in 3 clocks
    - (2-1) 567 clusters to 36 x 6 clusters array
    - (2-2) 36 x 6 clusters to 4 x 6 clusters array
    - (2-3) 4 x 6 clusters to 6 clusters array
- This study was done with UT3 and 3 out-of 7 strategies provide no timing error
  - Confirmed consistent results btw tsim and firmware results
  - No problem in cosmic run
- On UT4, no timing error with default implementation strategy
  - No change in resource consumption
  - (Comparison with tsim is not done yet on UT4)



Problems

- Results of cosmic with clustering logic is strange.



  - ECL data are OK, only ecl trigger data is strange with UT4
  - TC E and TC T are independent from clustering in local cosmic run
- data arrival timing “ecl-inj” on GDL is strange
  - Same for w/ and w/o clustering logic
  - But, timing of trigger signal in local cosmic is same btw UT3 and UT4
- Will investigate with B2 test bench

Summary / plan

- Summary
  - Migration of ETM to UT4 is still in progress
    - Two timing problems were fixed
    - Strange ecl trg data in cosmic run

- Plan
  - Investigate the reason of strange results in cosmic w/ CL logic
  - Check latency for GDL
  - Improve instability of TMM-ETM at link start
  - Update/test logic to compare tsim and firmware data
  - Update software and slow control for new VME interface
  - Test 12Gps link for GDL and GRL
  - Stability check (mainly optical link for TMM, GRL, GDL)
  - Trigger server related tasks

Backup

Plan for LS1

- ETM to UT4 from UT3
  - Optical link
    - TMM, GDL, GRL, and b2link -> Stability check
  - I/O for trigger server
    - FW logic, Software update on trigger server
- Background study
  - BGOverlay logic for both MC and random data
  - Performance study for MC and data
  - Consistency study between MC and data
  - Based on the results, make a strategy for high luminosity and bkg conditions (for both after LS1 and LS2)
- ETM logic study for hie, Bhabha, and other bits
  - Detail studies with MC and data rejected by HLT filter ?
- Update/modify local run scripts ?
  - Update of script of single channel test run for PCIe40 => prepared by Mikahil
  - (Hope to) fix default large timing resolution
  - Prepare linearity local run script

Plan for LS1

- Calibration
  - TC Energy (in progress by Eunji)
  - TC timing
  - Automation system for TC E and T calibration (CAF can be utilized ?)
    - Or consider or prepare system(DQM) to monitor them with beam data
- TC and event timing study
  - TC energy weighted event timing
  - Xtal by xtal timing bias into tsim
- Software update
  - conditionDB
  - Integer tsim version
  - MC truth information
- Trigger server related work for ecl trigger
- Online luminosity by ecl trigger as redundancy requested by Alex

Plan after LS1 and in LS2

- Try to separate two energy deposition in one TC (if necessary) ?
  - If two signal peak positions are >500ns, it would be possible

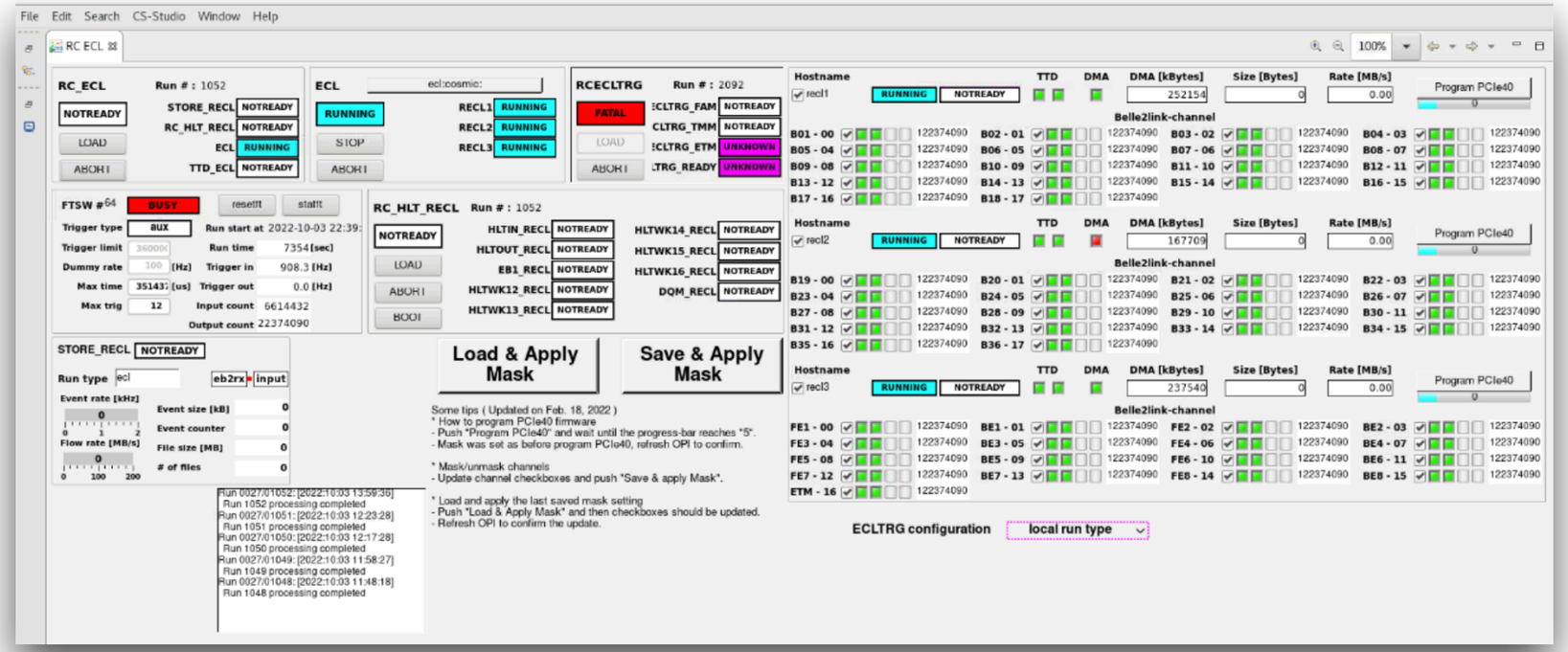
- New ShaperDSP ?
  - Currently 576 ShaperDSPs in 52 9-VMEs around Belle2 detector
  - Alex is planning to upgrade ShaperDSP
    - Some studies are in progress in BINP (the status not shown anywhere)
  - For ecl trigger, any requests and the meaningful improvement ?
    - “TC” timing can be improved if cell-by-cell timing adjustment in each TC is possible, but bad resolution is mainly from low energy TC
  - Any merit if logic of FAM can be implemented in new ShaperDSP ?
    - TC with from 4x4=16xtail to 2x2 if it improves some performance ?

- PureCsI ?
  - Would be not realistic…

Backup

System with PCIe40

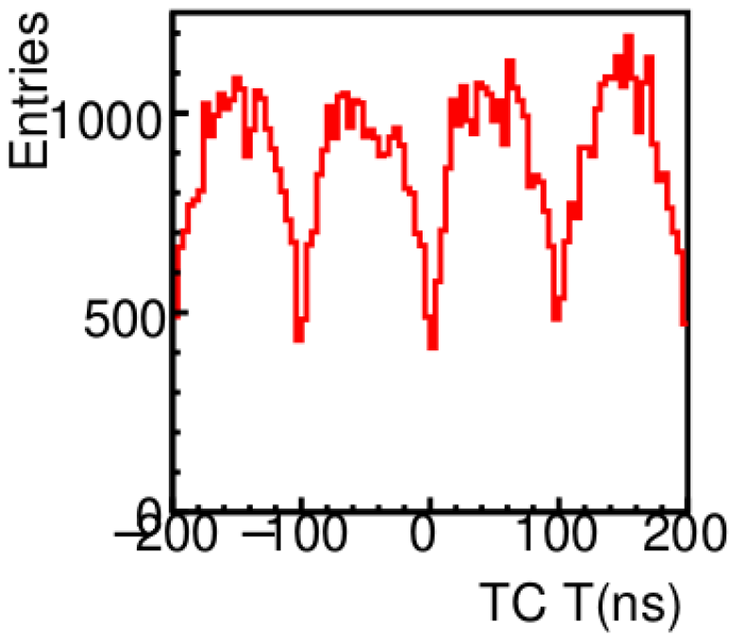
- Good shape with a lot of effort and help from Mikhail and DAQ experts



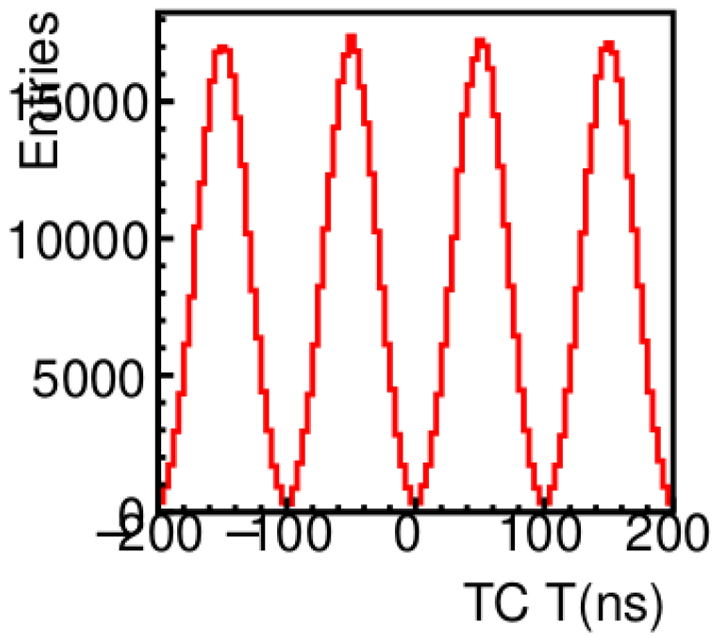
- Can take local runs(test pulse and cosmic)
  - User can change config for global, local cosmic, test pulse run from recl1
  - single channel test pulse run is possible
- No problem to take data w/ and w/o ETM configuration
  - Yamada-san updated software to change config automatically
- We can change attenuator coefficients easily for gain adjustment study
- Some functions on CSS for ecl trigger need to be updated

Status of background study

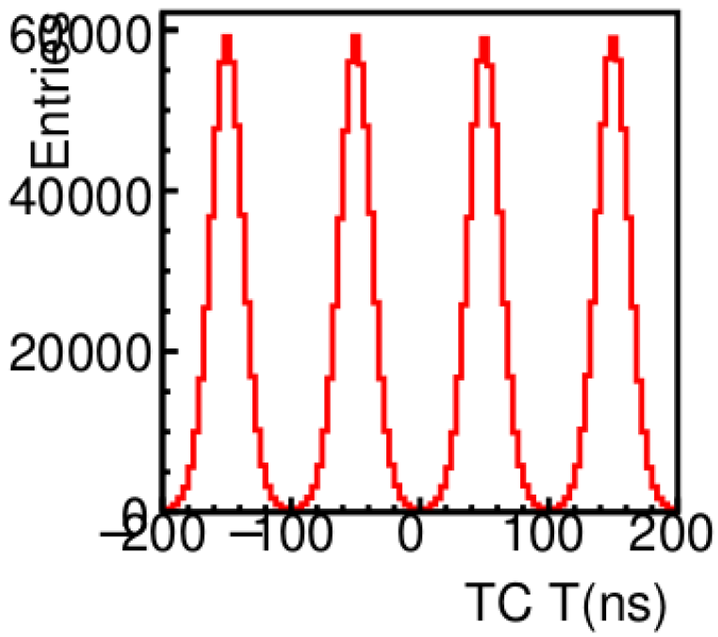
Early phase3



Nominal phase3 bkgx1



Nominal phase3 bkgx3



- Apparently TC timing distribution is strange.
  - TC energy distribution seems to be fine.
- Started the investigation

E-hut operation in LS1 (PCIe40 preparation)

S.Yamada

From a Gantt chart at SVD meeting on Mar. 1 ：
https://indico.belle2.org/event/6307/contributions/32993/attachments/15590/23376/220222-VXD_installation_2022c_cancelled_v0.pdf

Readout test with FEE (dummy trigger) **cannot** be done

Readout test with sensors(e.g. cosmic ray test) **cannot** be done

Cosmic ray test ?

	7	8	9	10	11	12	2023 Jan.	2	3	4	5	6	7	8
SVD					After IBBelle is turned off, no chance for cosmic ray test.									
							All FEEs -> B4, VXD commissioning							
CDC	Chiller work	LV off if air-con off			Be careful of VXD IP work		TOP PMT replacement(TBC)							
TOP							TOP PMT replacement(TBC)							
ARICH	Chiller work	All FEEs -> B4												
		Cosmic ray test is impossible.												
ECL		Endcap modules -> B4 (Barrell ECL is available for a dummy trigger test ? Endcap ECL's FEE is available as well ?)												
		Cosmic ray test with Barrell ECL is possible ?												
KLM														
TRG		E-hut air-conditioner (basically) OFF (Aug, Sep, Oct.)			Limited operation of E-hut air-conditioner. (Turn on if necessary such as cosmic ray test, global DAQ test)									

- If possible, we switch to PCIe40 in July and keep the system running when ECL is not used by ECL experts.
- Barrel ECL FEE is online in the LS1 ?
- Any ECL work in LS1 which conflicts to the DAQ commission ?

Preliminary

To save electricity cost