Belle II Trigger/DAQ Workshop 2022

2022/11/30 (Wed)

VXD TRG R&D status

The University of Tokyo

Tomoyuki Shimasaki

Motivation

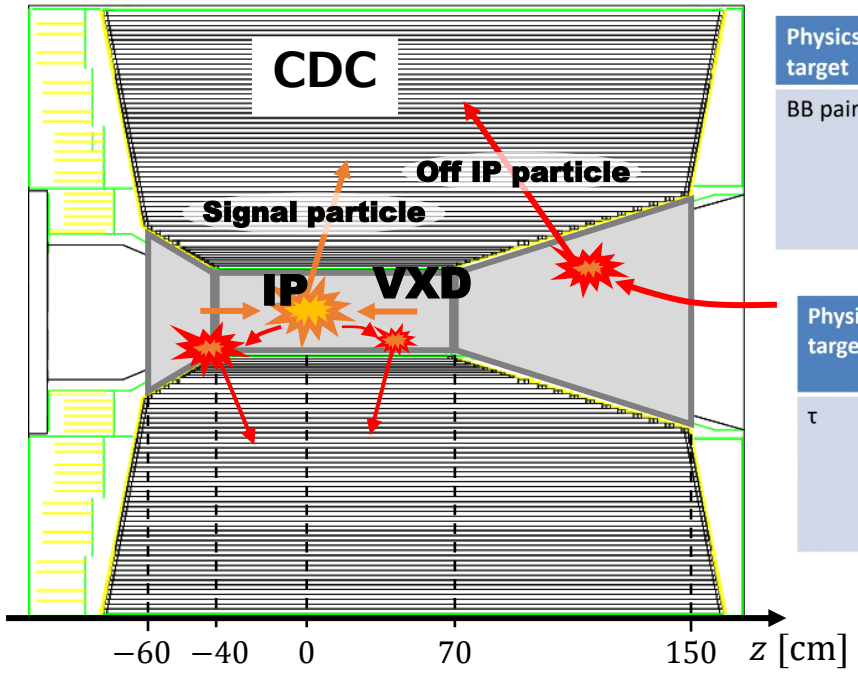
L1 rate will reach DAQ limit @ L ~ 10×10^{34} (with DAQ limit ~ 20kHz)
Reduction of L1 rate is needed

Category	Bit	Exclusive rate (kHz) @L=4.5e^{34}	Exclusive rate (kHz) @L=9e^{34}	Exclusive rate (kHz) @L=18e^{34}	Exclusive rate (kHz) @L=54e^{34}
CDC standard bits	ffy	1.8	3.6	7.2	21
	fyo	0.6	1.2	2.4	7
ECL standard bits	c4	0.26	0.5	1.0	3
	hie3	0.8	1.6	3.2	9
KLM τ/dark	klmb2b, eklmb2b, beklm cdcklm, ecleklm	0.23	0.23	0.23	0.23
		0.36	0.7	1.4	4
CDC τ/dark	stt	1.37	2.8	5.6	17
	syo	0.10	0.2	0.4	1
	fy30	0.18	0.4	0.8	2
Subtotal	**OR of above bits**	**5.7**	**11**	**22**	**66**
ECL τ/dark	lml	0.54	1.0	2.0	6
	eclmumu	0.51	1.0	2.0	6
Total	**OR of all bits**	**6.7**	**13**	**27**	**80**

T. Koga(KEK), 2022/7/21

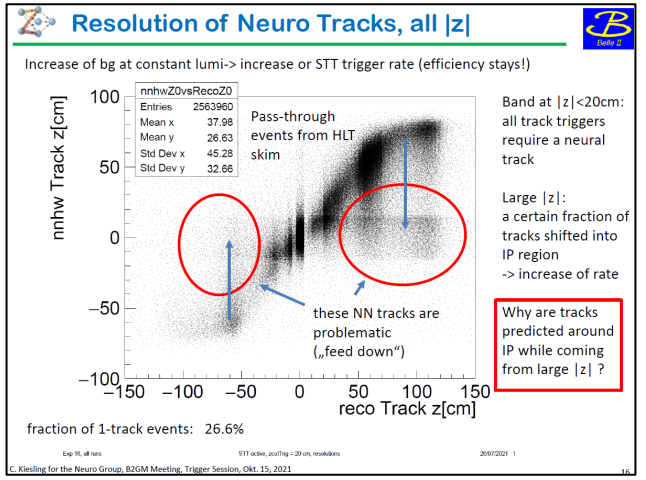
Motivation

- CDC trigger has highest trigger rate among sub-triggers of Belle II L1 trigger.
- Off IP particles are major beam-background source.
- CDC trigger rejects particles coming only from 15 or 20cm away from the IP.



Physics target	bit name	condition	Raw rate (kHz)	Exclusive rate (kHz)
BB pair	ffy	CDC #2track>=3, NNtrack>=1 with |z|<20cm >=1	1.40	1.40
	fyo	CDC #2track>=2, NNtrack>=1 with |z|<20cm >=1, Δϕ>90deg	1.03	0.47
			0.13	0.08
	c4	ECL #cluster>=4, 2<θid<15	0.69	0.56
	hie	ECL Energy sum>1GeV, 2<θid<15		

Physics target	bit name	condition	Raw rate (kHz)	Exclusive rate (kHz)
τ	stt	CDC #full track>=1, |z|<15cm, p>0.7GeV	1.74	0.96
	syo	CDC #full track>=1, |z|<15cm, #short track>=1, Δϕ>90deg.	0.74	0.38
	yioiecl1	CDC #full track>=1, |z|<15cm, #inner track>=1, Δϕ>90deg.	0.37	0.08
	lml12	NCL ≥ 3, at least 1 CL ≥ 500 MeV(Lab)) (with θID = 2 - 16)	0.17	0.03
	ecltaub2b	under optimization	-	-

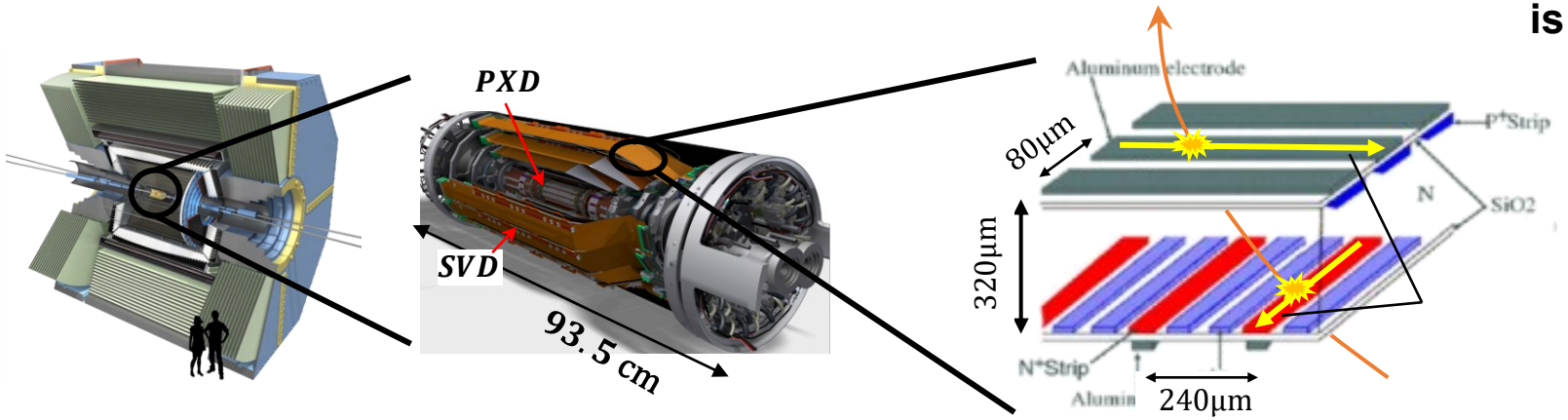


C. Kiesling, B2GM meeting, Oct 2021.

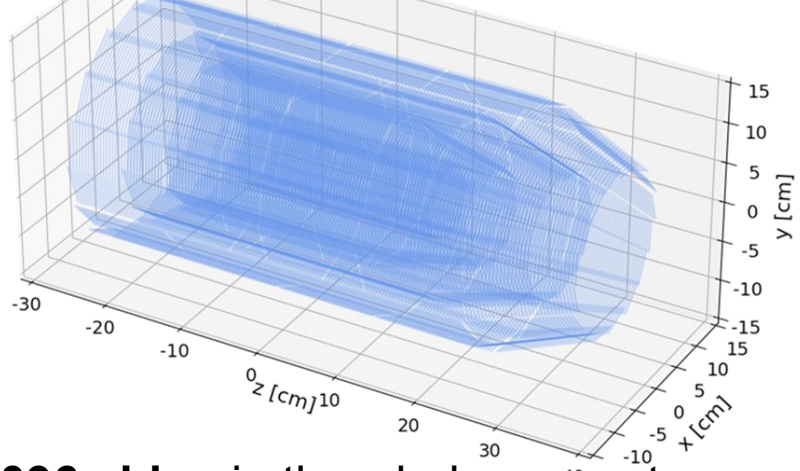
Since the z resolution of current CDC trigger is insufficient, there is room to improve the current L1 trigger

SVD

- the double-sided silicon-strip detector located in the innermost part of Belle II detector.
- detects the position through which the particle has passed.



For now, geometry of TFP-SVD is assumed to be the same as current SVD

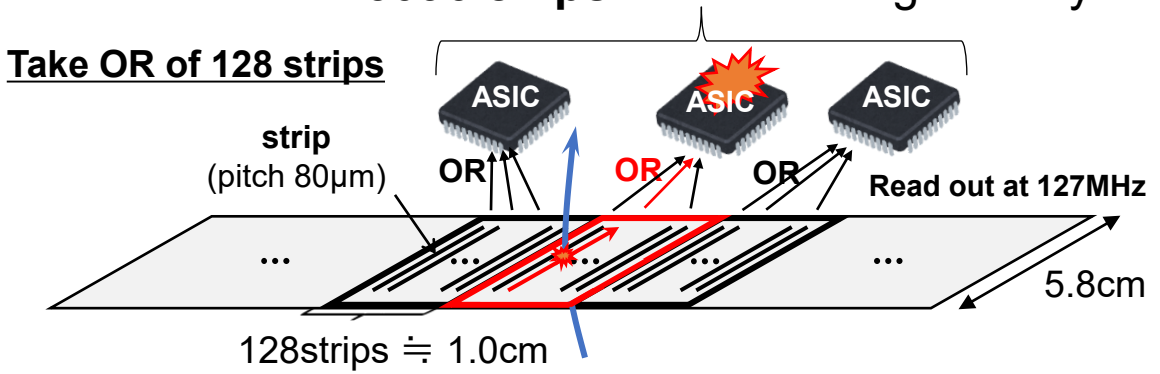


3096 chips in the whole geometry

Thin Fine-Pitch SVD (TFP-SVD)

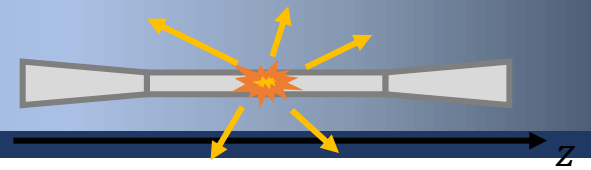
- We are developing new SVD to install after 2026.

	Current SVD	TFP-SVD
pitch of P side strip	75 μm	75 μm
pitch of N side strip	160 or 240 μm	80 μm
Sampling rate	32 MHz	127 MHz
Generate TRG signal	No	Yes



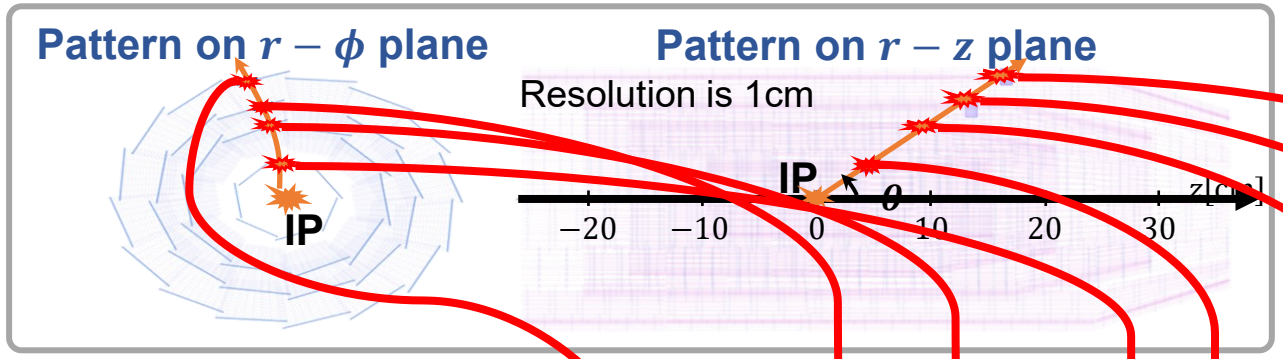
We are considering new L1 trigger using TFP-SVD

Development of core logic: Pattern table



Pattern matching by LOOK UP TABLE (LUT)

- Collect track patterns of particles from the IP.



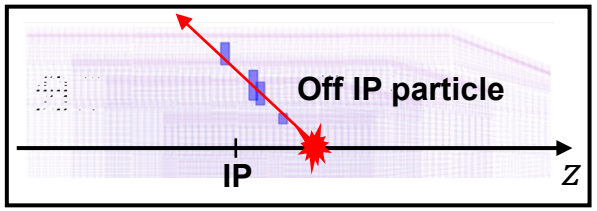
Encoded pattern table
[3096bits × 88,553]

Pattern 0: 100 ⋯ 001 ⋯ 010 ⋯ 001 ⋯ 100 ⋯ 010 ⋯ 100 ⋯ 001
Pattern 1: 100 ⋯ 010 ⋯ 100 ⋯ 100 ⋯ 010 ⋯ 010 ⋯ 010 ⋯ 100
⋮
Pattern 88552: 010 ⋯ 001 ⋯ 100 ⋯ 010 ⋯ 010 ⋯ 001 ⋯ 010 ⋯ 100

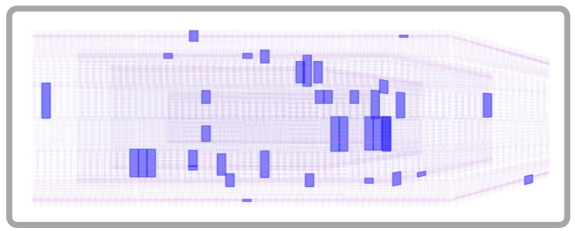
Conditions of particle generation for LUT

Parameter	Condition
Particle type	$\mu^{\pm}$
momentum p [GeV/c]	$0.2 \leq p \leq 3.0$
Production point z [cm]	$z = 0$

distinguish Off-IP track



- # of track pattern:88,553
- Each track is encoded in bit string with 3096-width



Online hits:

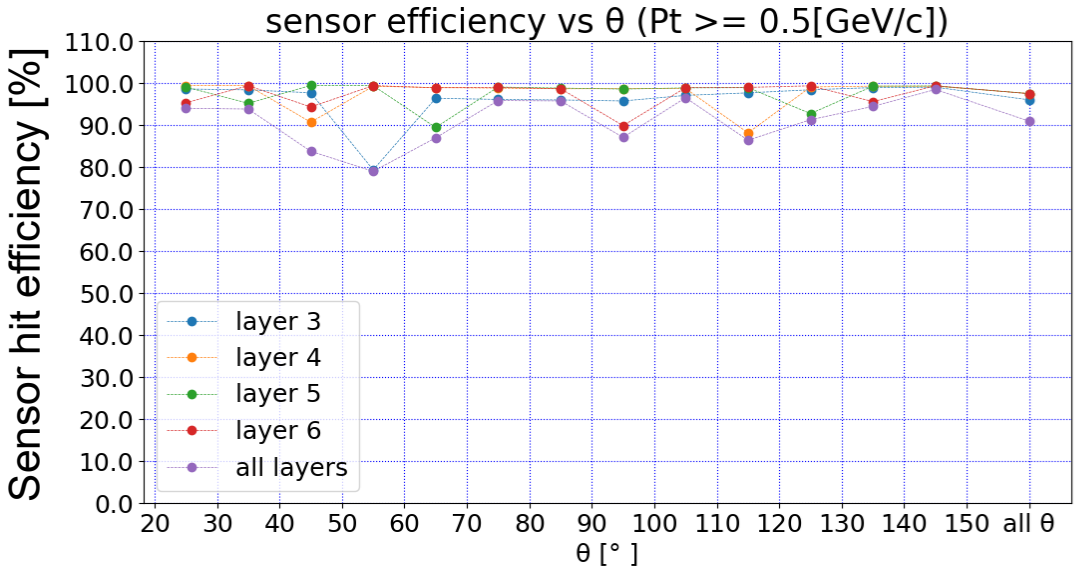
Compare online hits with the table

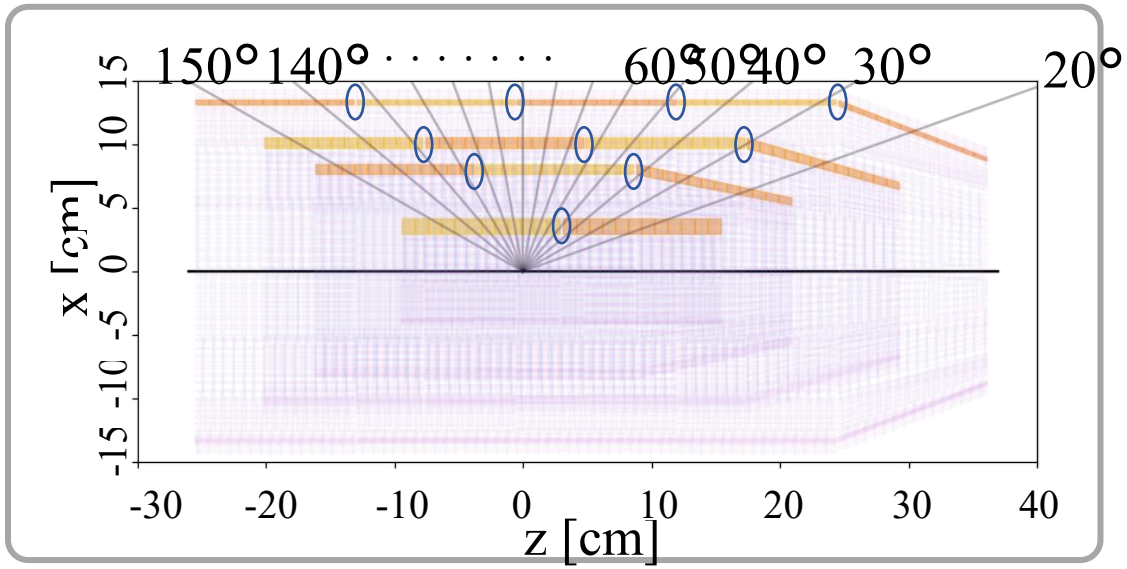
110 ⋯ 101 ⋯ 110 ⋯ 111 ⋯ 101 ⋯ 011 ⋯ 111 ⋯ 101

ex) this hits include the track pattern 0 of the table, and TFP-SVD trigger issue a trigger

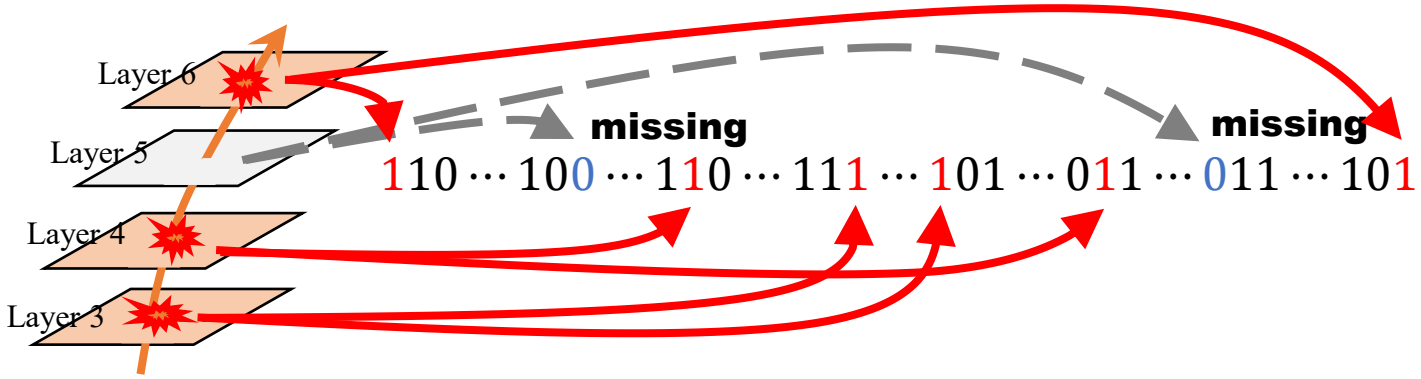
Modification of core logic

- There are sensor dead area at the edge of sensors.
- If a particle pass through the gaps, the track cannot be found by above algorithm → **trigger efficiency drops at the dead areas**





- For high trigger efficiency, matching condition is relaxed so that online hits can match the pattern table even if a particle doesn't hit any one of the four layers.



Implementation of logic on FPGA

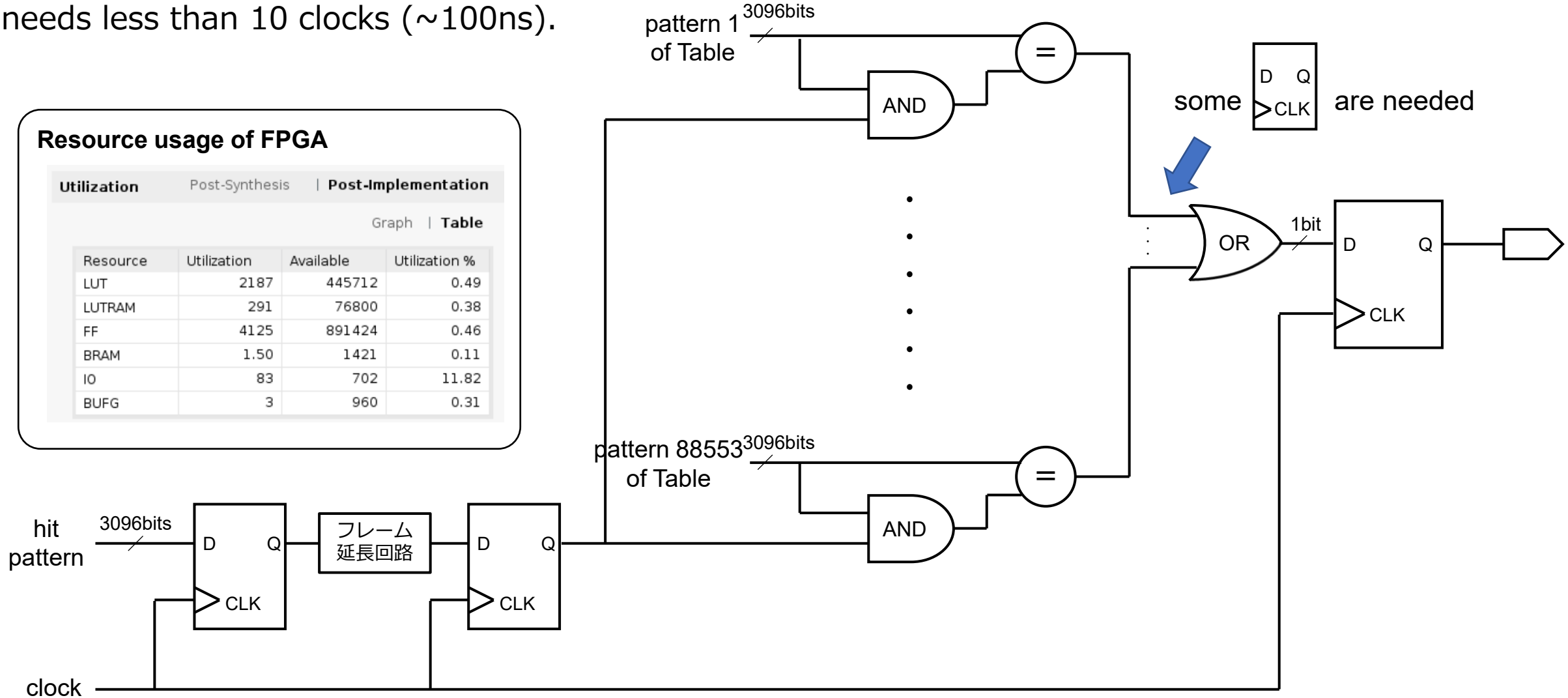
- We implemented core logic on FPGA
- 88553 patterns of the table are written in registers.
- It needs some flip flops to take the logical OR of results of 88553 equivalence operations → Core logic needs less than 10 clocks (~100ns).

Resource usage of FPGA

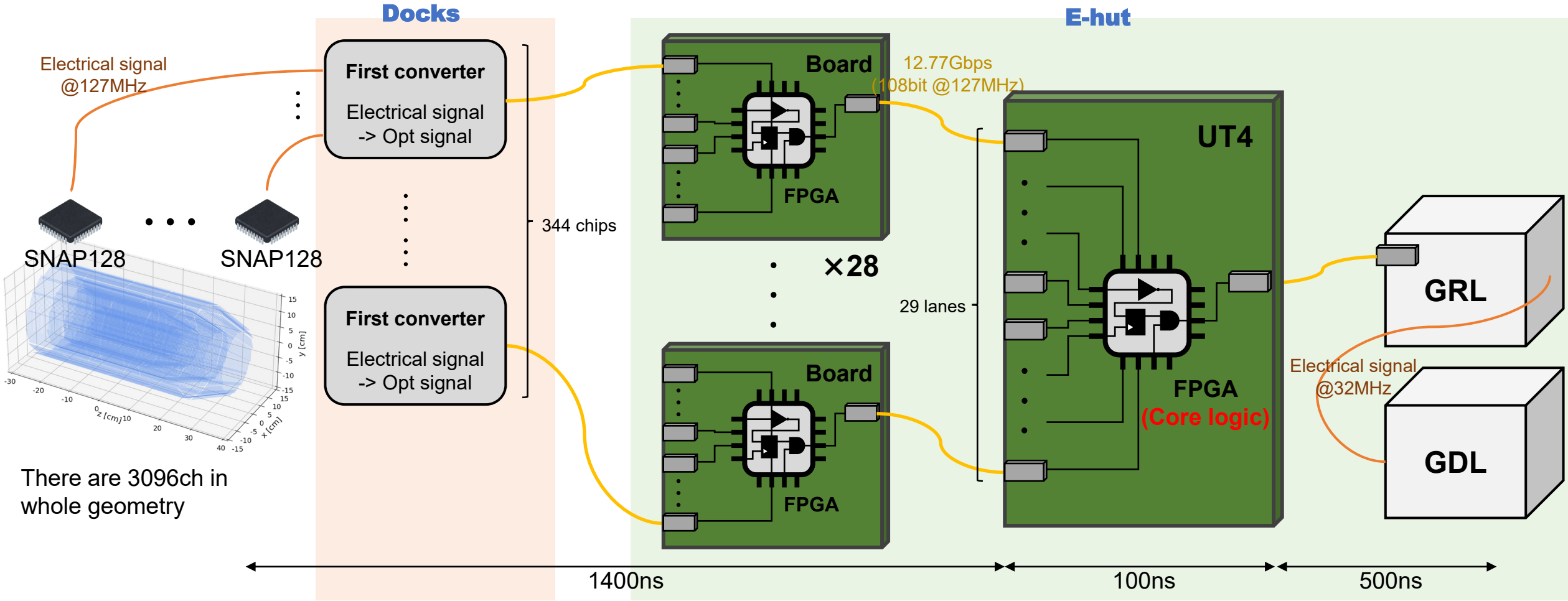
Utilization | Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	2187	445712	0.49
LUTRAM	291	76800	0.38
FF	4125	891424	0.46
BRAM	1.50	1421	0.11
IO	83	702	11.82
BUFG	3	960	0.31



Firmware setup



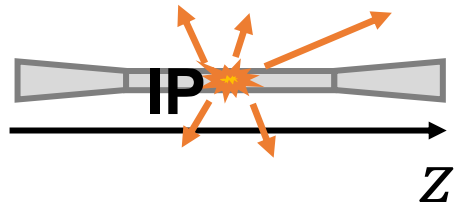
There are 3096ch in whole geometry

- We are assuming that it takes about 1400ns to convert electrical signals to optical signals and transmit the optical signal to UT4(core logic) via optical fiber cables .
- The core logic takes about 100ns (5% of total trigger latency).
- It takes about 500ns to transmit the TFP-SVD trigger output to GDL.
- After all, trigger latency to the GDL is about 2000ns(=1400+100+500).

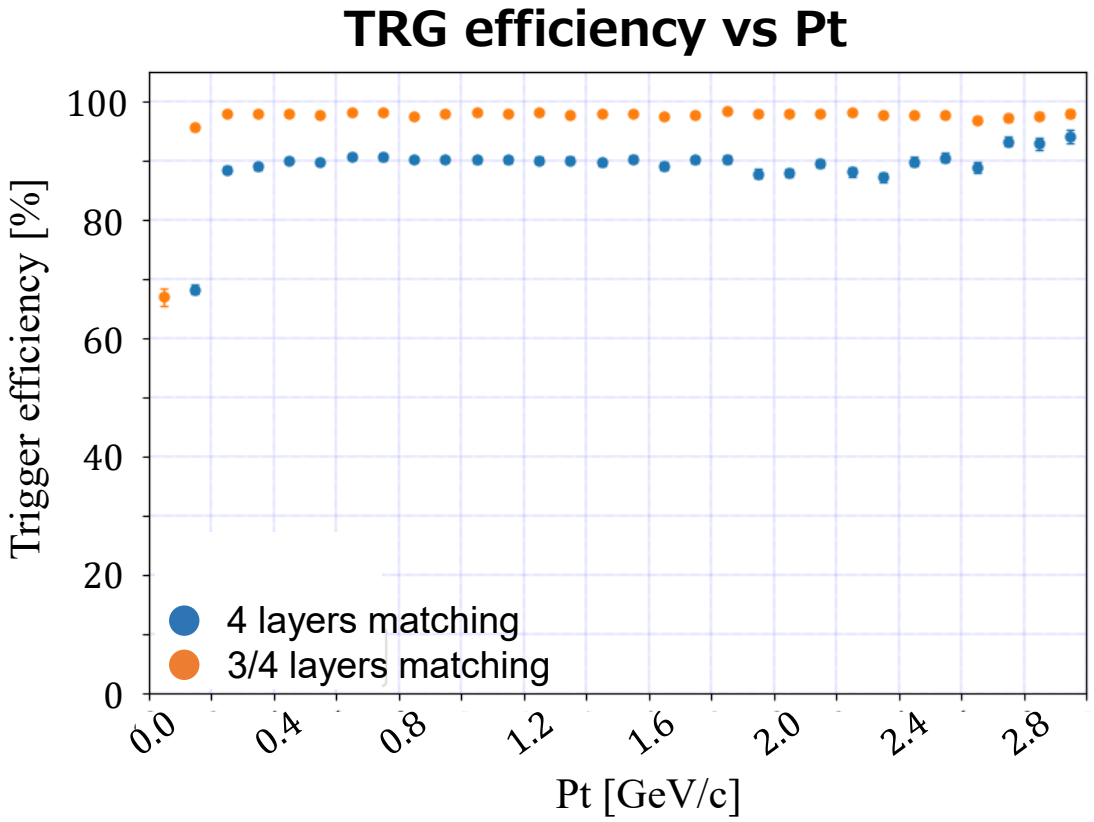
Performance on simulation: On-IP particle study

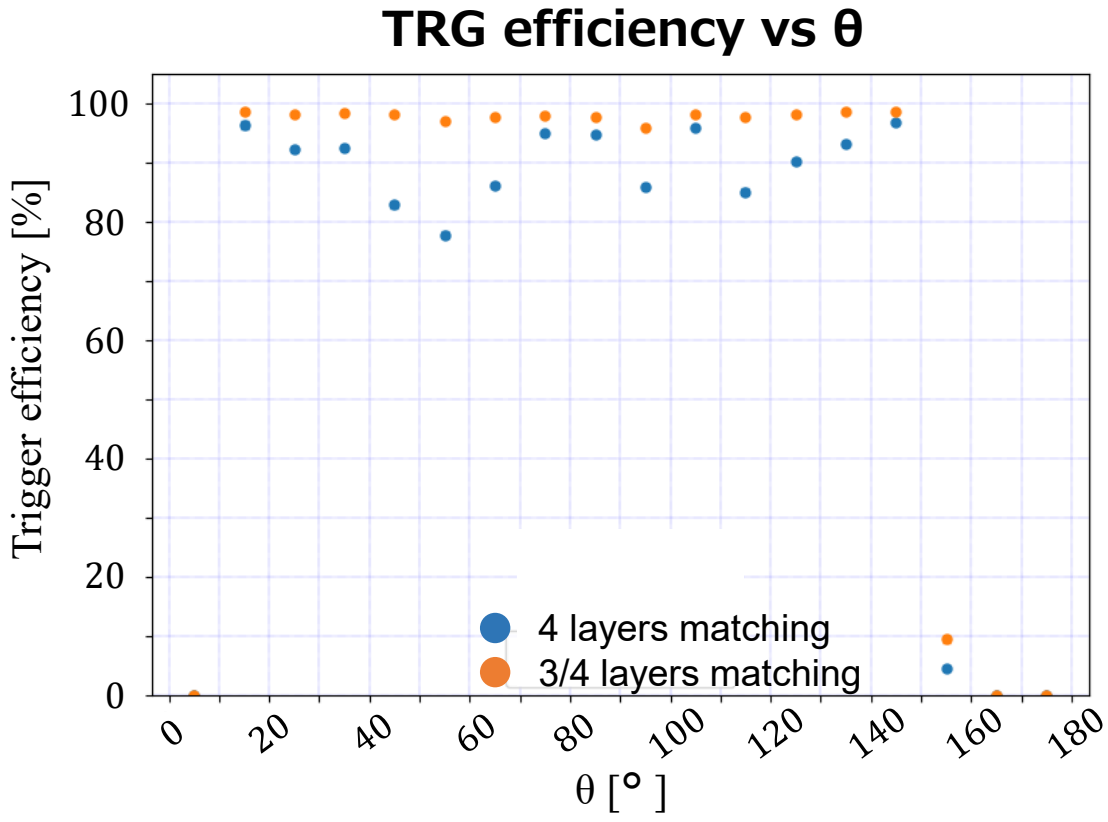
We generated only one particle at the IP and investigated trigger efficiency.

Blue (orange) plots represents trigger efficiency of 4 layers (3/4 layers) matching.



- is about 90% for all Pt.
- has dependency on θ. trigger efficiency drops where there are gaps.
- is about 98% for all Pt and θ. Relaxation of matching condition is effective against the existence of gap.

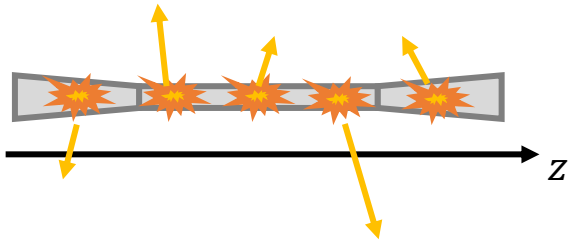


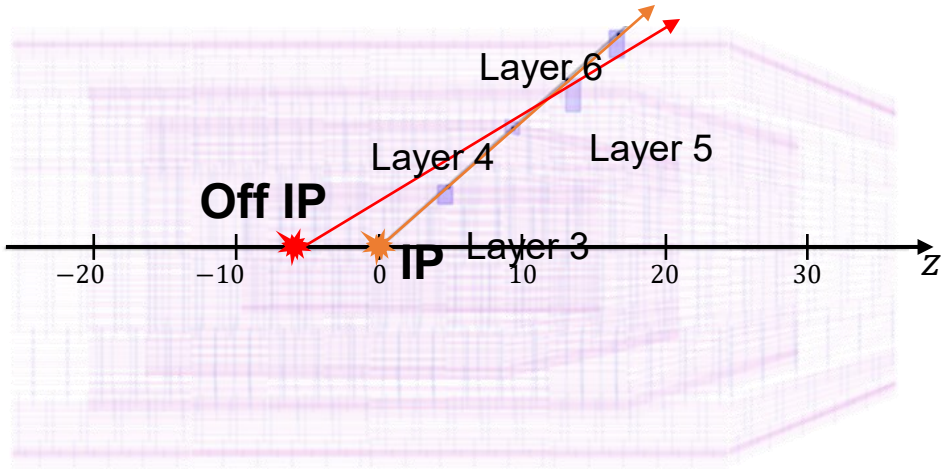


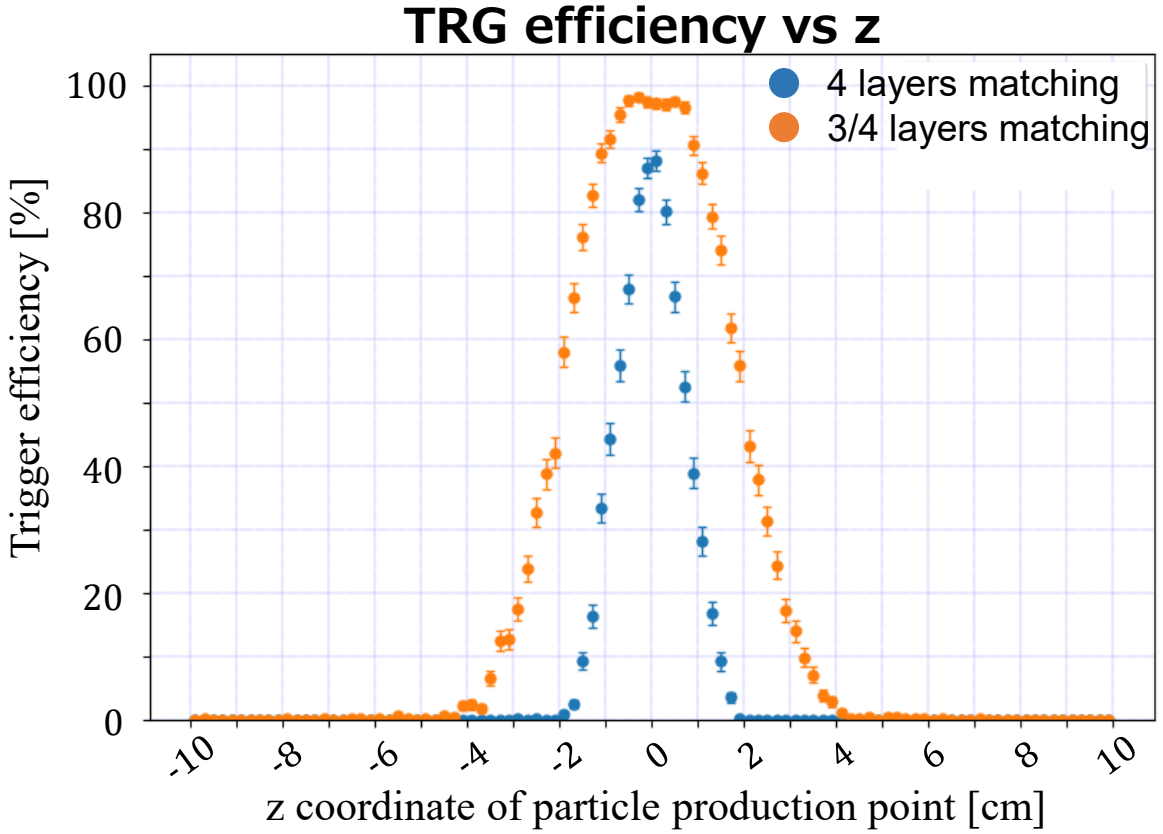
Performance on simulation: Off-IP particle study

To investigate Off-IP particle rejection power, we generated only one particle at various z.

- can reject particles generated at 2cm away from the IP with a probability of more than 99%.
- can reject particles generated at 4.5cm away from the IP with a probability of more than 99%.
- slow decrease in graph is due to relaxation of matching condition

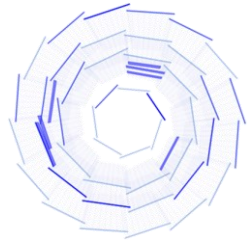


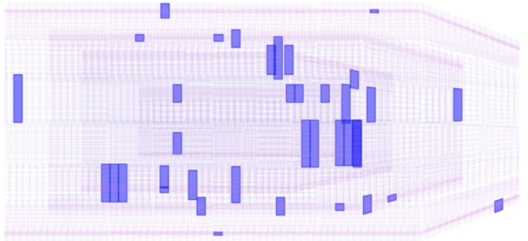




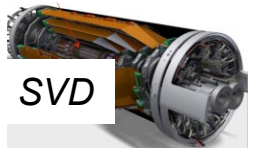
Result: Random BG study

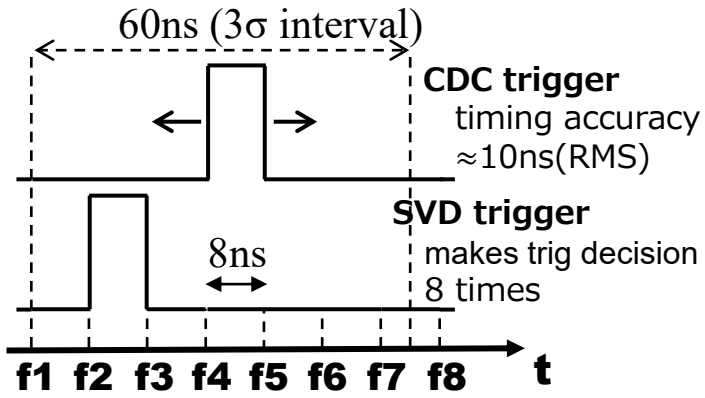
- BG particles with low momentum can make a lot of hits → we investigated fake trigger probability @ nominal L
- We considered two types of time scale
  - Sampling rate of ASIC of TFP-SVD: 8ns
  - Timing accuracy of CDC trigger: 60ns

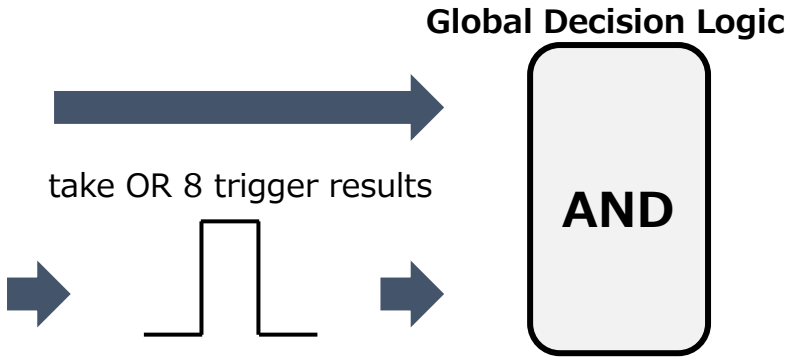




Taking AND with CDC trigger







- As shown in table below, fake trigger prob of 3/4 layers matching is high. Some countermeasures are needed.

TRG Prob

	4 layers matching	3/4 layers matching
8ns (per one frame)	0.67%	10.84%
60ns (taken OR of 8 frames)	2.44%	35.84%

Summary

- We considered firmware setup and developed core logic of TFP-SVD trigger.
- The total latency is about 2μs, and the latency of core logic is about 100ns(5%).
- Core logic can be implemented in one UT4 board.
- Trigger performance on simulation in shown table below.
- 3/4 layers matching algorithm with high trigger efficiency and sufficient Off-IP rejection power (current rejection area: large |z| > 15cm) is better.

Trigger performance on simulation

	4 layers matching	3/4 layers matching
Efficiency	90%	98%
Fake TRG prob under random BG (60ns)	2.44%	35.84%
Off IP rejection are	|z| > 2cm	|z| > 4.5cm

To Do

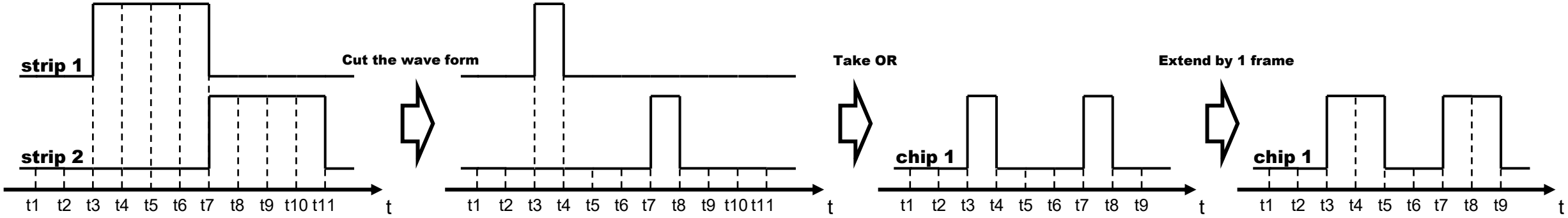
- For random BG, we will consider matching of TFP-SVD and CDC.
- We will calculate how much this TFP-SVD trigger improve trigger rate.

BACK UP

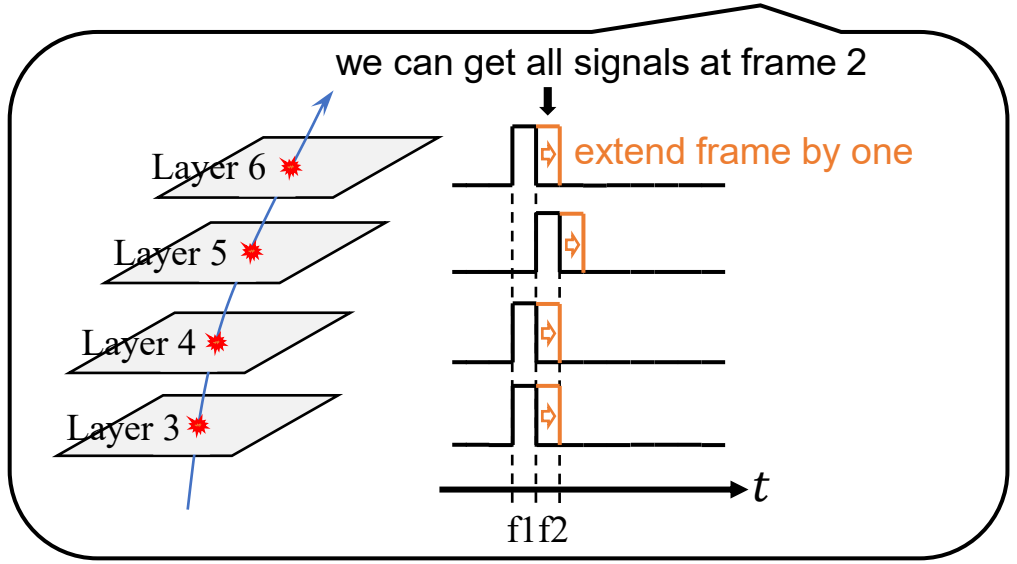
Wave form shaping

Read out by ASIC

- One ASIC of TFP-SVD(SNAP) will read out signals every about 8ns and will take OR.
- The timing of particle going through a sensor can be obtained from the rising edge of wave form.
- For that, before taking OR, we cut the waveform leaving rising edge.



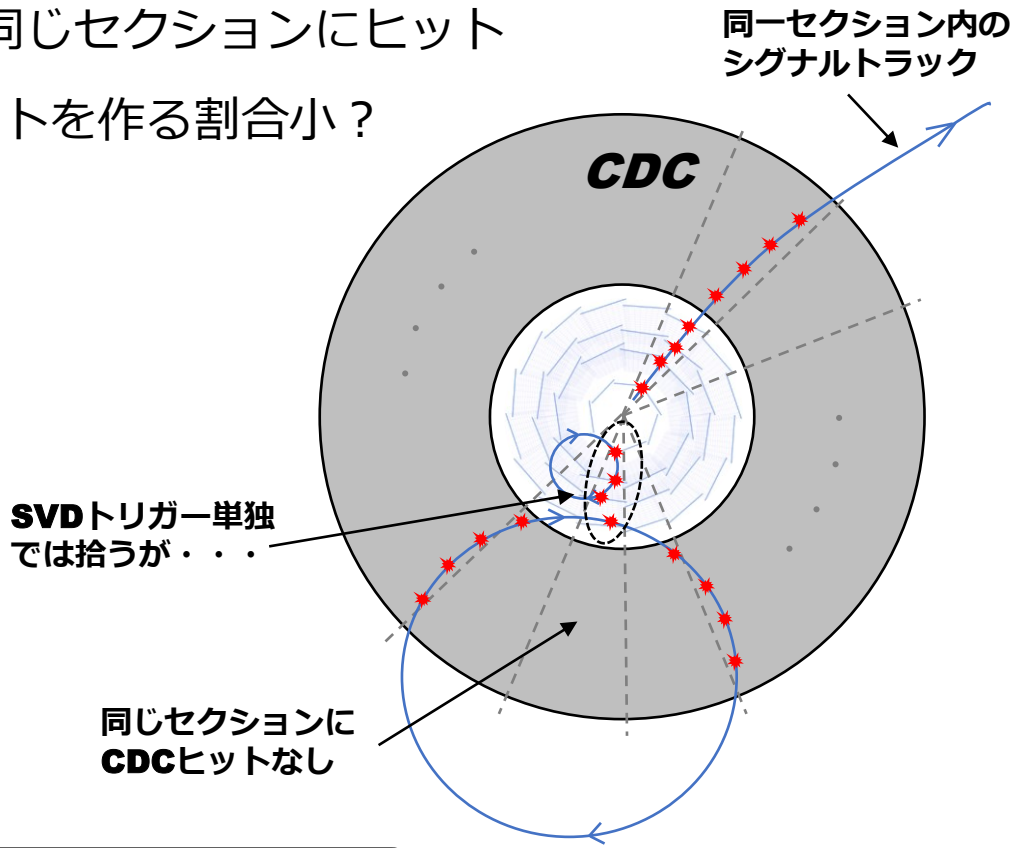
- However, the timing may be off by about one frame.
- In order not to miss a series of signals,
  we extended pulse rise frame by one.



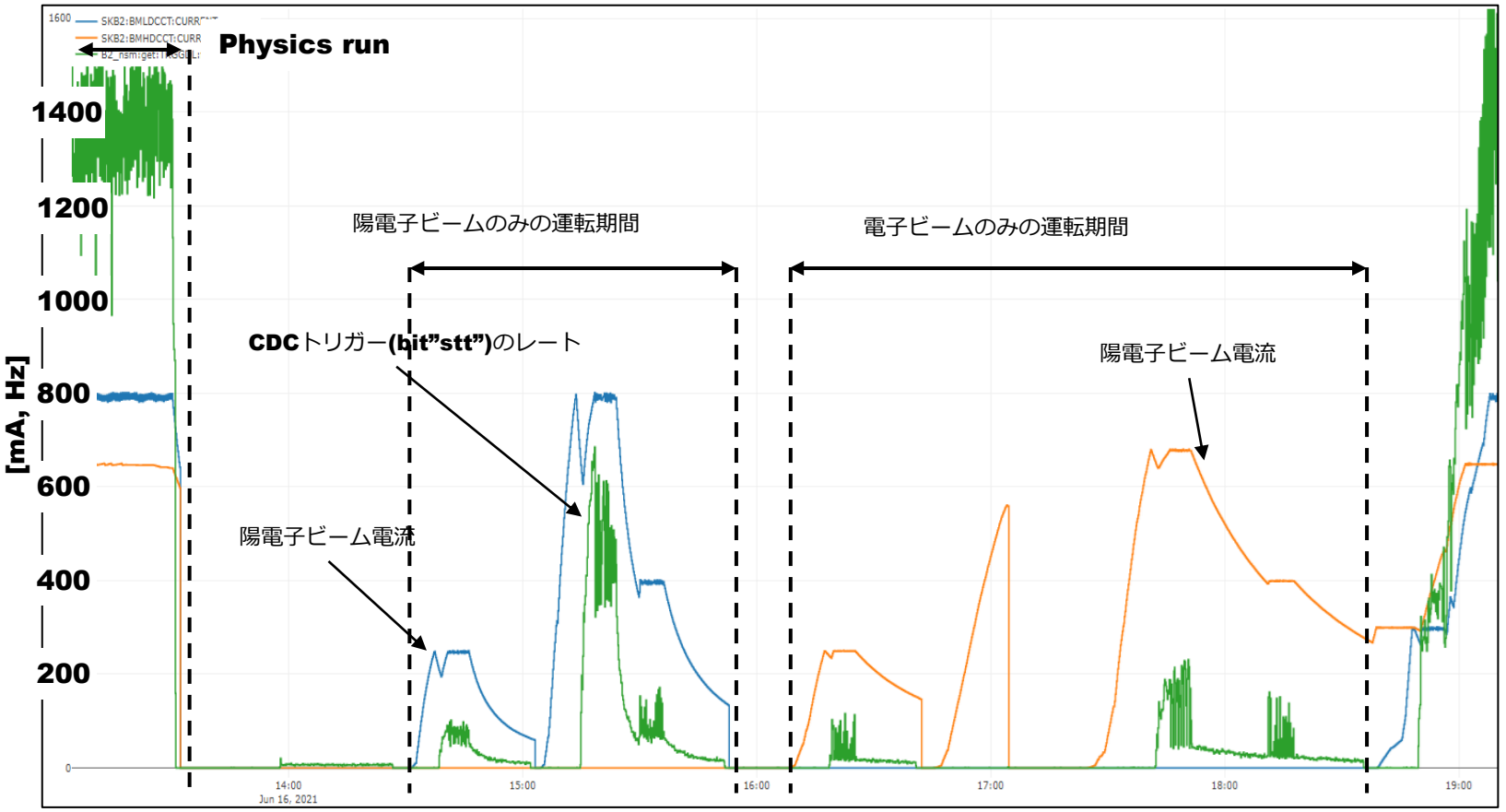
- ビームバックグラウンドはϕ方向ランダムにセンサーを鳴らすと考えられる.
- $r-\phi$平面で分割すると、、、

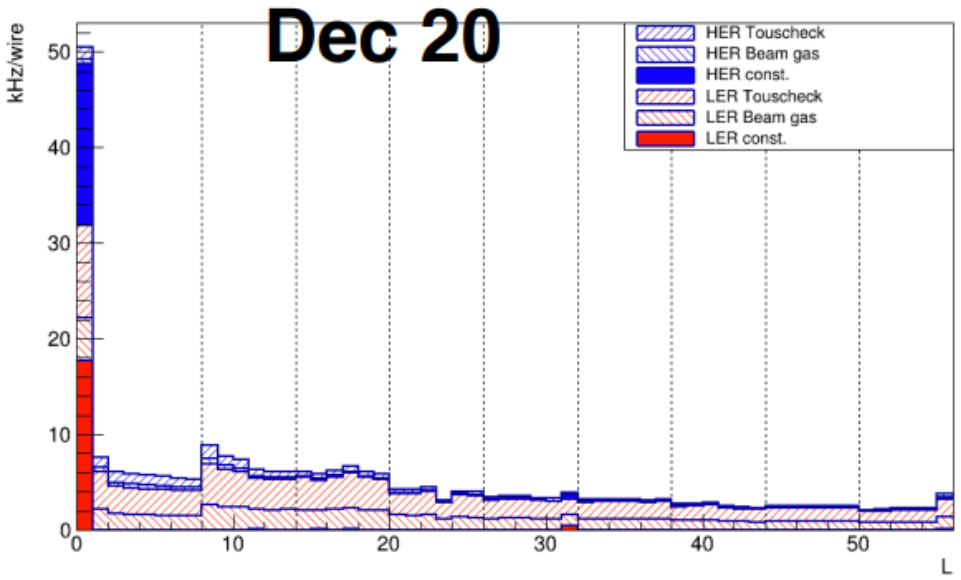
  IPから飛来するシグナル粒子は同じセクションにヒット

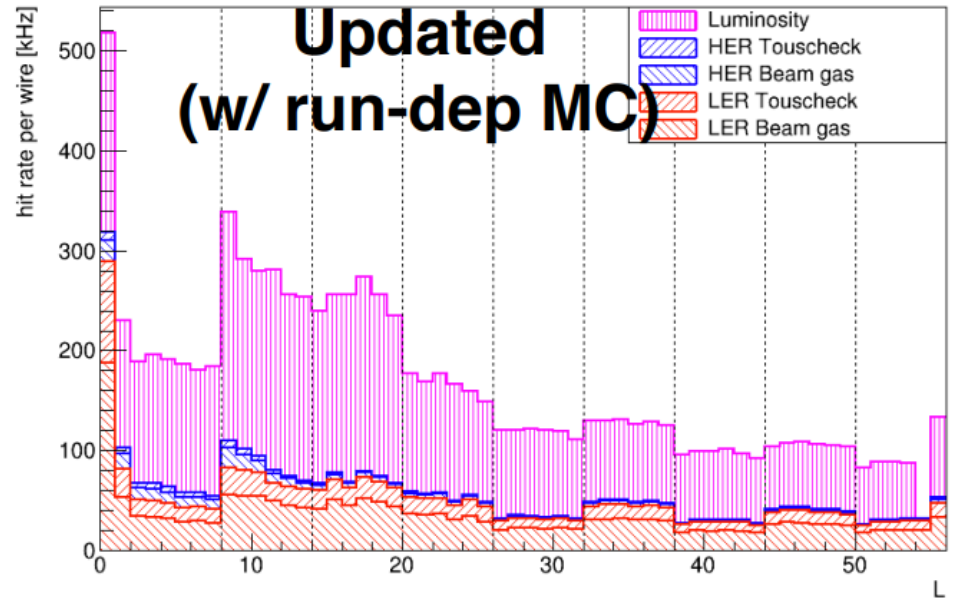
  BG粒子が同じセクションにヒットを作る割合小？



**CDCトリガーとϕマッチングを行うことで、
フェイクトリガー確率を減少させられるかも**

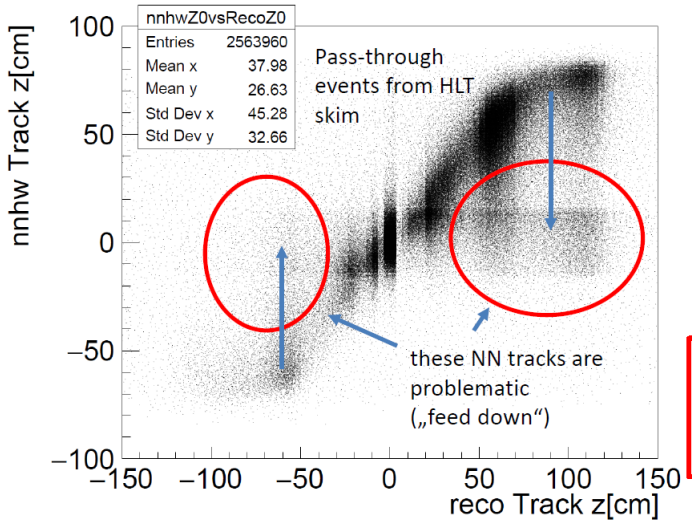

Physics run
陽電子ビームのみの運転期間
電子ビームのみの運転期間
CDCトリガー(hit"stt")のレート
陽電子ビーム電流
陽電子ビーム電流
[mA, Hz]
1600
1400
1200
1000
800
600
400
200
0
14:00
Jun 16, 2021
15:00
16:00
17:00
18:00
19:00


Dec 20
kHz/wire
HER Touscheck
HER Beam gas
HER const.
LER Touscheck
LER Beam gas
LER const.
0
10
20
30
40
50
L


Updated
(w/ run-dep MC)
hit rate per wire [kHz]
Luminosity
HER Touscheck
HER Beam gas
LER Touscheck
LER Beam gas
0
100
200
300
400
500
10
20
30
40
50
L

Resolution of Neuro Tracks, all |z|

Increase of bg at constant lumi-> increase or STT trigger rate (efficiency stays!)



Band at |z|<20cm: all track triggers require a neural track

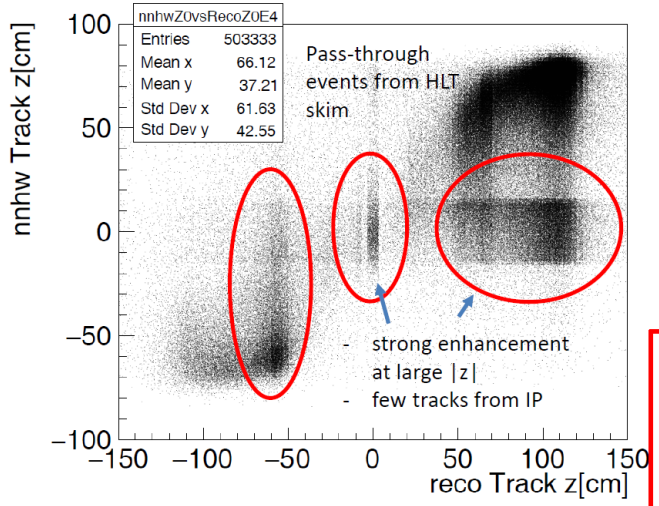
Large |z|: a certain fraction of tracks shifted into IP region -> increase of rate

Why are tracks predicted around IP while coming from large |z| ?

fraction of 1-track events: 26.6%

Large |z| Tracks: Expert 4 Network

Tracks from large |z| tend to miss the inner CDC layer („SL1“) -> „expert 4“ network



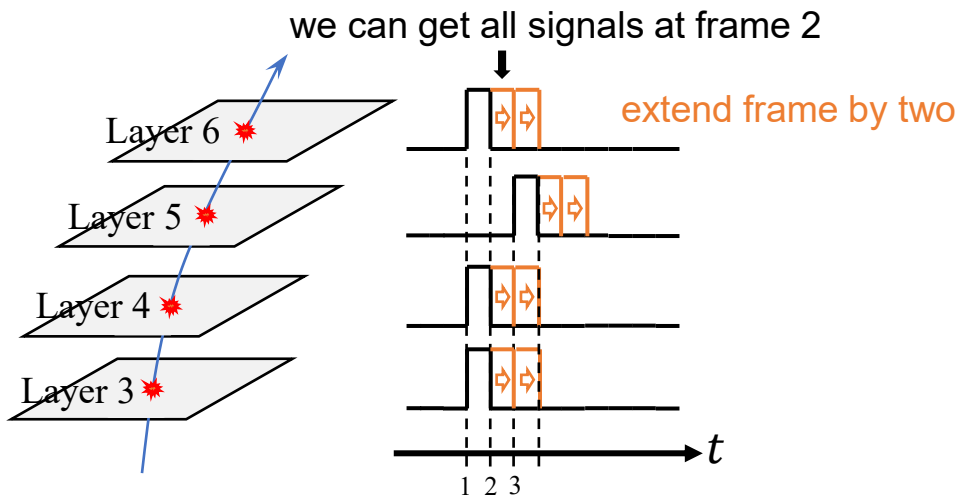
Plot: Neuro tracks selected which do not have inner stereo SL (SL1) hit (and also missed innermost axial SL0)

These tracks are dominantly coming from large |z|.

NN resolutions are about adequate

To-Do:
Feed-down must be reduced by improved training

Plot: reco tracks matched to neural tracks with missing stereo SL1


we can get all signals at frame 2
extend frame by two
Layer 6
Layer 5
Layer 4
Layer 3
t
1 2 3