GDL

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20221130@TRG/DAQ workshop

Transition to UT4

- UT3 (hx565t)
  - Resource > 70%
  - Tight timing score

	Strategy	Host	Output	Status	Timing Score	Run Time	LUTs	Slice Registers	WorstCaseSlack
☐	impTA	btrgpc08	run1	Done	177	03h 10m 05s	190,073 (53%)	132,484 (18%)	-0.115ns
☒	impTAJB2	btrgpc08	run2	Done	0	03h 10m 41s	190,367 (53%)	132,512 (18%)	0.006ns
☐	impTAJB3	btrgpc08	run3	Failed Par	None	08h 59m 29s	191,885 (54%)	132,964 (18%)	0.004ns
☐	impTAJB5	btrgpc08	run4	Done	177	03h 19m 49s	190,073 (53%)	132,484 (18%)	-0.115ns
☐	impTAJB6	btrgpc08	run5	Done	2228	03h 36m 42s	172,092 (48%)	132,478 (18%)	-2.029ns
☐	impTAJB7	btrgpc08	run6	Done	177	03h 17m 37s	190,073 (53%)	132,484 (18%)	-0.115ns
☐	impTAJB8	btrgpc08	run7	Done	213466	03h 30m 40s	190,534 (53%)	132,483 (18%)	-2.944ns
☐	impTAJB2CT2	btrgpc08	run8	Failed Par	None	05h 25m 26s	189,691 (53%)	132,512 (18%)	3.045ns
☐	impTAJB2CT3	btrgpc08	run9	Done	736	03h 11m 58s	190,647 (53%)	132,513 (18%)	-0.323ns
☐	impTAJB2CT4	btrgpc08	run10	Failed Par	None	05h 02m 38s	189,503 (53%)	132,513 (18%)	-3.978ns
☐	impTAJB2CT5	btrgpc08	run11	Done	0	03h 07m 08s	189,578 (53%)	132,513 (18%)	0.016ns
☐	impTAJB2CT6	btrgpc08	run12	Done	0	03h 02m 48s	190,228 (53%)	132,512 (18%)	0.005ns
☐	impTAJB2CT7	btrgpc08	run13	Done	244	03h 05m 34s	190,019 (53%)	132,512 (18%)	-0.148ns
☐	impTAJB2CT8	btrgpc08	run14	Done	0	02h 40m 21s	190,175 (53%)	132,512 (18%)	0.005ns
☐	impTAJB2CT9	btrgpc08	run15	Failed	None	00h 00m 04s	None	None	None
☐	impTAJB2CT10	btrgpc08	run16	Failed	None	00h 00m 04s	None	None	None
☐	impTAJB2CT11	btrgpc08	run17	Failed	None	00h 00m 04s	None	None	None
☐	impTAJB2CT12	btrgpc08	run18	Failed	None	00h 00m 04s	None	None	None
☐	impTAJB2CT13	btrgpc08	run19	Failed	None	00h 00m 04s	None	None	None
☐	impTAJB2CT14	btrgpc08	run20	Failed	None	00h 00m 04s	None	None	None

Optical Links

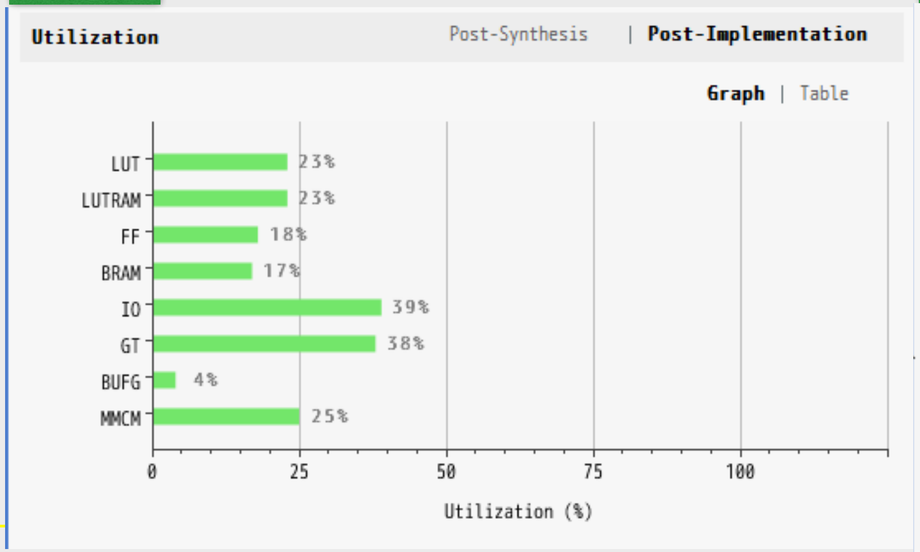
	UT4	dclk MHz	GB/s	FIFO	data
GRL	GTY0	127	8	126x4	42x4
KLM	GTY1	127	8	126x4	42x4
ETM	GTY4	8	8	16x1	256x1
ETF	GTY5	32	12	126x4	42x4
TOP	GTH1	127	5	16x4	32x4
B2L	GTH7		2.5		

Compile

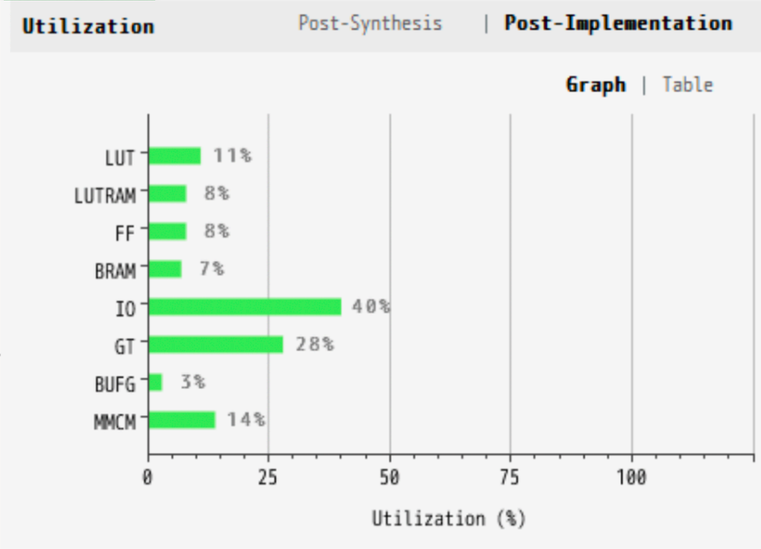
- Both vu080 and vu160 Tested
- Difference:
  - IO bank number for *set_property INTERNAL_VREF 0.6* in UT4_Main_GLOBAL.xdc
  - *set_properly LOC gen_ictrl1.map_ic* (vu160 only)

- No timing errors
  - MVSYSCLK, clk50m, clk20m are ignored (set_false_path). Is this OK?
  - set_false_path -through [get_nets map_b2l/map_b2tt/gen_useextclk0.map_clk/clr_ictrl_reg_n_0]
  - Resource usage of vu160 is less than half of vu080.

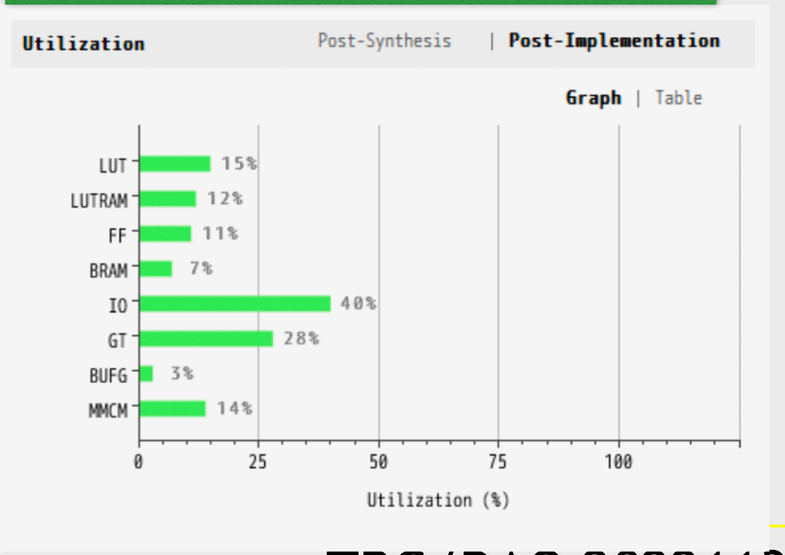
vu080



vu160



vu160 with alive rate scalers on



ftdl v46

- https://confluence.desy.de/pages/viewpage.action?pageId=75106458

- LVDS 4 ports (UT3) -> 2 ports (UT4)

  - 32 bit for 1 port
  - All GRL signals (CDCTRG, matching) via LVDS due to limited latency.
  - UT3 (4 LVDS ports)
    - 3 for GRL, 1 for ETF for future modification.
  - UT4 (2 LVDS ports)
    - 2 for GRL

  - Removed bits:
    Input: s2fo, s2f3, s2f5, s2so, s2s3, s2s5, grlgg1, grlgg2, bwdsb, fwdsb, bwdnb, fwdnb,
    brlnb1, brlnb2, brlfb1, brlfb2, ieklm
    Output: fso(0), syo(1), syoecl(0),

- New input bits
  - tx_3 “pulse of # of NN veto cut track > 3”

- New output bits
  - tx3 <= tx and !injection

To Do: Firmware modification for new LVDS

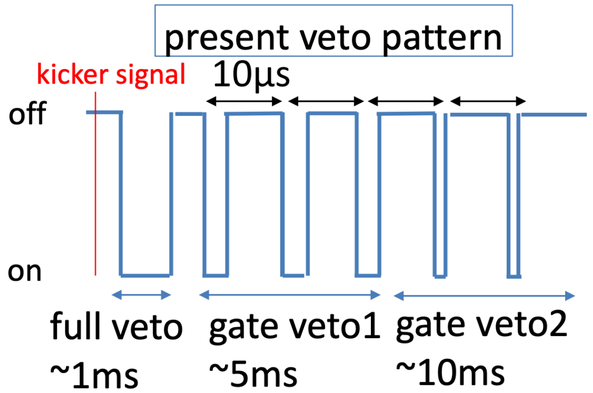
- On UT3, all 4 LVDS ports were fully used to receive signals from GRL
  - LVDS 4 ports (UT3) -> 2 ports (UT4)
    - On UT4, monitoring bits are temporarily removed.

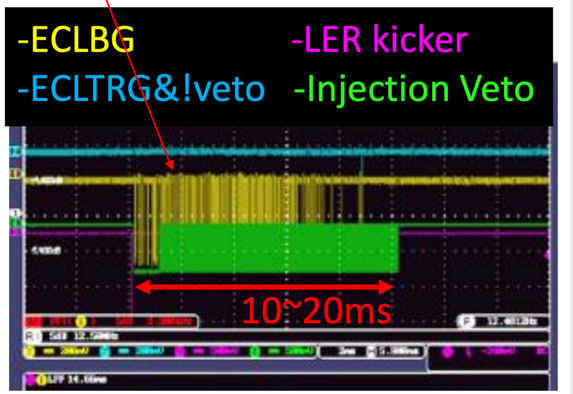
- New LVDS extension board being developed
  - but between LVDS and FPGA is limited, so need to switch port when receiving signal.
  - Will start modification when the new board at hand.

To do: Modification of Inejection veto

- BG duration is longer than expected, > 10ms.
- Injection Frequency in exp26 is 25Hz=40ms.
  => overlap will occur at 50Hz.
- Present one cannot accept next injection signal if it comes before completion of prior veto process.
- Modification
  - Simply instantiate injection veto component for the 2nd injection, and take OR over the 2 veto signals.
  - 2 components enough? Pipelined ?

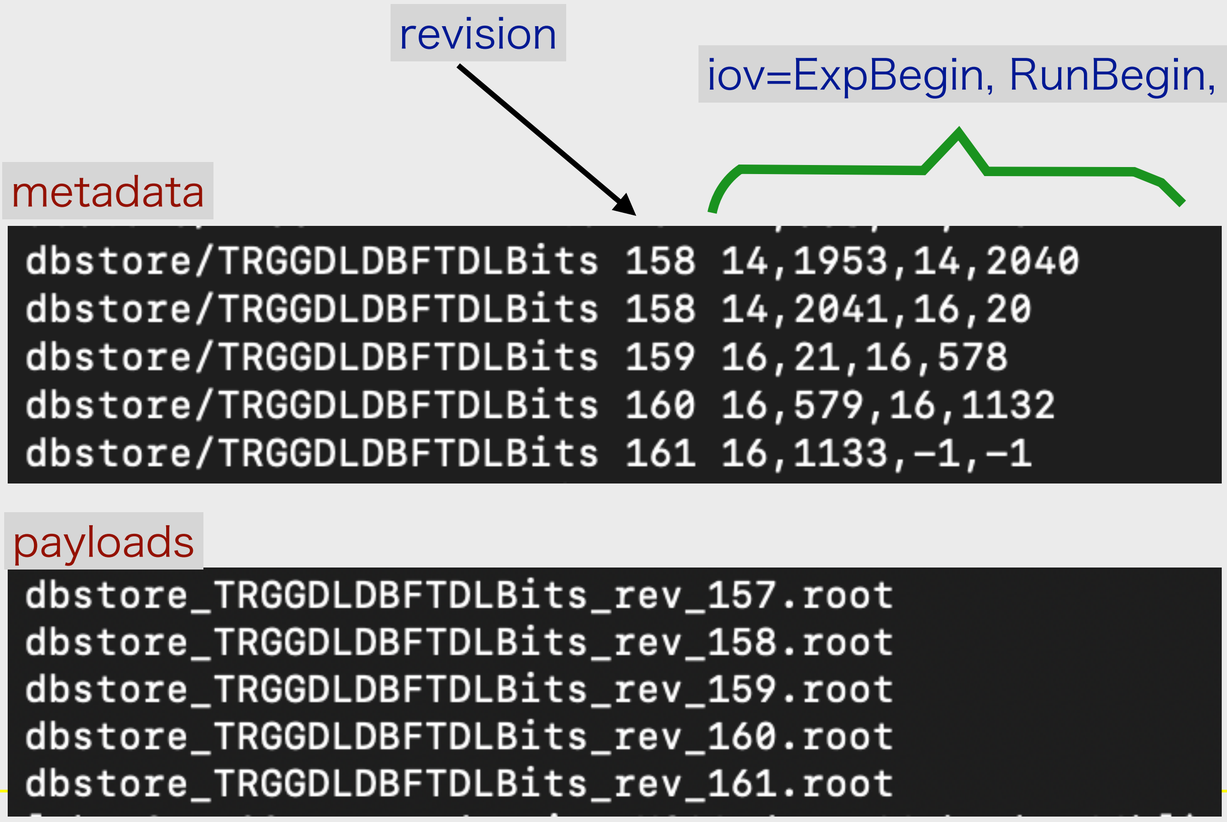
-It was not expected that BG duration continues more than 10ms
(At belle, it was ~3ms.)





Automation of GDL payload production

- Payload: data in database. Collected from all subsystems as Global tag.
  - Used to analyze experiment data and to generate MC samples.
  - Root file (TObject with only data, getter, and setter) for specific Exp/Run period, and metadata for Exp/Run dependence, iov (interval or validity).



	data
TRGGDLDBUnpacker	Valuable names, positions in rawdata
TRGGDLDBInputBits	Bit names, positions
TRGGDLDBFTDLBits	Bit names, positions
TRGGDLPrescales	Prescales
TRGGDLDBAlgs	Logics

Automation of GDL payload production

- Payloads are generated by basf2 module, trg/gdl/tools/trggdlWriteLocalDB.cc, in which parameter values are hard coded by hand.
  - Wrong values were set several times.

- Automation: Log => Data files => trggdlWriteLocaldb command => payloads

  - Generate data files using script
    - Data = When (Exp/Run) the config changed and updated values.
    - Fetch values from trggdld (nsm daemon) log
      - In condition database, sometimes recoding were failed.
      - Frequency of failed recording is less than configuration database.
    - Logics are taken from VHDL code
      - VHDL code must follow some rule so the script can extract logic.
      - Converted to C++ style. Used in Tsim.

  - trggdlWriteLocalDB.cc reads data files and generate payloads.
    - No need to touch trggdlWriteDB.cc any more.

  - Successfully working for latest payloads.
    - Generating payloads from beginning (exp7) with this new package.
    - PR

Hard coded vals in trggdlWriteLocalDB.cc

```
    // 60: e22r372  ecltaub2b(175) and ecltaub2b2(3) 0->1
    {100, 100, 100, 1, 100, 1000, 0, 0, 1, 0, 0, 2000, 0, 400, 0, 0, 0
, 0, 1, 100, 0, 1, 1, 0, 0, 0, 1, 1, 1, 0, 0, 1, 0, 10, 2, 1, 100, 10,
1, 20000, 4000, 0, 500, 0, 0, 0, 0, 0, 0, 50, 50, 0, 0, 8000, 0, 0, 0,
    // 61: e22r381  ecltaub2b(175) and ecltaub2b2(3) 1->0
    {100, 100, 100, 0, 100, 1000, 0, 0, 1, 0, 0, 2000, 0, 400, 0, 0, 0
, 0, 1, 100, 0, 1, 1, 0, 0, 0, 1, 1, 1, 0, 0, 1, 0, 10, 2, 1, 100, 10,
1, 20000, 4000, 0, 500, 0, 0, 0, 0, 0, 0, 50, 50, 0, 0, 8000, 0, 0, 0,
    // 62: e24r1  2022a. elog/TRG+operation/869
    {0, 0, 0, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0,
, 0, 0, 1, 0, 10, 2, 1, 100, 10, 100, 1, 1, 1, 1, 1, 1, 10, 1, 1, 0, 0
0, 0, 8000, 0, 0, 0, 0, 8000, 0, 0, 50, 0, 0, 0, 0, 0, 1, 0, 0, 0, 0}
```

Logic in VHDL

```
fff <= '1' when (t2(2)='1' or t2(3)='1') and veto='0' else '0';
```

Logic in C++

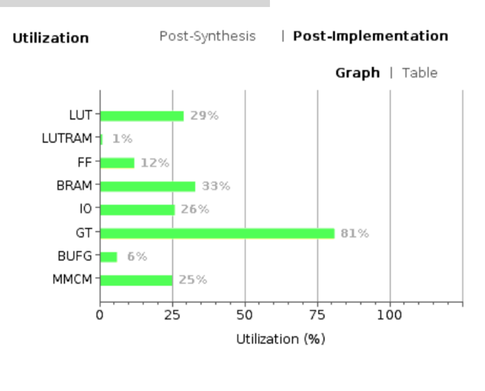
```
10 !105 + 11 !105
```

Unification of GDL and GRL ?

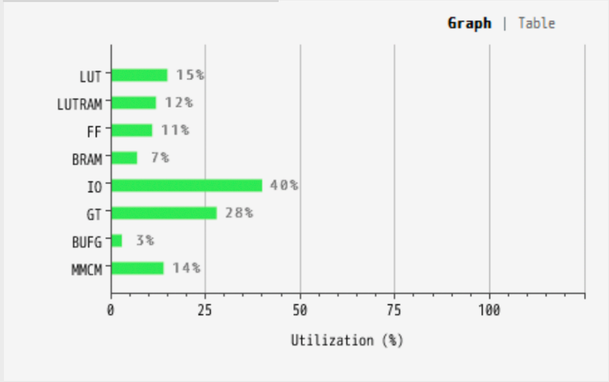
- Resource and connections look OK.
- Pros
  - Latency reduction. No need to use LVDS.
  - Down sizing, anyway. One free vu080, free slot in vme18.
- Cons
  - ETM, TOP and KLM data unified ? Bandwidth OK?
  - Less spare resource for future improvement
  - Need 2 B2L lines?
  - There should be some difficulty beyond simple sum of resource consumption. SLR problem ?
  - No strong motivation.

	GDL	GRL
GTH0		2D
GTH1	TOP	3D
GTH2		NN
GTH3		ETM
GTH4		KLM
GTH5		GDL
GTH6		
GTH7	B2L	B2L?
GTY0	GRL	
GTY1	KLM	TOP
GTY2		TSF0
GTY3		TSF2
GTY4	ETM	TSF4
GTY5	ETF	TSF1
GTY6		TSF3
GTY7		

GRL on vu080



GDL on vu160



Status and Summary

- Transition to UT4
  - ECLTRG signals seen.
    - GTH (UT3) -> GTY (UT4)
    - Consistent rates with ETM
    - ecl-ing=1 (~3 for UT3)
      - Arrival timing can be delayed by 1 127m clock.
  - B2L readout OK (vu160 not yet tested) on testbench
    - Data quality is not checked yet
  - Need to test other connections
    - Link to KLM and TOP up
    - Link to ETF (only 12g) and GRL (same config with KLM) down.
  - Will use vu160 unless urgent need of vu160 from other module.
- A package for GDL payload production made and being tested with entire Exp/Run data.
- To do during LS1.
  - Finalize UT4 transition
  - Modification of injection veto
  - Modification of LVDS connection