GRL status and plan
2022/11/23
T.Koga

GRL status and plan in LS1

-Hardware transition of UT3→UT4, LVDS extended UT4

-CDC-TOP matching

-Neural network implementation

-Short tracking upgrade (Yun-Tsung's talk)

GRL UT4 commissioning status

-Report at last B2GM (in backup)

-GRL is updated with UT4 VU080, same core logic with UT3

- -UT4 installed to vmetrg18.
  reconnect optical cables from UT3 GRL.
- -named “grl2” on btrgsrv0 temporary
- -UT3 GRL is still kept in Ehut.

-Commissioning is done with cosmic

- -Trigger rate is consistent with UT3
- -DQM is consistent with UT3
- -Stable link

-Remained Tasks:

- -Need to check with UT4 GDL
- -Need to check more bits with KLM and TOP ON
- -Update of optical transceiver speed

UT4GRL task: transceiver speed

-Transceiver speed can be increased for UT4 of 2D, ETM, GDL, TOP, TSF

-latency should be reduced (bandwidth should be increased too)

-GTY 12Gbps has been operated stably in 2022ab, TSF->2D.
New trial for GTH.

-I would like to update them during LS1.
Can Nakazawa-san, Unno-san, and Tianping help to modify your FW at January, when Ehut will be ON at next time?

GTY	Module	speed (Gbps)	encode/ decode	GTH	Module	speed (Gbps)	encode/ decode
GTY0	2D (Koga)	5.5->12	64b66b	GTH0	TOP1(Tianping)	5.0->12	8b10b->64b66b
GTY1	3D	5.5	64b66b	GTH1	TOP2(Tianping)	5.0->12	8b10b->64b66b
GTY2	NN	5.5	64b66b	GTH2	TSF0(Koga)	5.0->12	8b10b->64b66b
GTY3	ETM (Unno)	5.5->12	64b66b	GTH3	TSF2(Koga)	5.0->12	8b10b->64b66b
GTY4	KLM	5.5	64b66b	GTH4	TSF4(Koga)	5.0->12	8b10b->64b66b
GTY5	GDL (Nakazawa)	5.5->12	64b66b	GTH5	TSF1(Koga)	5.0->12	8b10b->64b66b
GTY6	--			GTH6	TSF3(Koga)	5.0->12	8b10b->64b66b
GTY7	--			GTH7	B2L		

UT4GRL task: new bit map GRL->GDL with LVDS

-Because the number of LVDS port is 2(4) with UT4(UT3), need to reduce the number of bits. Now keep old bitmap without LVDS_C.

-New bit map: https://confluence.desy.de/pages/viewpage.action?pageId=75106458

-Rate etc. should be checked with UT4 GDL.

LVDS	bit position		content
A	0	iecl_1	#TSF0.1.2-Endcap ECL matching>1
A	1		cluster_b2b_1to5
A	2		trkcluster_b2b_1to5
A	3		samehem
A	4		opphem
A	5		pulse of # of matched clusters (2D-ECL) = 1
A	6		pulse of # of matched clusters (2D-ECL) = 2
A	7		pulse of # of matched clusters (2D-ECL) = 3
A	8		pulse of # of matched clusters (2D-ECL) > 3
A	9		pulse of # of matched 2GeV clusters (2D-ECL) = 1
A	10		pulse of # of matched 2GeV clusters (2D-ECL) = 2
A	11		b2b_1to7: Opening angle of 2 tracks from 140 to 180
A	12		cdc_open90
A	13		pulse of # of matched TOP slots (2D-TOP) = 1
A	14		pulse of # of matched TOP slots (2D-TOP) = 2
A	15		pulse of # of matched TOP slots (2D-TOP) = 3
A	16		pulse of # of matched TOP slots (2D-TOP) > 3
A	17		pulse of # of matched KLM sectors (2D-KLM) = 1
A	18		pulse of # of matched KLM sectors (2D-KLM) > 1
A	19		pulse of # of matched KLM sectors (short-EKLM) = 1
A	20		pulse of # of matched KLM sectors (short-ELM) > 1
A	21		pulse of N_track = 1
A	22		pulse of N_track = 2
A	23		pulse of N_track = 3
A	24		pulse of N_track > 3
A	25		pulse of # of short track = 1
A	26		pulse of # of short track = 2
A	27		pulse of # of short track = 3
A	28		pulse of # of short track > 3
A	29	i2io	~~TSF1 b2b~~ TSF0,1,2 vs TSF0,1,2 open
A	30	typ	~~TSF2 b2b~~ pulse of NN single track
A	31		pulse of # of 3D z0 cut track = 1
B	0		pulse of # of 3D z0 cut track = 2
B	1		pulse of # of 3D z0 cut track = 3
B	2		pulse of # of 3D z0 cut track > 3
B	3		pulse of # of NN z0 cut track = 1
B	4		pulse of # of NN z0 cut track = 2
B	5		pulse of # of NN z0 cut track = 3
B	6		pulse of # of NN z0 cut track > 3
B	7		pulse of reduced N_track = 1
B	8		pulse of reduced N_track = 2
B	9		pulse of reduced N_track = 3
B	10		pulse of reduced N_track > 3
B	11	fwd_s	#forward short track>0
B	12	bwd_s	#backward short track >0
B	13	f2f30	open30, full-to-full
B	14	s2s30	open30, short-to-short
B	15		open30, short-to-full
B	16		TSF0,1,2 b2b
B	17	typ4	~~pulse of # of NN veto cut track = 1~~ pulse of NN single track p>0.4GeV
B	18	typ5	~~pulse of # of NN veto cut track = 2~~ pulse of NN single track p>0.5GeV
B	19	typ6	~~pulse of # of NN veto cut track = 3~~ pulse of NN single track p>0.6GeV
B	20		pulse of # of NN veto cut track > 3
B	21	ti	TSF0,1,2 coincidence
B	22	i2fo	TSF0,1,2 coincidence vs ft open90
B	23	secl	short-Endcap ECL matching
B	24	iecl_0	#TSF0.1.2-Endcap ECL matching>0
B	25	ecleklm	ECL-EKLM matching
B	26		st vs st b2b_1to5
B	27		st vs st open90
B	28		st vs ft b2b_1to5
B	29		st vs ft open90
B	30		total matched bhabha cluster in 3 regions, N = 1
B	31		total matched bhabha cluster in 3 regions, N > 1

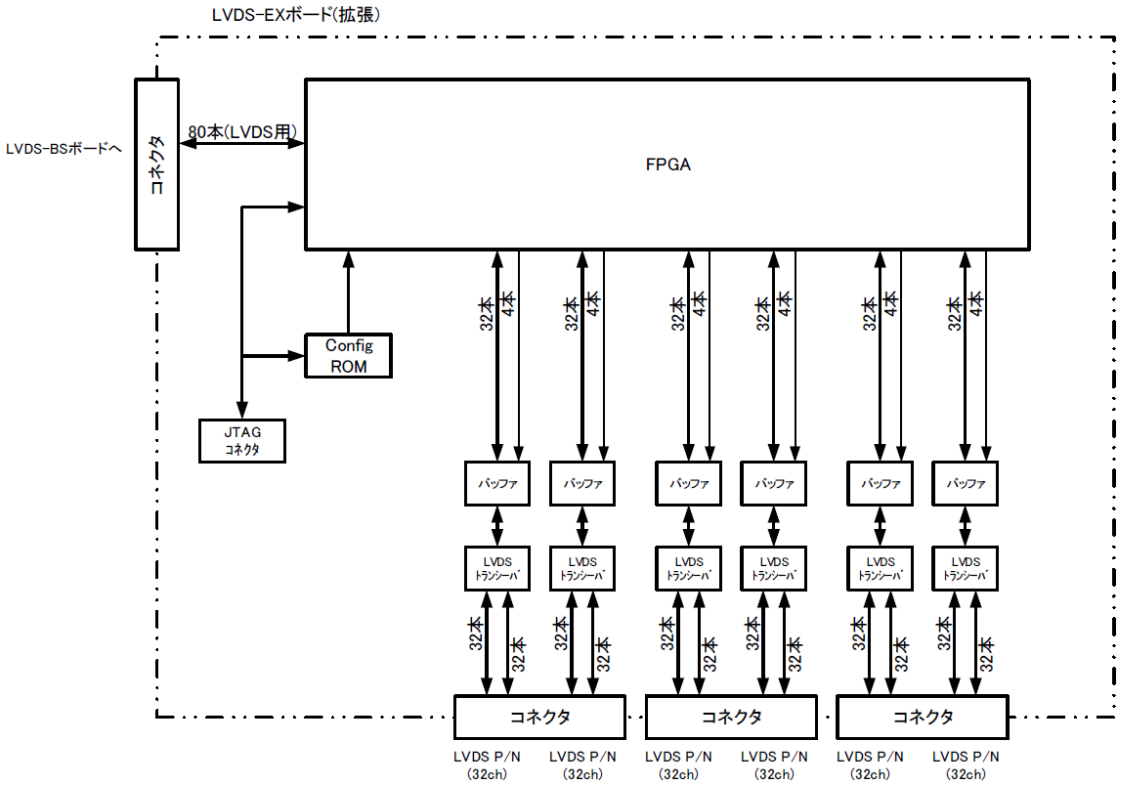
Transition to LVDS extended UT4

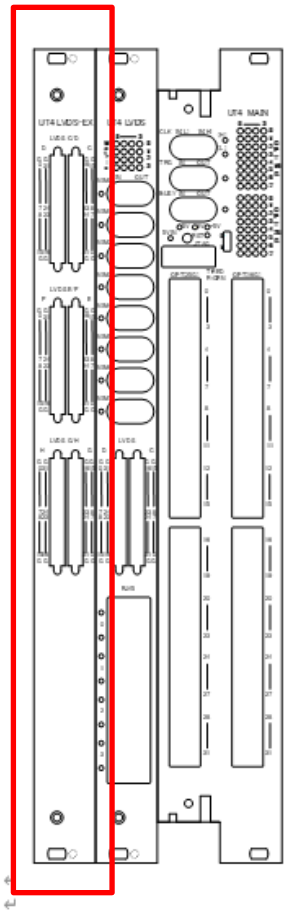
-LVDS extended UT4 will be produced at next year for GRL and GDL

-Additional 32x3 LVDS port with a new boards

-It is possible to keep and send more bits

-GRL and GDL will be updated with the LVDS extended UT4 during LS1 if time allows.





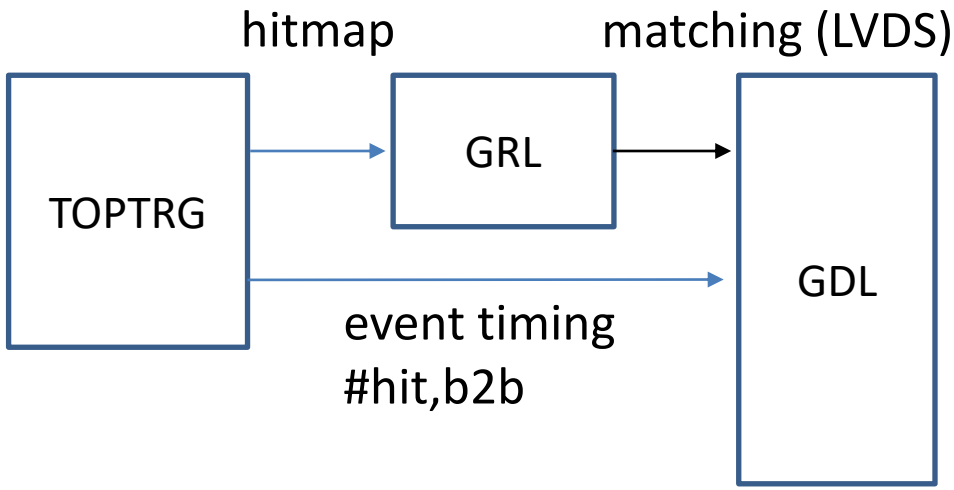
CDC-TOP matching

-TOPTRG and GRL FW will be modified for track matching

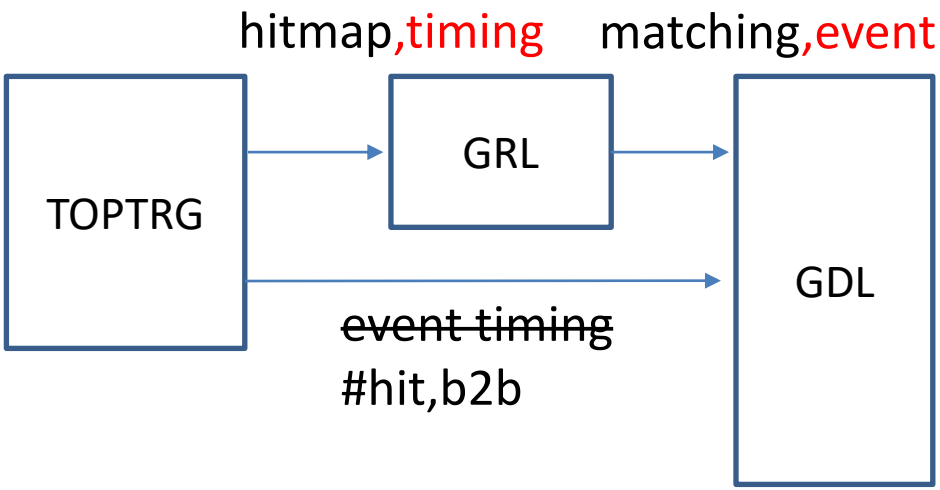
-matching itself has been done successfully on GRL since 2019, with ~90% efficiency with dimuon

-matching information will be newly used for timing decision

Present



New



TOPTRG->GRL data format

-Data format from Tianping, with 5Gbps on GTH0,1 (256bits/127MHz)

-I make a table in this time. Is this OK? More bits possible with 12Gbps.

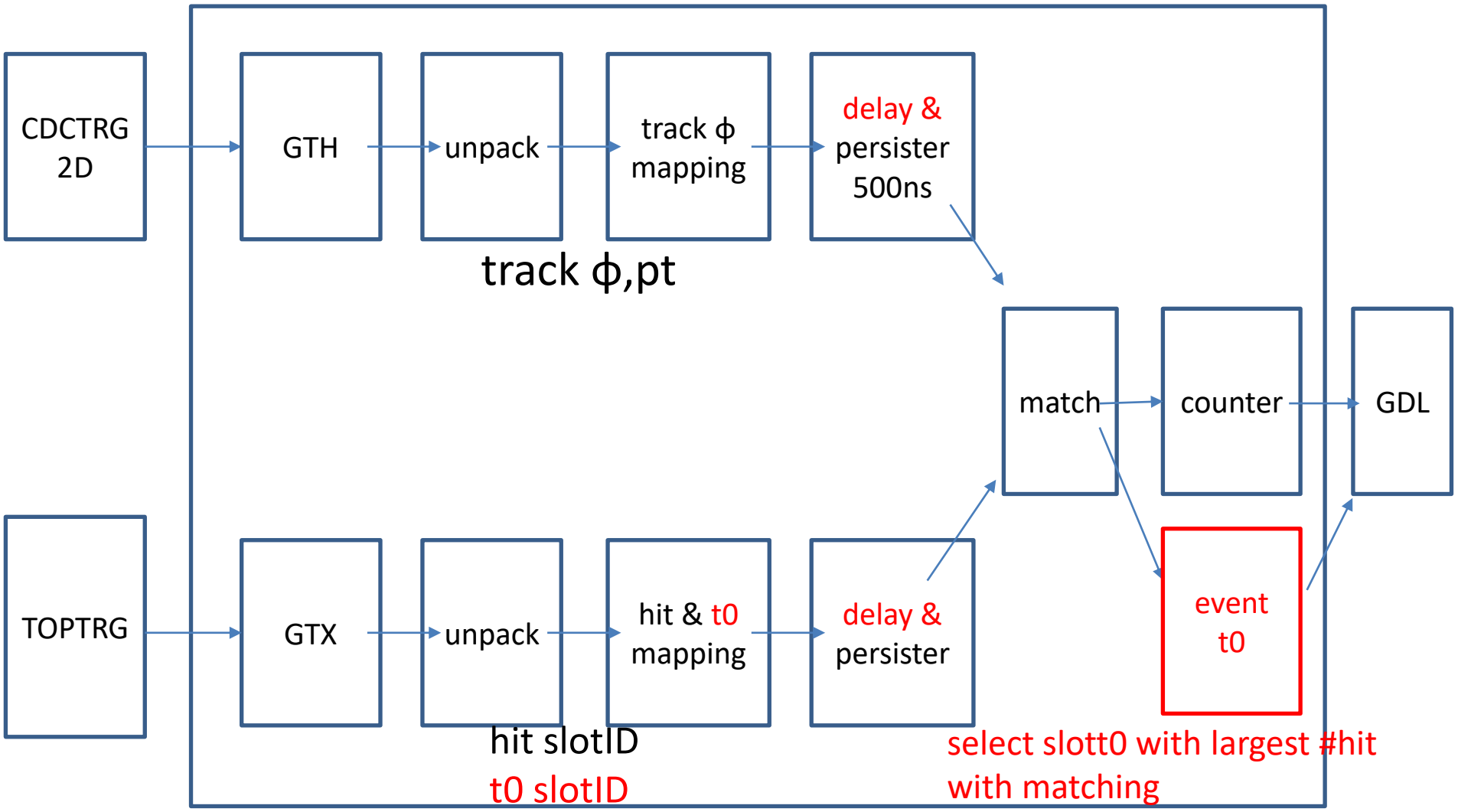
GTH0, slot0-7(same as GTH1, slot8-15)

bit	7	6	5	4	3	2	1	0
127-120	t0 activate flag (1bit × 8 slot=8bits, 127-120)							
119-112	#of hits (8bits × 8 slot=64bits, 119-56)							
111-104								
103-96								
95-88								
87-80								
79-72								
71-64								
63-56								
55-48	clock counter (10bits, 56-45)							
47-40			slot t0 (6bits × 8slot=48bits, 47-0)					
39-32								
31-24								
23-16								
15-8								
7-0								
+	send additional 10bits for validation with >5Gbps							

New CDC-TOP matching logic on GRL

-Modification (red) of logic on GRL from Koga

-Better to align the hit timing according to estimated t0 on TOPTRG, if latency allows

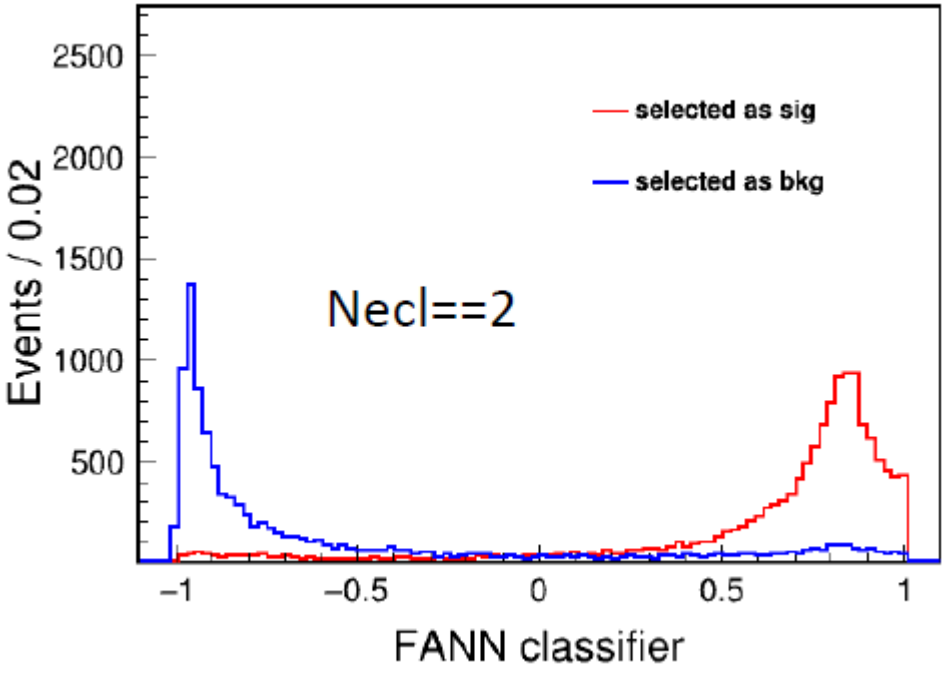


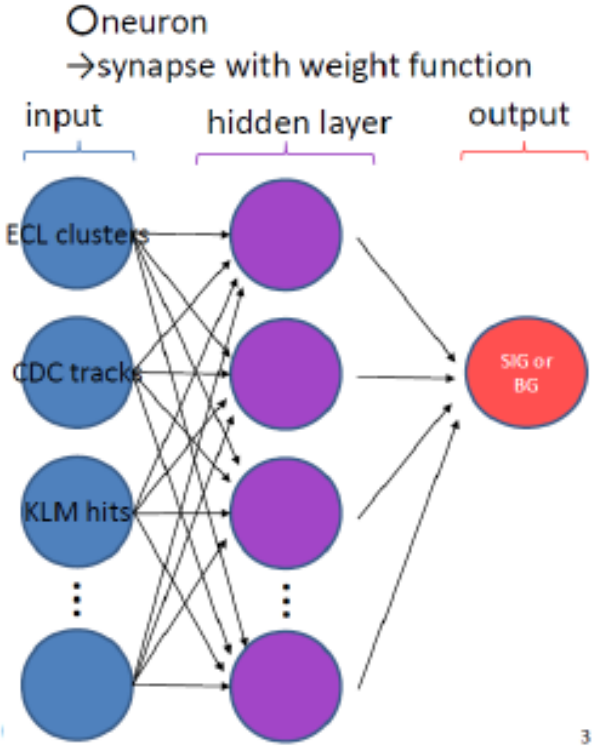
Neural network simulation

-Neural network on GRL to judge signal and BG with all subtrigger inputs

-Junhao is performing R&D with simulation

- -it looks good signal and BG identification for tau events
- -getting close to optimization



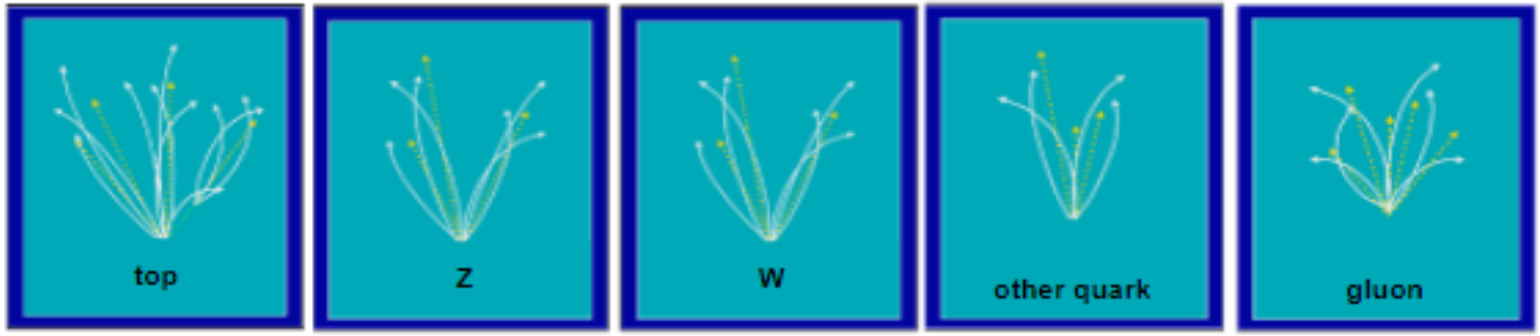


Neural network with vivado HLS

-Nomaru-san, a new student from Tokyo University, is recently playing to implement neural network on FPGA with Vivado HLS

-with help of Yu Nakazawa-san

-IP core will be generated by python automatically with [example code on git from ATLAS workshop](#) to identify jet pattern



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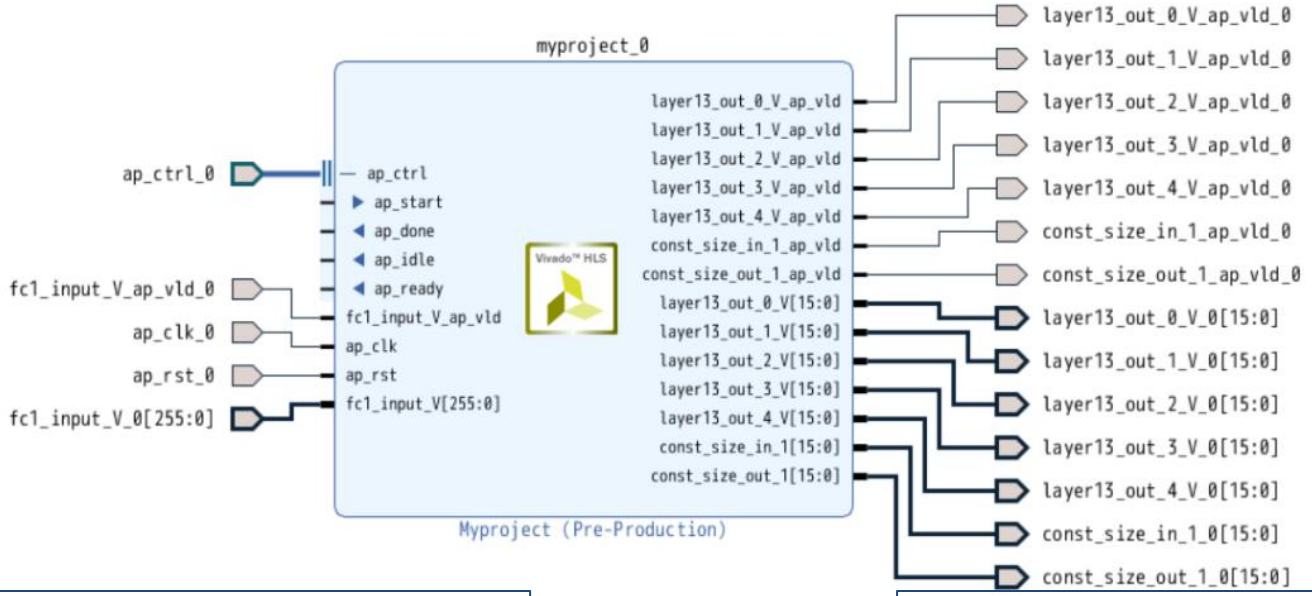
- -with help of Yu Nakazawa-san
- -IP core will be generated by python automatically with [example code on git from ATLAS workshop] to identify jet pattern

->plan to optimize ecltaub2b with machine learning, stay tuned

IP core made by Nomaru-san



Input of jet information

output of jet category

Summary of GRL status and plan in LS1

-Hardware transition of UT3→UT4, LVDS extended UT4

- ->check with ,KLM, TOP, UT4 GDL
- ->speed up optical transmission with ETM, GDL, TOP, CDC2D
- ->LVDS extended UT4

-CDC-TOP matching

- ->update data format and firmware

-Neural network implementation

- ->simulation study by Junhao
- ->Vivado HLS by Nomaru-san

Plan in LS2 and after

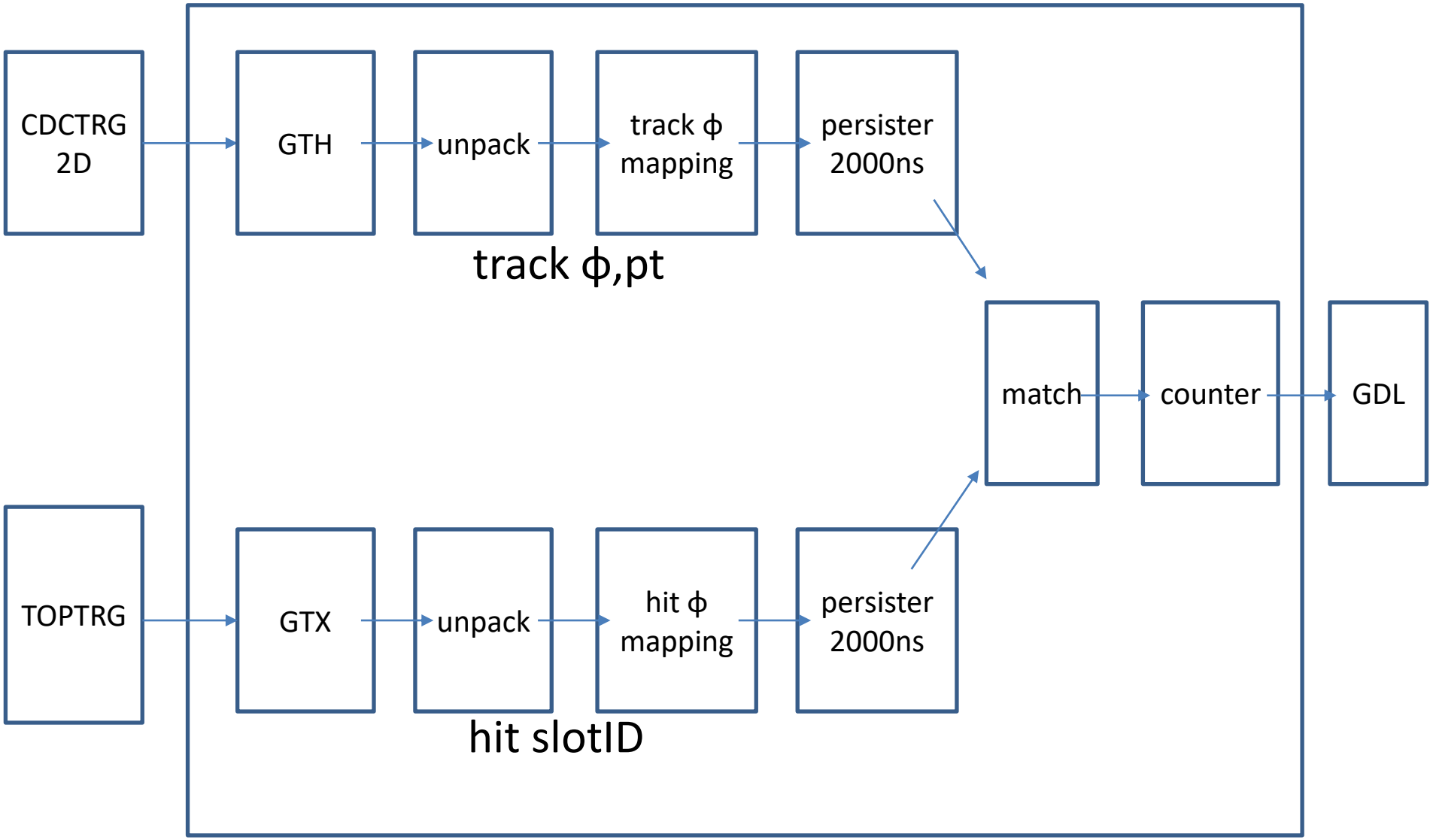
-There is no big plan of GRL upgrade in LS2 and after for now

-List of idea for brainstorming

- -Transition to UT5
  - -more resource and high speed link is possible
  - -neural net with vivado
  - -combine GRL and GDL on single FPGA
- -3D track matching of CDC-ECL,TOP,KLM
  - -BG reduction performance should be improved
  - -for now, it is impossible due to latency of 3D tracks from NN and 3D
- -Short tracking with full wires with ADC and TDC
  - -with new CDCFE (even with present CDCFE??)
  - -all wires inside TSF, or “TSF less” tracking
  - -we can measure |z| position to improve BG rejection

backup

Present CDC-TOP matching logic on GRL

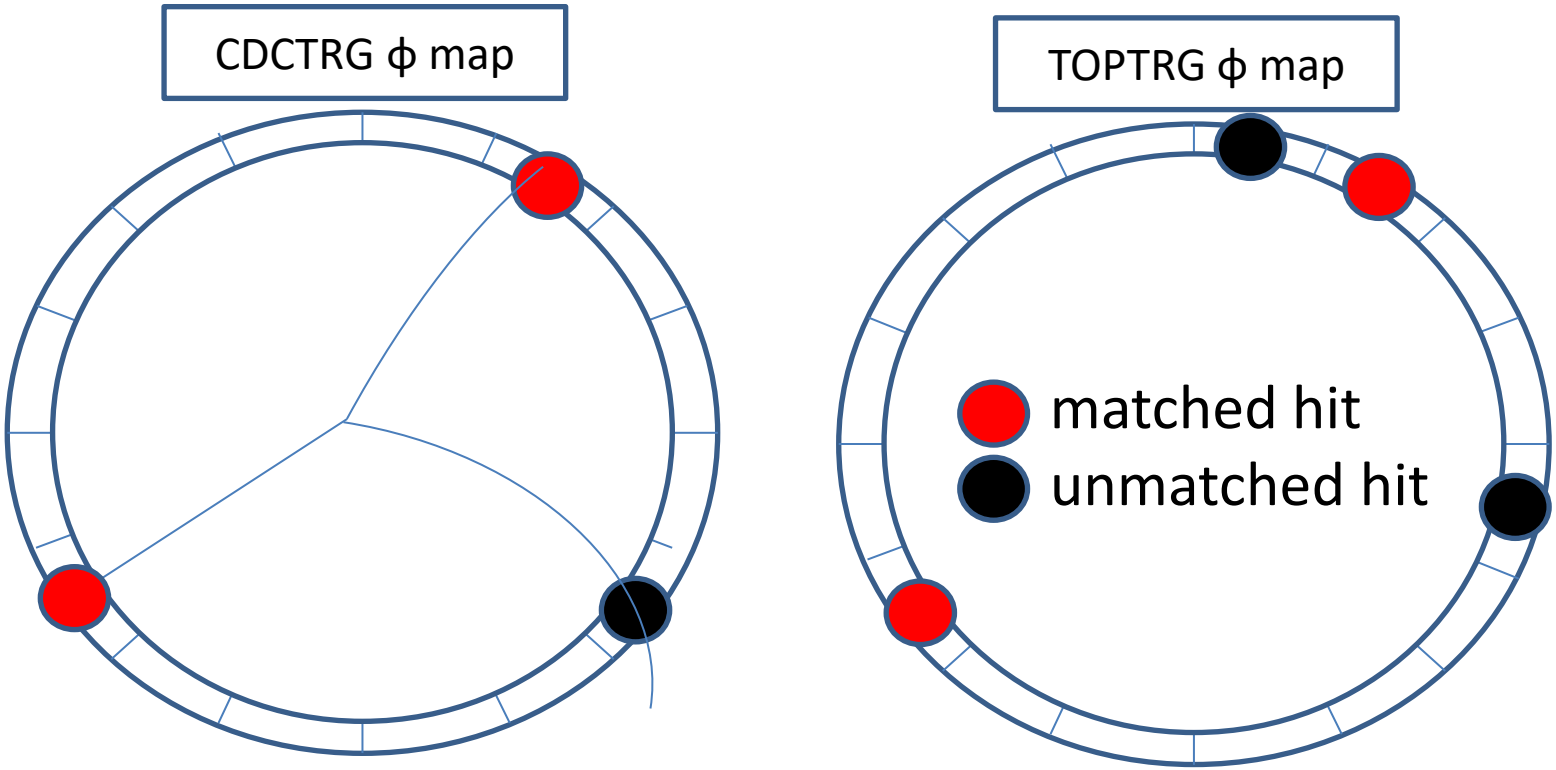


Present CDC-TOP matching logic on GRL

-Make ϕ map of CDC 2D track and TOP hit
  -ϕ is divided in 16 slots
  -CDC ϕ is extrapolated to TOP with pt curve

-If ϕ map of CDC and TOP have hits in the same slot, judged as matched

-Count the number of matched CDC-TOP tracks and send it to GDL
  -input bit name: cdctop_0-3



Present TOPTRG->GRL data format

-Present bit map with 128bits/127MHz (5Gbps × 4lane)
-totally 78 spare bits

bit	7	6	5	4	3	2	1	0
127-120	clock counter							
119-112				hit flag	slot hit map			
111-104								
103-96					b2b	spare		
95-88								
87-80							combined t0	
79-72								
71-64								

Present TOPTRG->GRL data format

-Present bit map with 128bits/127MHz (5Gbps × 4lane)
-totally 78 spare bits

bit	7	6	5	4	3	2	1	0
63-56	spare(segment number, not used anymore)							
55-48								
47-40								
39-32								
31-24								
23-16								
15-8								
7-0								

GRL UT4 commissioning

-Report at last B2GM

-GRL is updated with UT4 VU080
- -UT4 installed to vmetrg18.
  reconnect optical cables from UT3 GRL.
- -named “grl2” on btrgsrv0 temporary
- -UT3 GRL is still kept in Ehut.

-Commissioning is done with cosmic
- -Trigger rate is consistent with UT3
- -DQM is consistent with UT3
- ->Need to check more bits with KLM and TOP before next physics run

UT4 GRL logic change

-No core logic is changed

-To avoid compile error, one of short track source code is modified

-trigger rate counter is added on VME to monitor all output bit rate

-TOP module and interface modules of VME, OPT, B2L are modified with library

-The latest code is on svn:
UT4/FPGA/GRL/GRL_v1.0

-TOPTRG interface will be modified after UT4 toptrg be ready.

UT4 GRL: channel configuration and transceiver speed

-All cables were replaced from UT3 GRL to UT4 GRL
  -LEMO, RJ45, OPT, Jtag, LVDS (A and B only)
  -no change of optical speed for now (can be speed up)
  -GTY: 127MHz, GTH: 254MHz reference clock

GTY	GTH	speed	GTH		speed
GTY0	2D		GTH0	TOP1	
GTY1	3D		GTH1	TOP2	
GTY2	NN		GTH2	TSF0	
GTY3	ETM		GTH3	TSF2	
GTY4	KLM		GTH4	TSF4	
GTY5	GDL		GTH5	TSF1	
GTY6	--		GTH6	TSF3	
GTY7	--		GTH7	B2L	

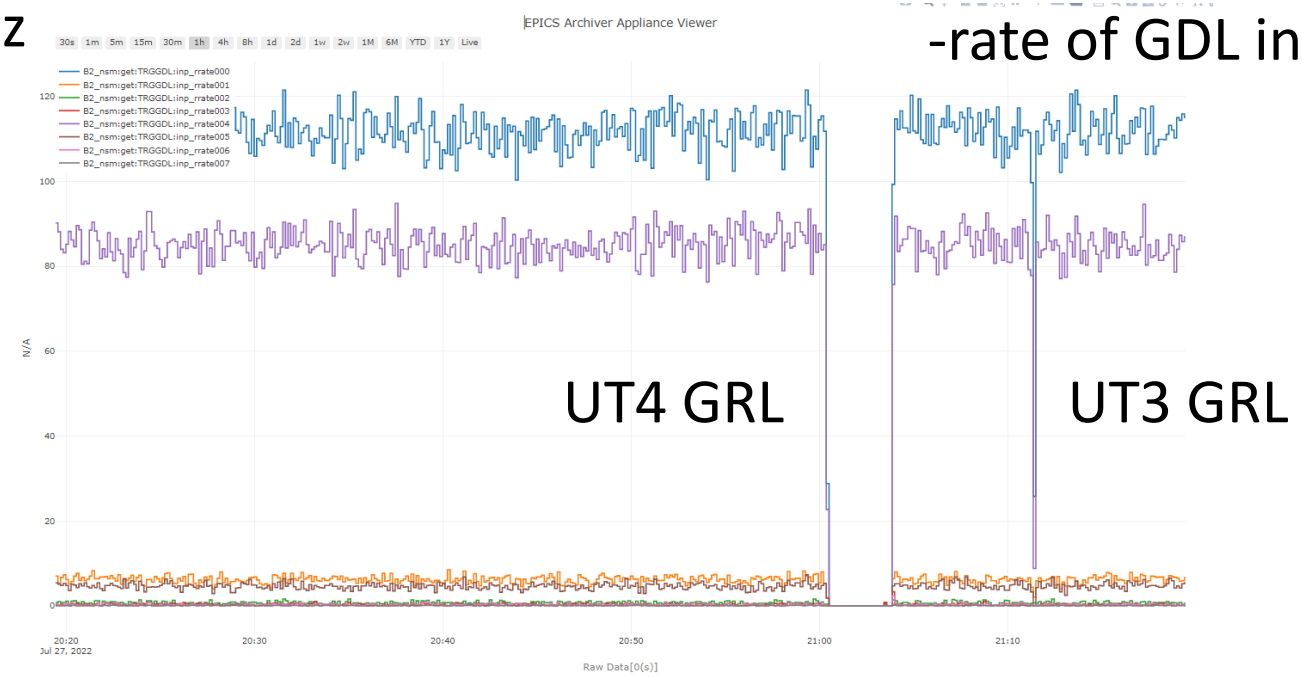
Output rate check

-All input bit rates from GRL are checked on GDL between UT3 GRL and UT4 GRL with cosmic, except for

- -bits on LVDS_C
- -TOP and KLM related bits (HV OFF)
- -low rate bits with cosmic

-Rates are consistent between UT3 and UT4.

Hz



-rate of GDL input bits

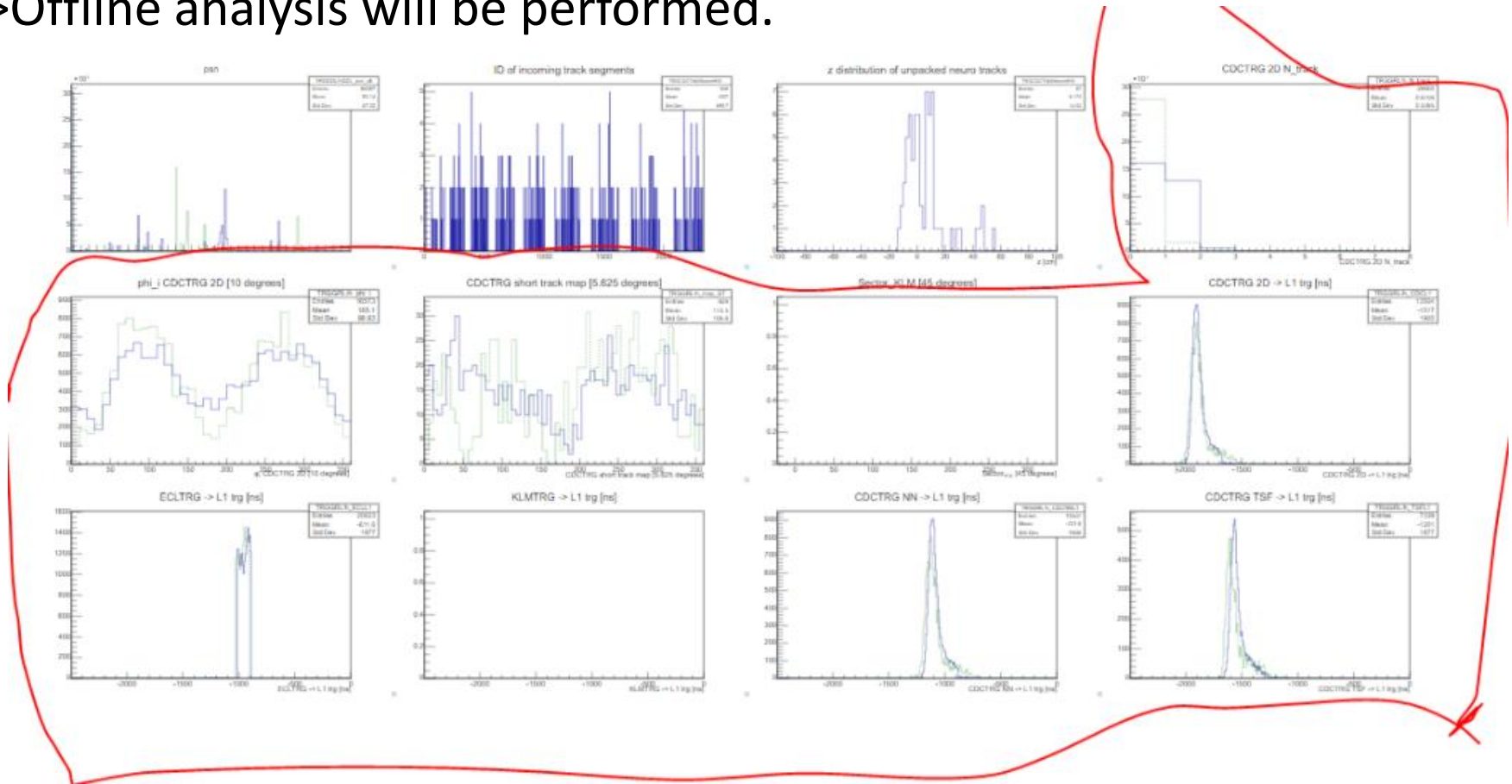
UT4 GRL

UT3 GRL

DQM

-After a few bug fixes, B2L works with UT4 GRL
  -GTH, 254MHz reference clock

-Plots on DQM are consistent with UT3 GRL.
 ->Latency will be checked more carefully.
 ->Offline analysis will be performed.



new bit map GRL->GDL with LVDS

-Because the number of LVDS port is 2(4) with UT4(UT3), need to reduce the number of bits. Now keep old bitmap without LVDS_C.

-New bit map: https://confluence.desy.de/pages/viewpage.action?pageId=75106458

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A	1		cluster_b2b_1to5
A	2		trkcluster_b2b_1to5
A	3		samehem
A	4		opphem
A	5		pulse of # of matched clusters (2D-ECL) = 1
A	6		pulse of # of matched clusters (2D-ECL) = 2
A	7		pulse of # of matched clusters (2D-ECL) = 3
A	8		pulse of # of matched clusters (2D-ECL) > 3
A	9		pulse of # of matched 2GeV clusters (2D-ECL) = 1
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A	11		b2b_1to7: Opening angle of 2 tracks from 140 to 180
A	12		cdc_open90
A	13		pulse of # of matched TOP slots (2D-TOP) = 1
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A	31		pulse of # of 3D z0 cut track = 1
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B	4		pulse of # of NN z0 cut track = 2
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B	13	f2f30	open30, full-to-full
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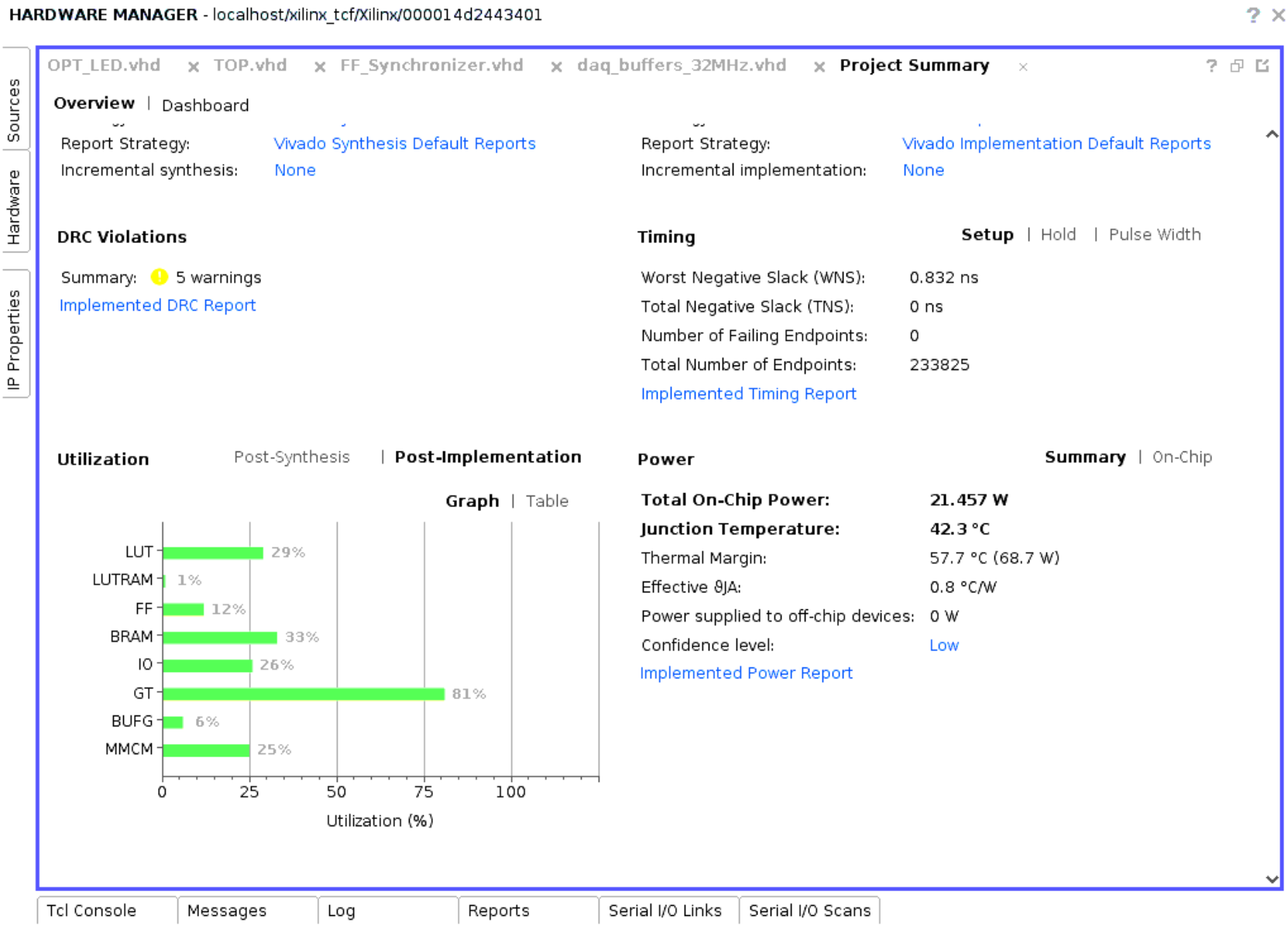
resource usage

-with B2L



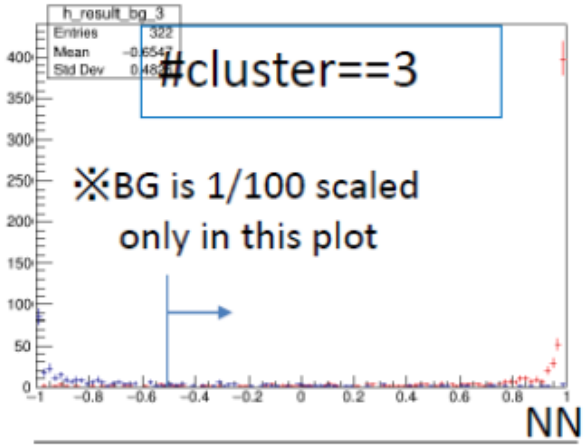
GRL UT4: plan in LS1

-Remained commissioning items of UT4 GRL

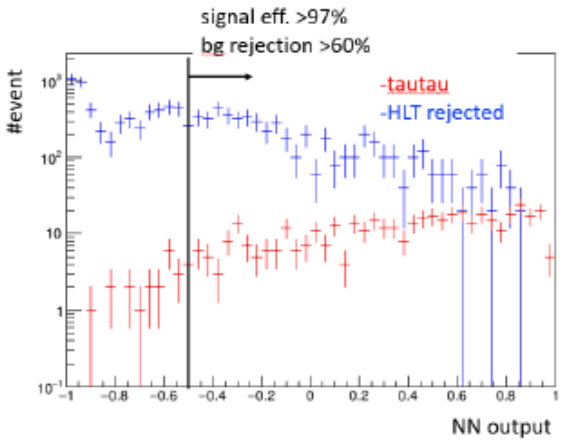
- -KLMTRG
- -TOPTRG
- -GRL->UT4GDL with new bit map
- -low rate bits with cosmic

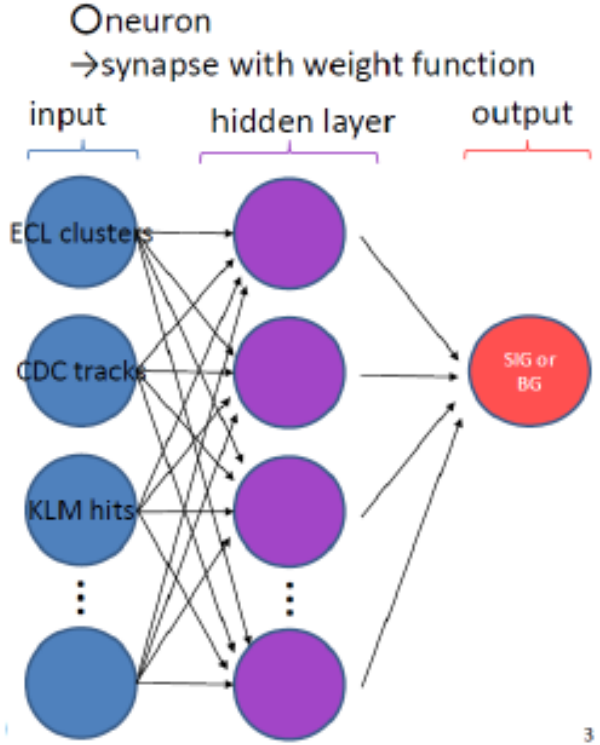
-design, implementation, comissioning of NN logic on GRL

hadronb2 skim case



tautau skim case





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A	2		cluster_b2b_1to5
~~A~~	~~3~~		~~cluster_b2b_1to3~~
~~A~~	~~4~~		~~trkcluster_b2b_1to9~~
~~A~~	~~5~~		~~trkcluster_b2b_1to7~~
A	6		trkcluster_b2b_1to5
~~A~~	~~7~~		~~trkcluster_b2b_1to3~~
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A	12		pulse of # of matched clusters (2D-ECL) = 3
A	13		pulse of # of matched clusters (2D-ECL) > 3
A	14		pulse of # of matched 2GeV clusters (2D-ECL) = 1
A	15		pulse of # of matched 2GeV clusters (2D-ECL) = 2
~~A~~	~~16~~		~~pulse of # of matched~~ 2GeV clusters (2D-ECL) = 3
~~A~~	~~17~~		~~pulse of # of matched~~ 2GeV clusters (2D-ECL) > 3

A	20 → 18		pulse of # of unmatched 1 GeV clusters (2D-ECL) = 1
A	21 → 19		pulse of # of unmatched 1 GeV clusters (2D-ECL) = 2
A	22 → 20		pulse of # of unmatched 1 GeV clusters (2D-ECL) = 3
A	23 → 21		pulse of # of unmatched 1 GeV clusters (2D-ECL) > 3
A	24 → 22		pulse of # of unmatched 2 GeV clusters (2D-ECL) = 1
A	25 → 23		pulse of # of unmatched 2 GeV clusters (2D-ECL) = 2
A	26 → 24		pulse of # of unmatched 2 GeV clusters (2D-ECL) = 3
A	27 → 25		pulse of # of unmatched 2 GeV clusters (2D-ECL) > 3
A	26		b2b_1to9: Opening angle of 2 tracks from 130 to 180
A	27		b2b_1to7: Opening angle of 2 tracks from 140 to 180
A	28		b2b_1to5: Opening angle of 2 tracks from 150 to 180
A	29		b2b_1to3: Opening angle of 2 tracks from 160 to 180
A	30		cdc_open90
A	31		TSF0 b2b

B	0		pulse of # of matched TOP slots (2D-TOP) = 1
B	1		pulse of # of matched TOP slots (2D-TOP) = 2
B	2		pulse of # of matched TOP slots (2D-TOP) = 3
B	3		pulse of # of matched TOP slots (2D-TOP) > 3
B	4		pulse of # of matched KLM sectors (2D-KLM) = 1
B	5		pulse of # of matched KLM sectors (2D-KLM) > 1
B	6		pulse of # of matched KLM sectors (short-EKLM) = 1
B	7		pulse of # of matched KLM sectors (short-ELM) > 1
B	8		pulse of N_track = 1
B	9		pulse of N_track = 2
B	10		pulse of N_track = 3
B	11		pulse of N_track > 3
B	12		pulse of # of short track = 1
B	13		pulse of # of short track = 2
B	14		pulse of # of short track = 3
B	15		pulse of # of short track > 3
B	16	i2io	~~TSF1 b2b~~ TSF0,1,2 vs TSF0,1,2 open
B	17	tyo	~~TSF2 b2b~~ pulse of NN single track

new bit map GRL->GDL with LVDS

-Because the number of LVDS port is 2(4) with UT4(UT3), need to reduce the number of bits

-Original bit map: https://confluence.desy.de/pages/viewpage.action?pageId=75106458

B	18		pulse of # of 3D z0 cut track = 1
B	19		pulse of # of 3D z0 cut track = 2
B	20		pulse of # of 3D z0 cut track = 3
B	21		pulse of # of 3D z0 cut track > 3
B	22		pulse of # of NN z0 cut track = 1
B	23		pulse of # of NN z0 cut track = 2
B	24		pulse of # of NN z0 cut track = 3
B	25		pulse of # of NN z0 cut track > 3
B	26		pulse of reduced N_track = 1
B	27		pulse of reduced N_track = 2
B	28		pulse of reduced N_track = 3
B	29		pulse of reduced N_track > 3
B	30	fwd_s	#forward short track>0
B	31	bwd_s	#backward short track >0

C	0	f2f30	open30, full-to-full
C	1	s2s30	open30, short-to-short
C	2		open30, short-to-full
C	3		TSF0,1,2 b2b
C	4	typ4	~~pulse of # of NN veto cut track = 1~~ pulse of NN single track p>0.4GeV
C	5	typ5	~~pulse of # of NN veto cut track = 2~~ pulse of NN single track p>0.5GeV
C	6	typ6	~~pulse of # of NN veto cut track = 3~~ pulse of NN single track p>0.6GeV
C	7		pulse of # of NN veto cut track > 3
C	8	zi	TSF0,1,2 coincidence
C	9	i2fo	TSF0,1,2 coincidence vs ft open90
C	10	secl	short-Endcap ECL matching
C	11	iecl_0	#TSF0,1,2-Endcap ECL matching>0
C	12	eclekIm	ECL-EKLM matching
C	13	iekIm	TSF0,1,2-EKLM matching
C	14		matched, 2D (full) vs bhabha cluster, N = 1
C	15		matched, 2D (full) vs bhabha cluster, N > 1
C	16		non-matched, 2D (full) vs bhabha cluster, N = 1
C	17		non-matched, 2D (full) vs bhabha cluster, N > 1

C	18		st vs st b2b_1to3
C	19		st vs st b2b_1to5
C	20		st vs st open90
C	21		st vs ft b2b_1to3
C	22		st vs ft b2b_1to5
C	23		st vs ft open90
C	24		forward endcap, non-matched bhabha cluster
C	25		backward endcap, non-matched bhabha cluster
C	26		forward endcap, matched st vs bhabha cluster
C	27		backward endcap, matched st vs bhabha cluster
C	28		total matched bhabha cluster in 3 regions, N = 1
C	29		total matched bhabha cluster in 3 regions, N > 1
C	30		No cluster matched in 3 regions
C	31		No cluster matched in 3 regions && No TSF(0,1,2) b2b

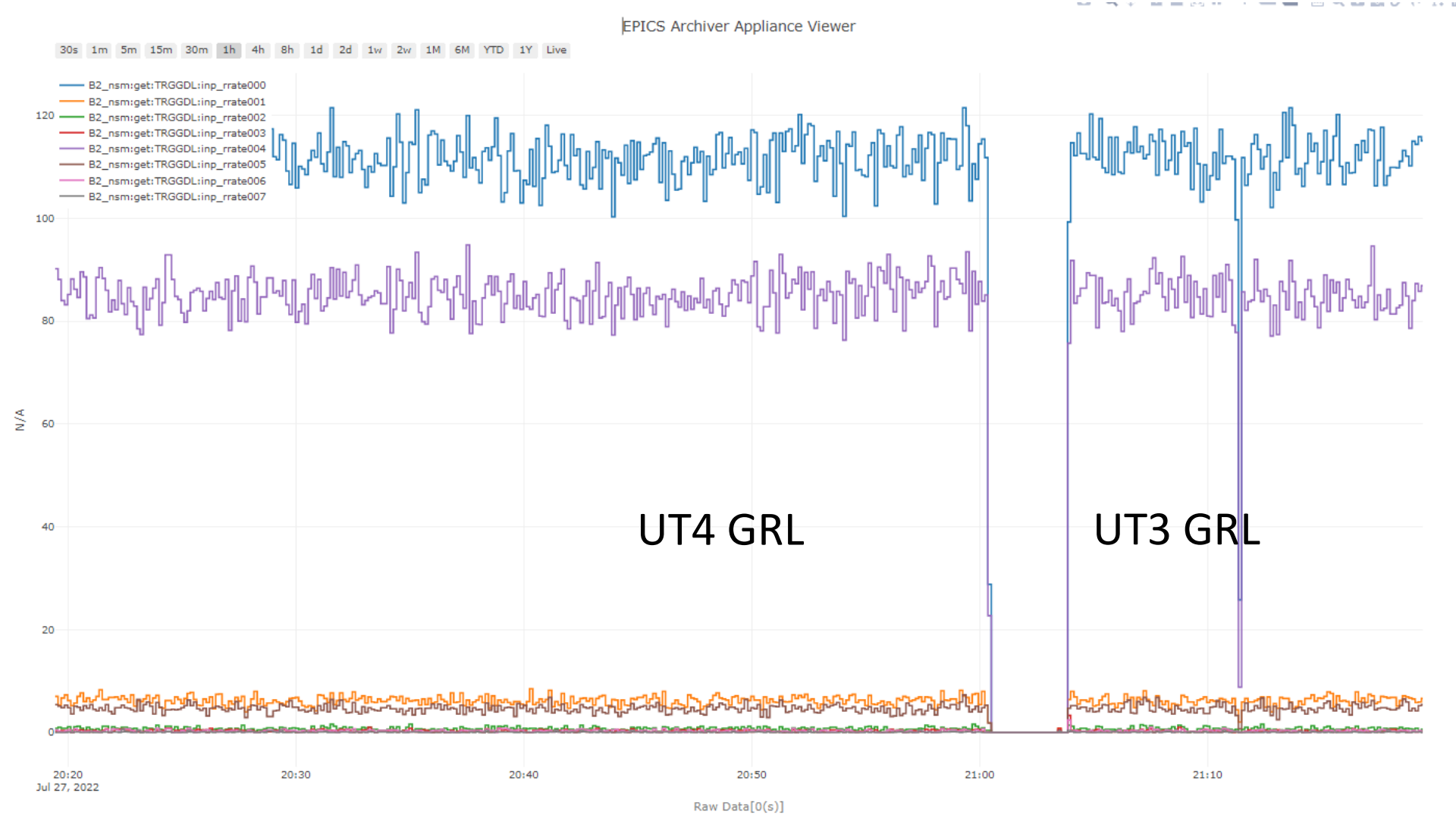
new bit map GRL->GDL with LVDS

-Because the number of LVDS port is 2(4) with UT4(UT3), need to reduce the number of bits

-New bit map: https://confluence.desy.de/pages/viewpage.action?pageId=75106458

LVDS	bit position		content
A	0	iecl_1	#TSF0.1.2-Endcap ECL matching>1
A	1		cluster_b2b_1to5
A	2		trkcluster_b2b_1to5
A	3		samehem
A	4		opphem
A	5		pulse of # of matched clusters (2D-ECL) = 1
A	6		pulse of # of matched clusters (2D-ECL) = 2
A	7		pulse of # of matched clusters (2D-ECL) = 3
A	8		pulse of # of matched clusters (2D-ECL) > 3
A	9		pulse of # of matched 2GeV clusters (2D-ECL) = 1
A	10		pulse of # of matched 2GeV clusters (2D-ECL) = 2
A	11		b2b_1to7: Opening angle of 2 tracks from 140 to 180
A	12		cdc_open90
A	13		pulse of # of matched TOP slots (2D-TOP) = 1
A	14		pulse of # of matched TOP slots (2D-TOP) = 2
A	15		pulse of # of matched TOP slots (2D-TOP) = 3
A	16		pulse of # of matched TOP slots (2D-TOP) > 3
A	17		pulse of # of matched KLM sectors (2D-KLM) = 1
A	18		pulse of # of matched KLM sectors (2D-KLM) > 1
A	19		pulse of # of matched KLM sectors (short-EKLM) = 1
A	20		pulse of # of matched KLM sectors (short-ELM) > 1
A	21		pulse of N_track = 1
A	22		pulse of N_track = 2
A	23		pulse of N_track = 3
A	24		pulse of N_track > 3
A	25		pulse of # of short track = 1
A	26		pulse of # of short track = 2
A	27		pulse of # of short track = 3
A	28		pulse of # of short track > 3
A	29	i2io	~~TSF1 b2b~~ TSF0,1,2 vs TSF0,1,2 open
A	30	typ	~~TSF2 b2b~~ pulse of NN single track
A	31		pulse of # of 3D z0 cut track = 1
B	0		pulse of # of 3D z0 cut track = 2
B	1		pulse of # of 3D z0 cut track = 3
B	2		pulse of # of 3D z0 cut track > 3
B	3		pulse of # of NN z0 cut track = 1
B	4		pulse of # of NN z0 cut track = 2
B	5		pulse of # of NN z0 cut track = 3
B	6		pulse of # of NN z0 cut track > 3
B	7		pulse of reduced N_track = 1
B	8		pulse of reduced N_track = 2
B	9		pulse of reduced N_track = 3
B	10		pulse of reduced N_track > 3
B	11	fwd_s	#forward short track>0
B	12	bwd_s	#backward short track >0
B	13	f2f30	open30, full-to-full
B	14	s2s30	open30, short-to-short
B	15		open30, short-to-full
B	16		TSF0,1,2 b2b
B	17	typ4	~~pulse of # of NN veto cut track = 1~~ pulse of NN single track p>0.4GeV
B	18	typ5	~~pulse of # of NN veto cut track = 2~~ pulse of NN single track p>0.5GeV
B	19	typ6	~~pulse of # of NN veto cut track = 3~~ pulse of NN single track p>0.6GeV
B	20		pulse of # of NN veto cut track > 3
B	21	ti	TSF0,1,2 coincidence
B	22	i2fo	TSF0,1,2 coincidence vs ft open90
B	23	secl	short-Endcap ECL matching
B	24	iecl_0	#TSF0.1.2-Endcap ECL matching>0
B	25	ecleklm	ECL-EKLM matching
B	26		st vs st b2b_1to5
B	27		st vs st open90
B	28		st vs ft b2b_1to5
B	29		st vs ft open90
B	30		total matched bhabha cluster in 3 regions, N = 1
B	31		total matched bhabha cluster in 3 regions, N > 1

Rate check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B2_nsm:get:TRGGDL:inp_rrate001
B2_nsm:get:TRGGDL:inp_rrate002
B2_nsm:get:TRGGDL:inp_rrate003
B2_nsm:get:TRGGDL:inp_rrate004
B2_nsm:get:TRGGDL:inp_rrate005
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B2_nsm:get:TRGGDL:inp_rrate007
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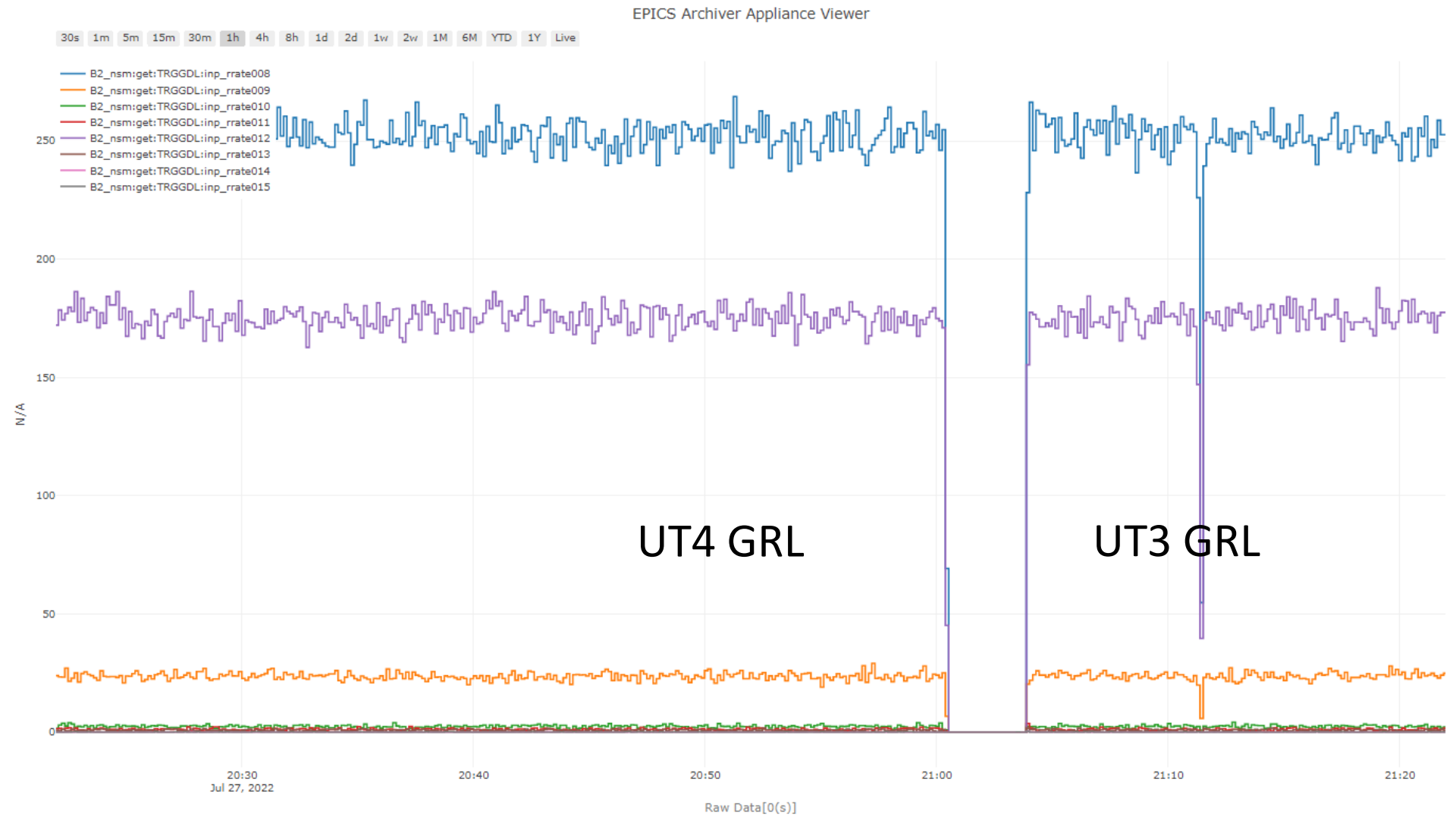
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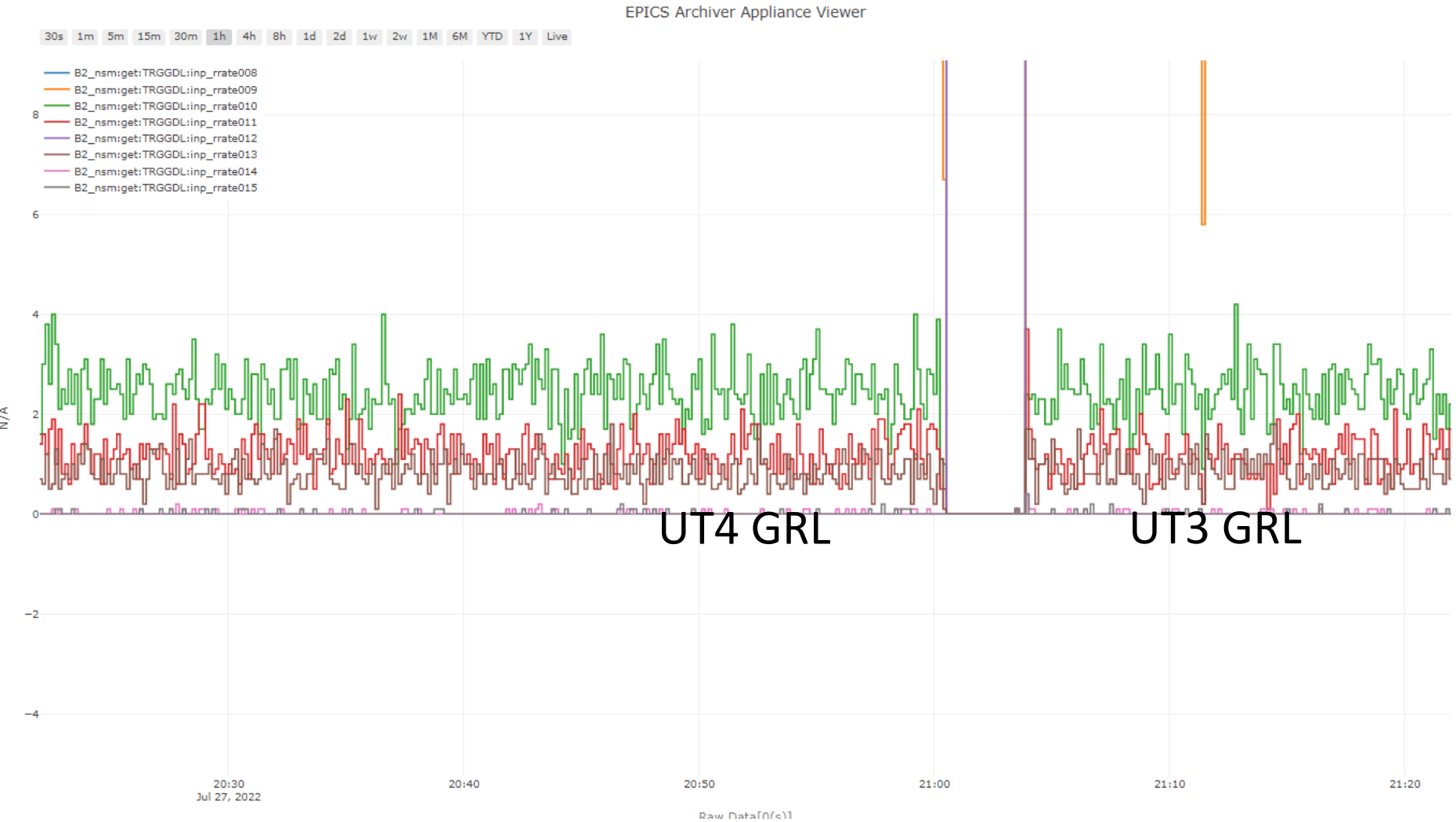
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UT3 GRL

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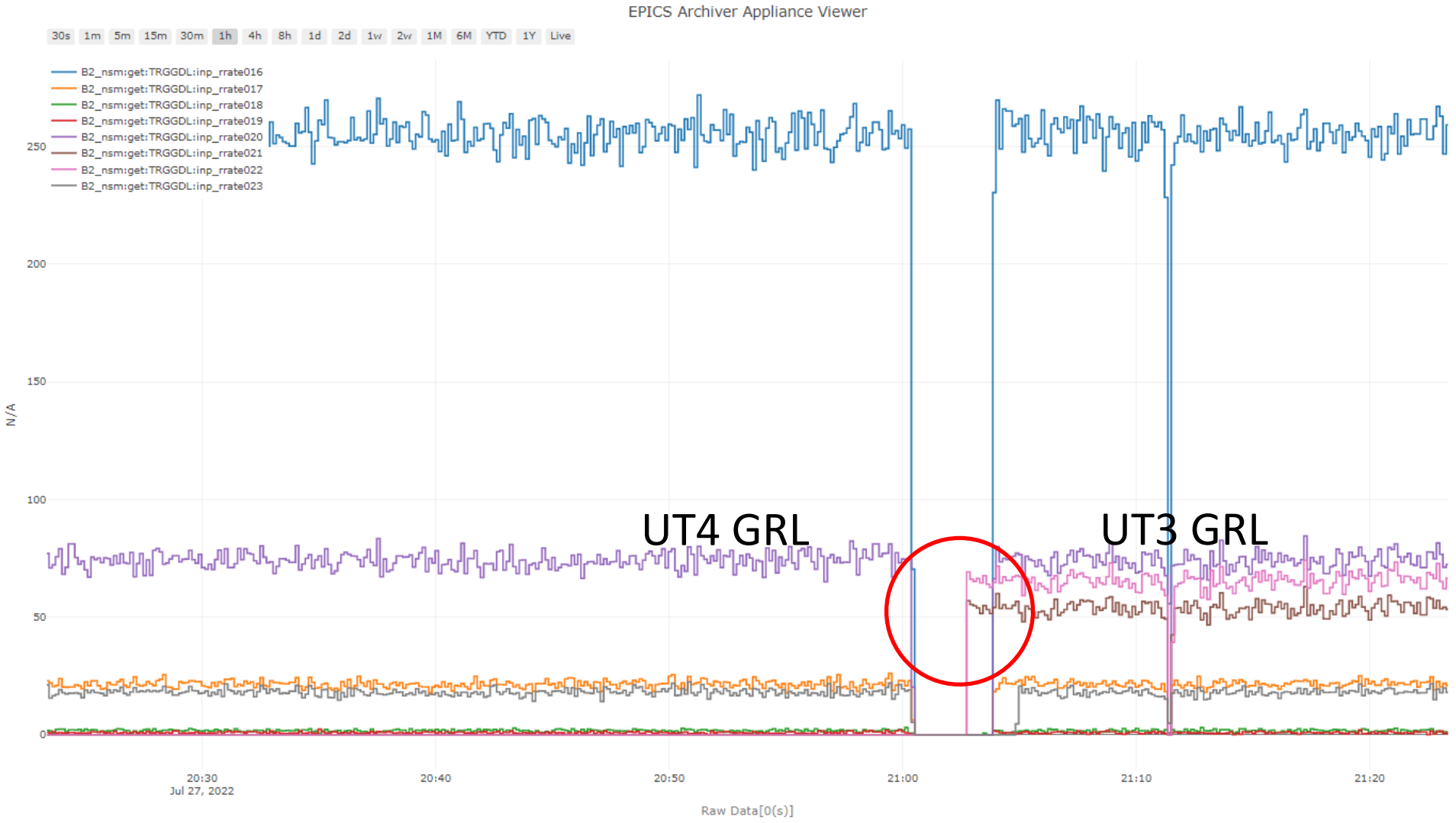
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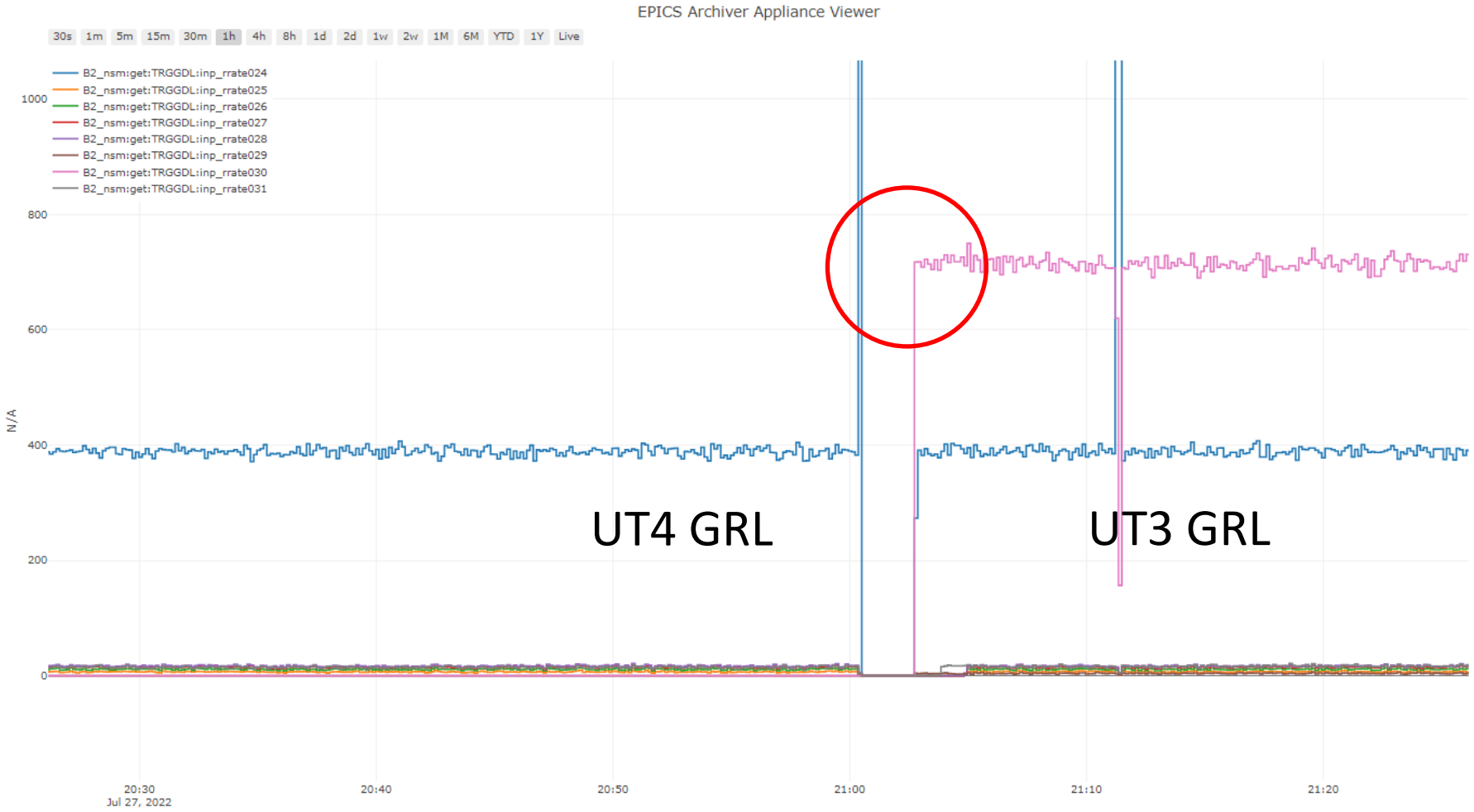
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B2_nsm:get:TRGGDL:inp_rrate030
B2_nsm:get:TRGGDL:inp_rrate031
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600
400
200
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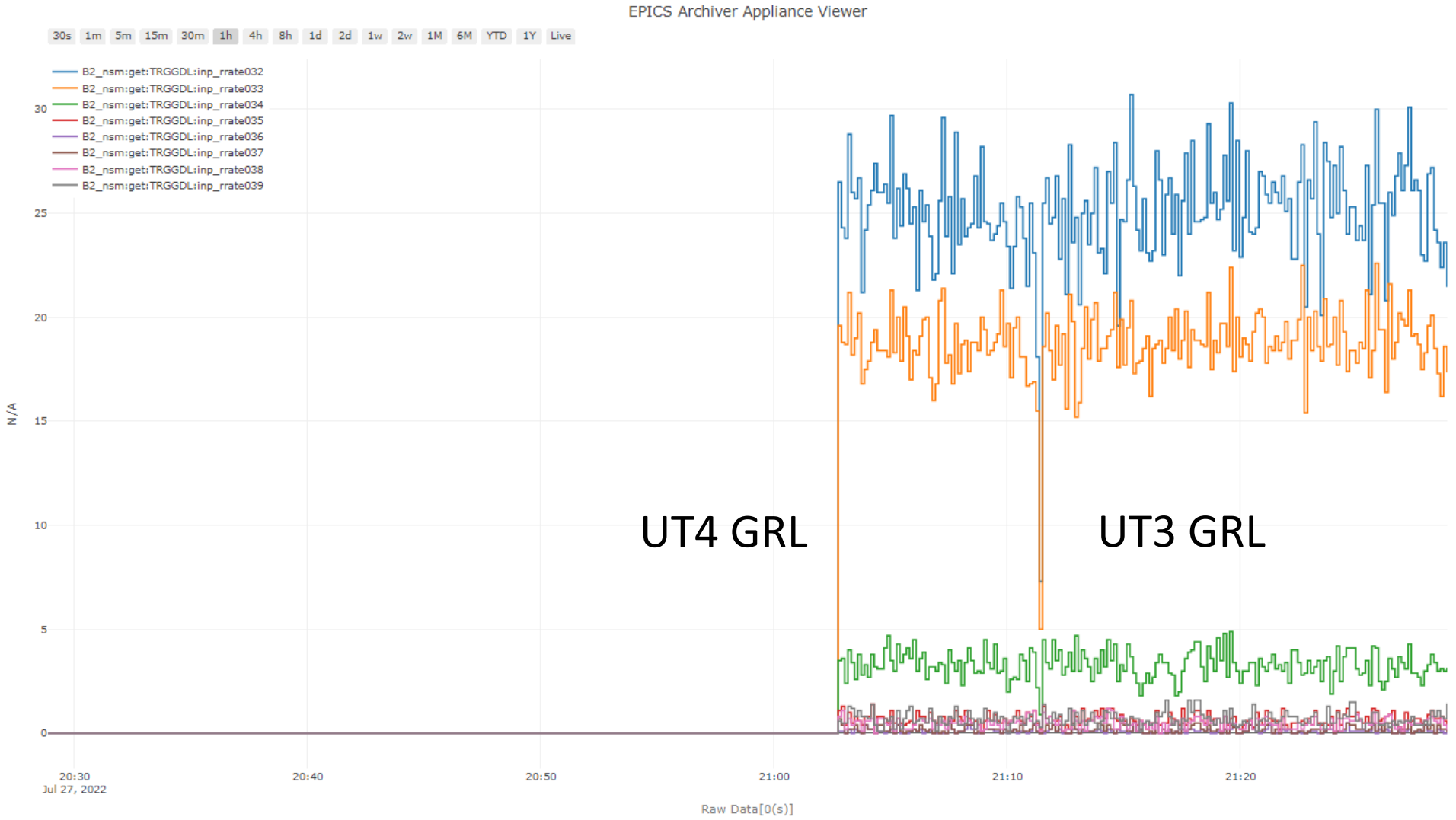
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B2_nsm:get:TRGGDL:inp_rrate038
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10
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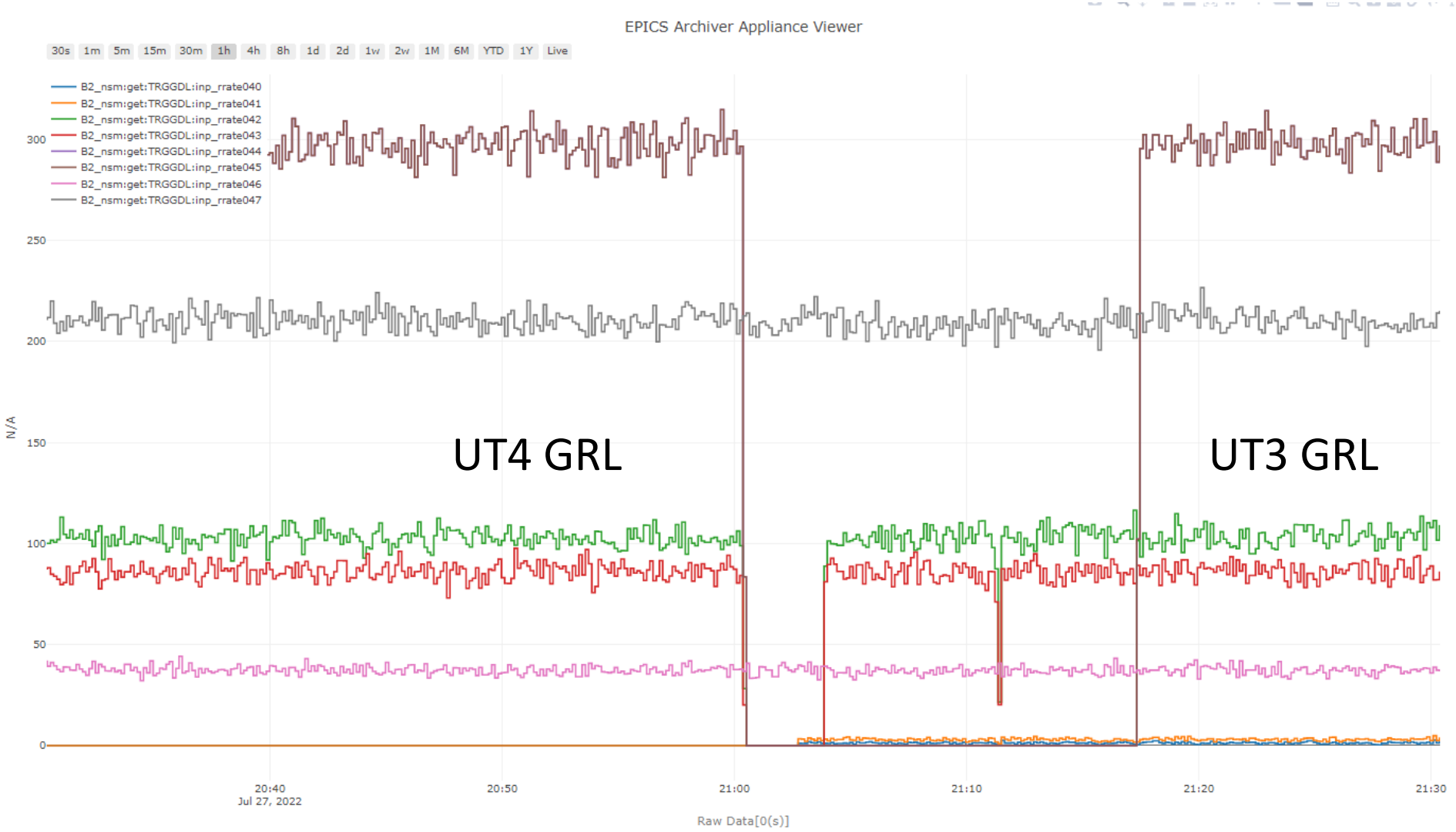
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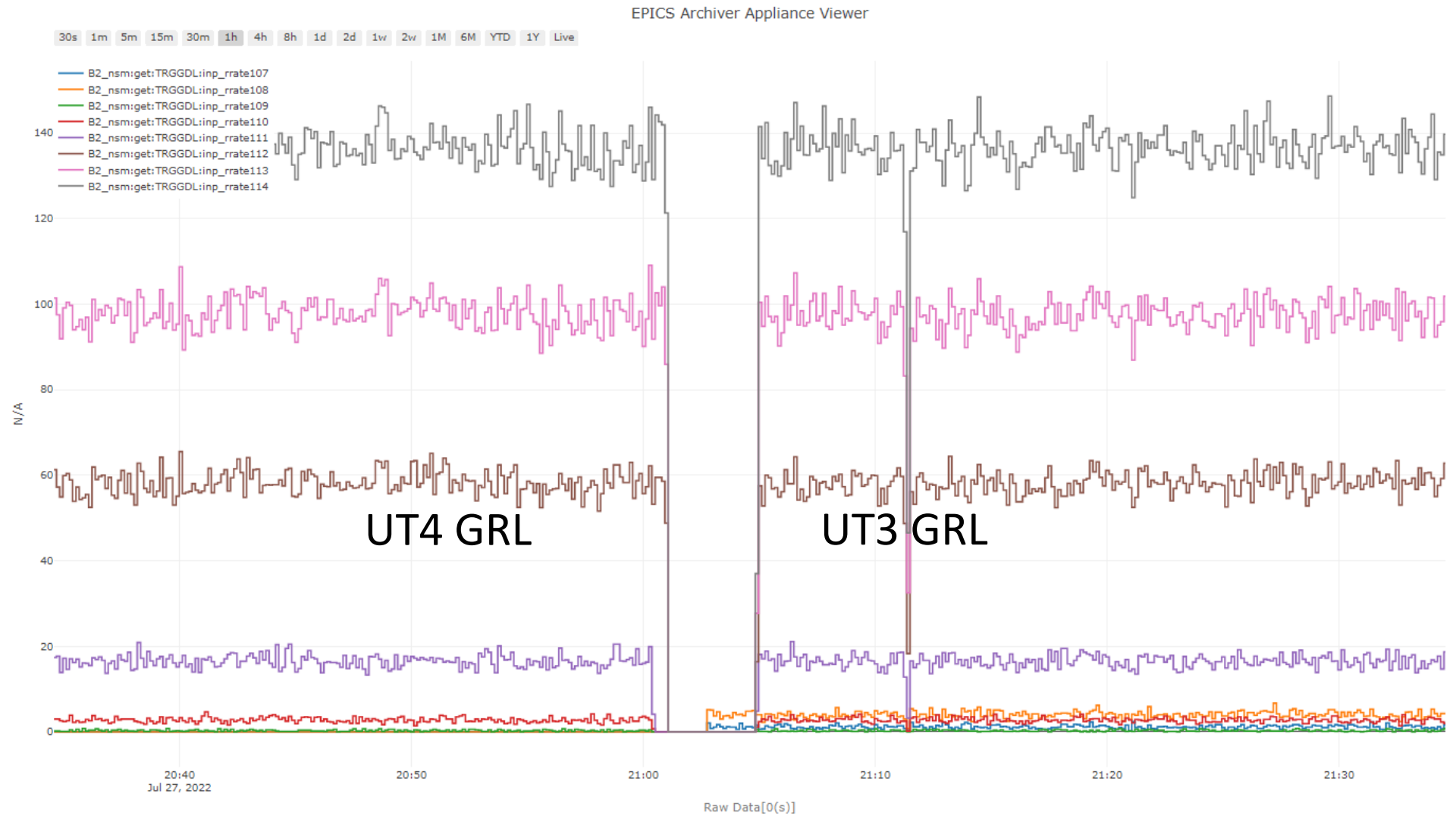
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B2_nsm:get:TRGGDL:inp_rrate114
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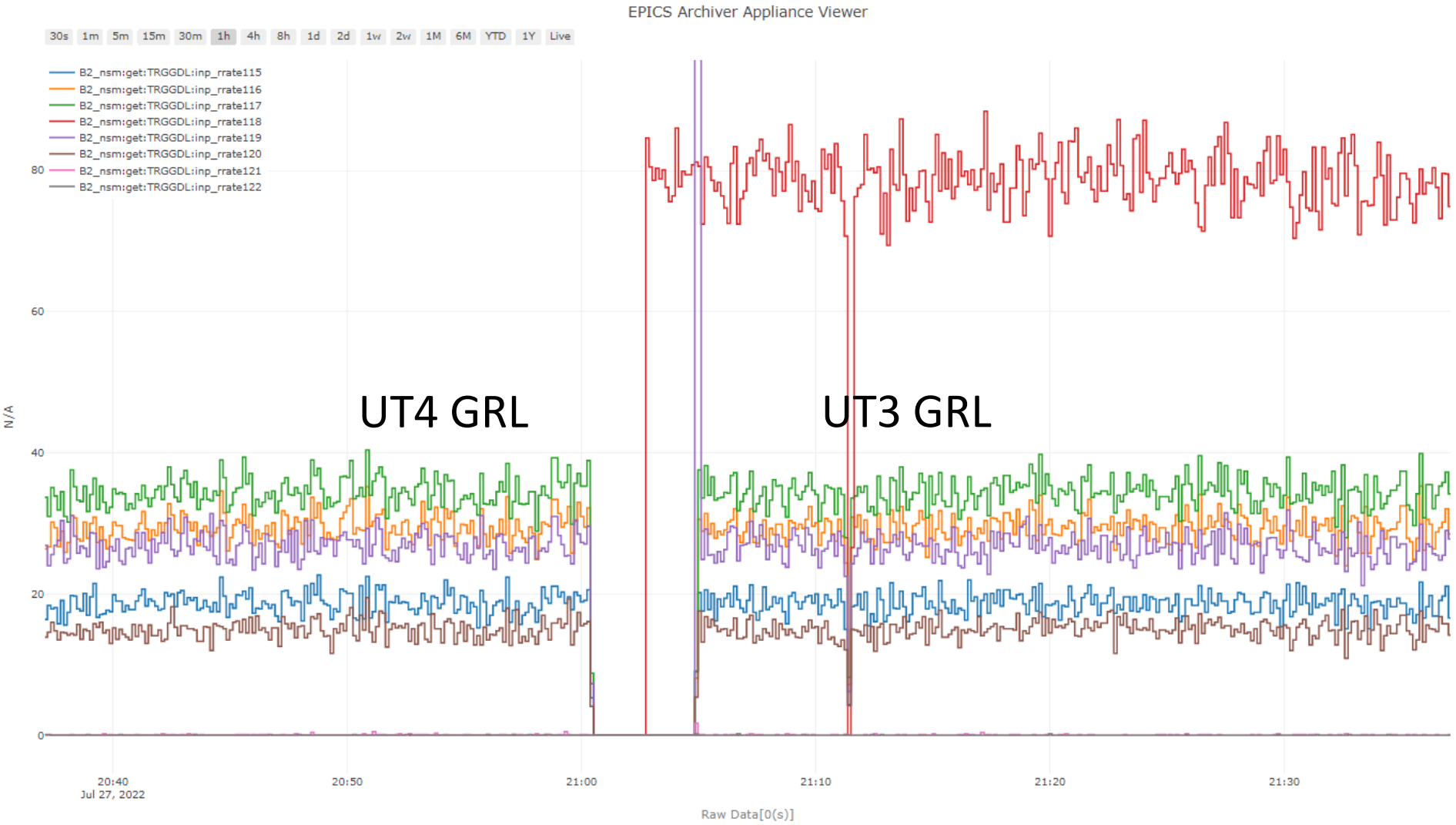
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B2_nsm:get:TRGGDL:inp_rrate119
B2_nsm:get:TRGGDL:inp_rrate120
B2_nsm:get:TRGGDL:inp_rrate121
B2_nsm:get:TRGGDL:inp_rrate122
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UT4 GRL
UT3 GRL
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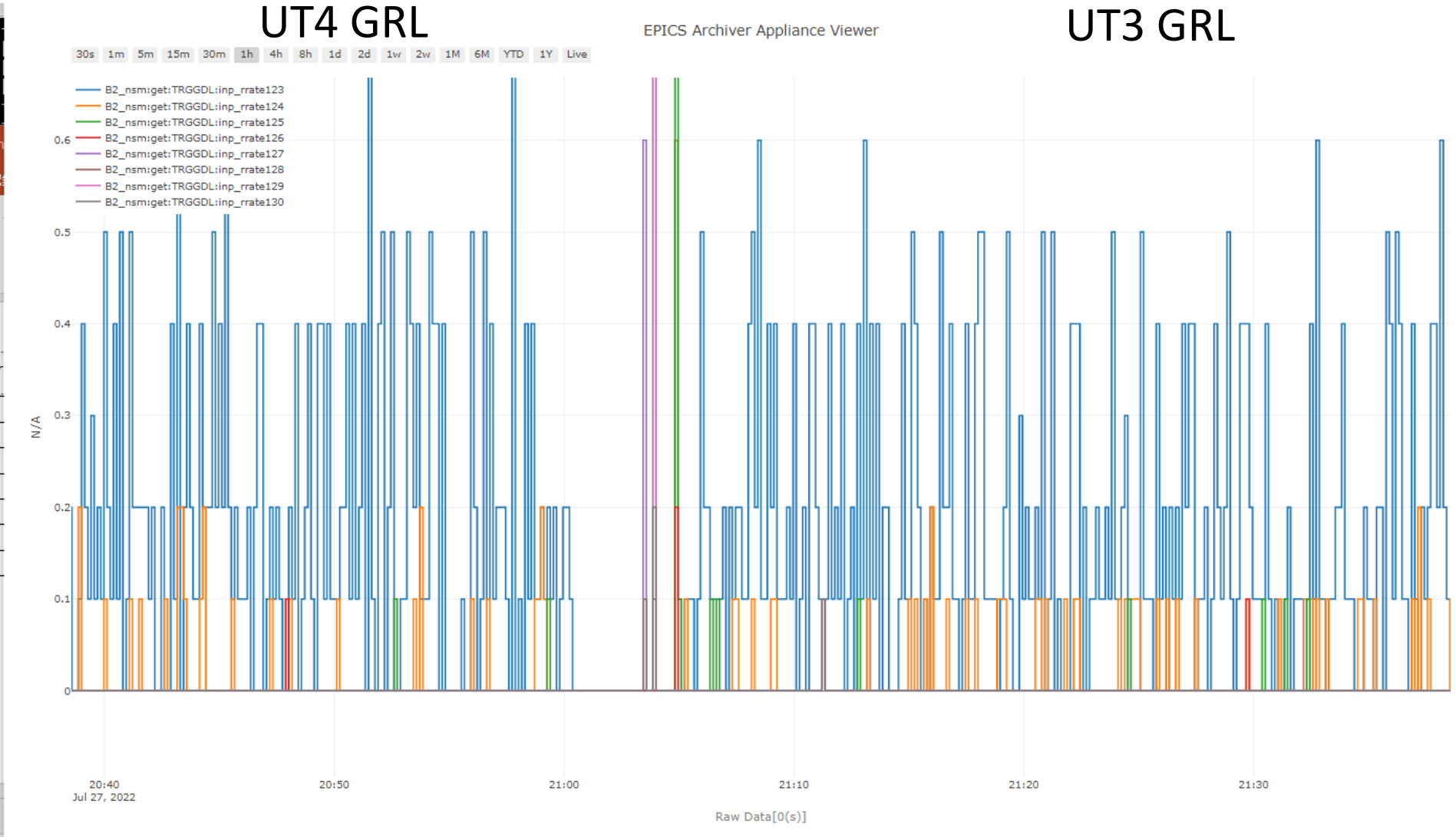
Rate check

UT4 GRL

UT3 GRL



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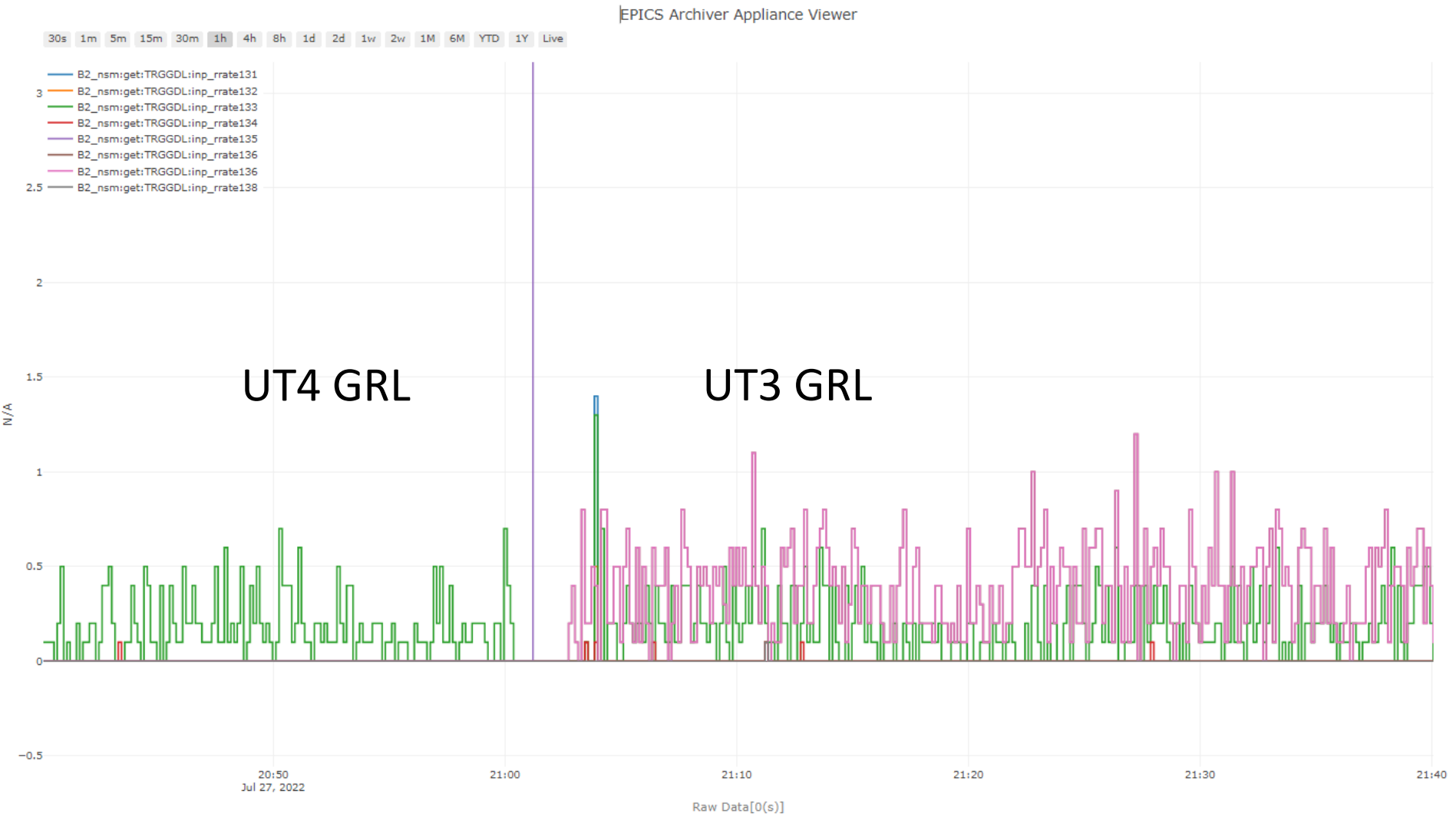
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