# UT4 production and UT5
2022/11/23
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# UT4 production

-Last report at weekly meeting, existing list of UT4s

-We plan to produce ~15 UT4s in this year and next year

-Price of UT4 is increasing from 3,000,000 JPY from 4,000,000 JPY by soaring.
There is no estimation how long does it take to purchase new FPGA from Xilinx.
-situation is getting serious and serious
-~10 FPGA(VU190) is purchased in 2022, for 2023 production

-If you can get additional funding to produce more module, it is very nice.
-thank you very much Myeongjae and Byung-Gu !
-At present there is no modules for new projects, displaced vertex etc.
KEK can not prepare money for that maybe.

# UT4 production

-List of UT4s

| module | #UT4 VU080 | #UT4 VU160 | #UT4 VU190 | #UT4 VU190 extended LVDS |
|---|---|---|---|---|
| TSF | 4 | 5 | | |
| TSF for LS2 | | | 9(2023-2024) | |
| 2D | | 4 | | |
| ETF | 1 | | | |
| 3DHough | | 4 | | |
| NN | | | 4(2022) | |
| GRL | 1 | | | 1(2023) |
| GDL | | 1 | | 1(2023) |
| ETM | | 1 | | |
| TOPTRG | | | 2 | |
| Spare, test bench | 4 | 1 | 1(2023-2024) | 2(2023) |
| Total | 10 | 17 | 16 | 4 |

# UT5: status

-Last report at weekly meeting

-Discussion has been started with company and Esys
  -Yun-Tsung's talk at Friday (as member of Esys)
  -KEK purchaced test board with versal FPGA and PAM4 interface, for FPGA candidate selection.
  New comer is very welcome for this new activity with test board.

-Time scale in Japanese physical year:
  -2022-: FPGA selection
  -2023-: prototype board ← depends on money
  -2024-: production ← depends on money

# Fix existing issues on UT4

-GTH transceiver is not working with 127MHz reference clock.
Laser from the transceiver is not brightening sometimes with some FW.
→Voltage of PLL is suspicious.
Check accuracy of the voltage carefully for UT5.

-VME communication is failed when UT4 is installed to VME crate.
→Need investigation with type of VME error and response to VME bus.
→Bad mechanical connection is one possibility, but the connector of VME<->UT4 itself is widely used commercial one and should be stable.

-Maximum optical speed is not achieved due to bit error or unstable link.
Operated with ~half of maximum rate (12Gbps/10Gbps for GTY/GTH).
→Only self-feedback test on single channel is done by company, when UT4 is constructed. Better to do more realistic test with two UT5s and full channels for UT5.
→Optimization of parameters of transceiver IP might help.

# New UT5 feature

-Versal or Vertex Ultrascale+ FPGA, with large resource (~5-10 times larger than UT4) and high optical speed (25-60Gbps) ?

→Present Versal do not have large resource.
At next year, a new Versal FPGA with ~4 times larger resources than UT4 VU190 will be published. It may be a good candidate.

→Present Ultrascale+ has ~4 times larger resource than UT4 VU190.
Optical speed is 32Gbps (no PAM4). It might be one candidate.

→With conventional protocol, 32Gbps is maximum.
With PAM4, 58Gbps is possible but latency may be increased.
They will check the latency and let us know.

| | Vertex Ultrascale VU190 (UT4) | Vertex Ultrascale+ XCVU19P | Vertex Ultrascale+ XCVU29P | Versal next year |
|---|---|---|---|---|
| Logic cell (K) | 2350 | 8938 | 3780 | ~9000 |
| Slice | 1800 | 3840 | 12288 | ? |
| Optical speed | 25Gbps | 32Gbps | 58Gbps | ? |

# Possible new logic on UT5

-Idea of new logic is very welcome to motivate UT5 production

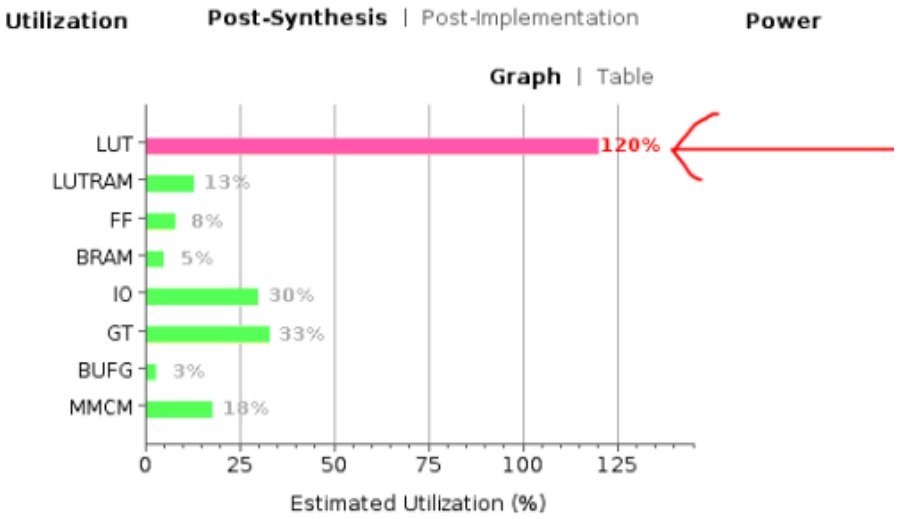
- -in general, large resource and high bandwidth are needed for better (complicated) logic

-For now, two practical idea: CDCTRG 2D and NN, GNN

- -increase hough mesh size of 2Dfinder from 160(ϕ) × 34(pt) to 320 × 68
- -better BG rejection performance with high BG, studied by Ping
- -machine learning related algorithm can be upgrade with versal I guess.

2D compile with 320 × 68

-More idea from all sub trigger is very welcome.



# Summary

-Additional ~15 UT4s will be produced in this and next year

  -no module for displaced vetex etc.: need more money from you!

-Discussion of UT5 has been started

  -testboard with versal is purchased at KEK. welcome new comer.

  -any comments/requests are welcome for new UT5 feature

  -any idea of new logic is welcome to motivate UT5