CDCTRG upgrade for LS2 and beyond

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Motivation

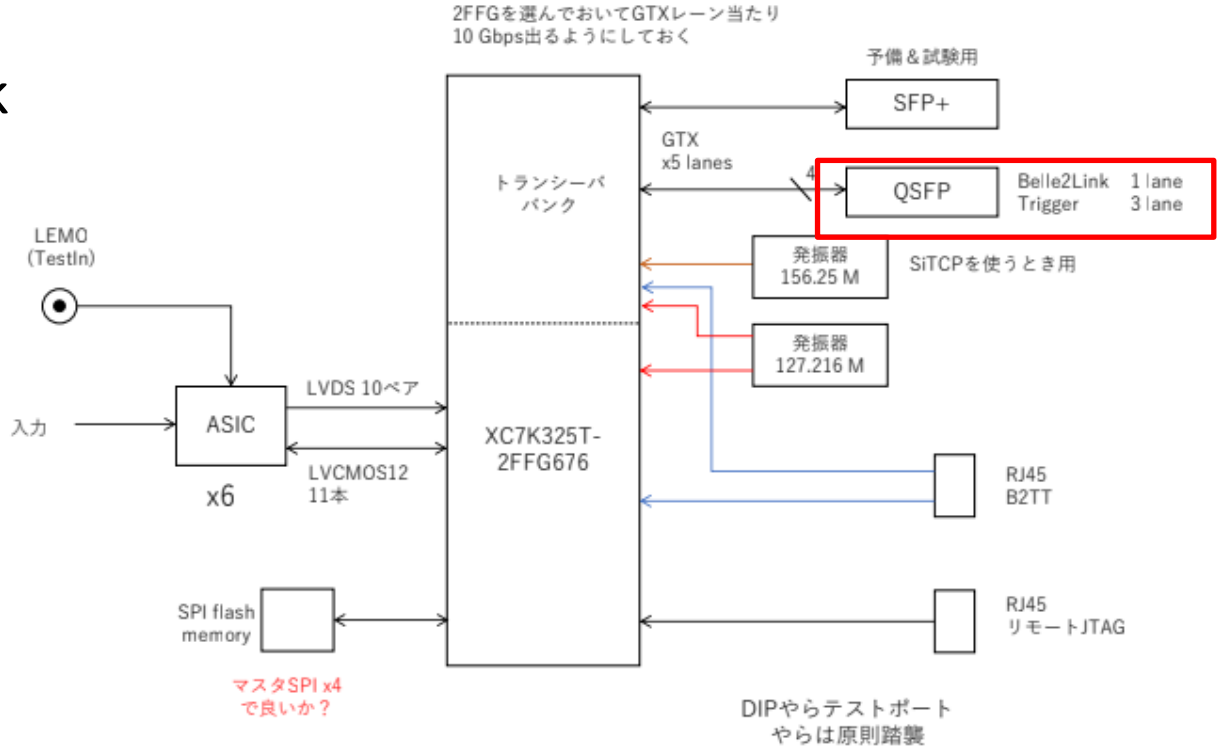
-We plan to update CDCTRG system in LS2, with upgraded CDCFE
  -feature
  -time schedule

Upgrade of CDCFE

-CDCFE hardware will be upgraded around LS2(~2026?),
before optical transceiver of CDCFE->CDCTRG is broken by radiation

-Bandwidth of optical transceiver will increase from 2.5Gbps to 10.3Gbps
->We can send more information from CDCFE to CDCTRG

-new CDCFE has a QSFP: 10Gbps × 4 lane GTX
- -2lane is for TRG
- -1lane is for Belle2link
- -1lane is spare



Upgrade of CDCFE and CDCTRG

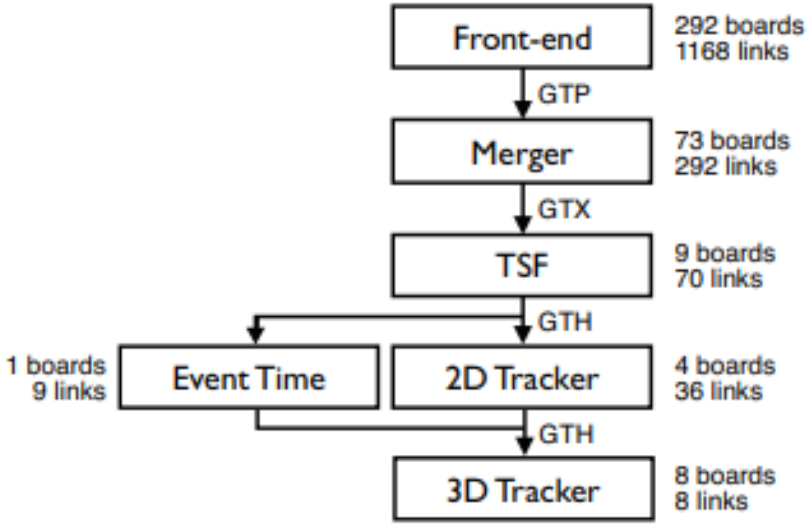
-Optical transceiver speed will be improved with new CDCFE

-To use the high speed, receiver side (MGR) need to be upgraded too

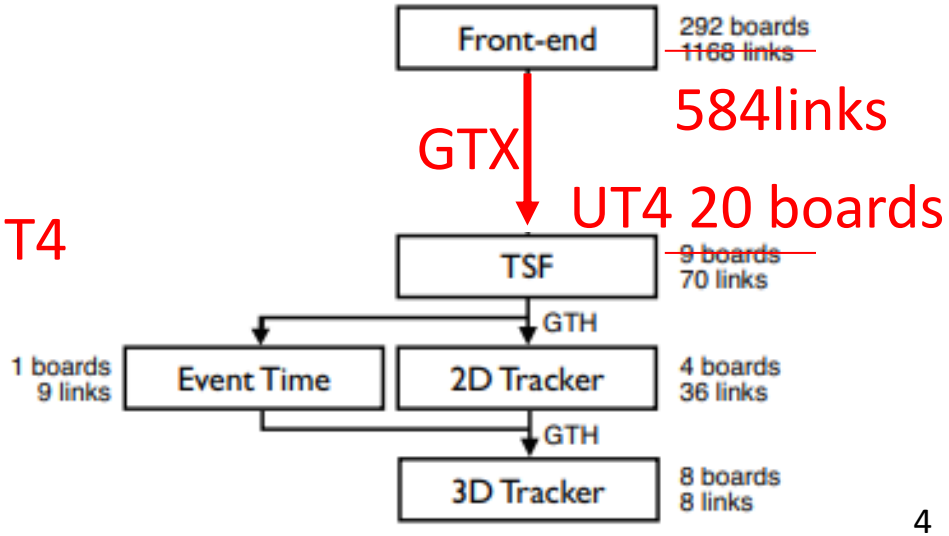
->We plan to bypass the MGR and connect TSF directly

	speed per lane	#lane per CDCFE<->TRG	#bit/32MHz/CDCFE
Present CDCFE	3.2Gbps (2.5Gbps with 8b10b)	4	256
New CDCFE	10.3Gbps (10Gbps with 64b66b)	2	512

Present configuration



New configuration



Merit of high speed

-With the higher speed, we can send TDC and ADC of all wires to CDCTRG

Figure 10: Part of CDC outer SL inside wire cell configuration [6].

Data from a CDCFE to CDCTRG

	data	#bit/32MHz/CDCFE
Present	-hitmap of 5/6 wires -tdc of part(~1/6) of wires (2ns) -fastest tdc among all wires -edge information -clock -total	48 (40)bit 5bit × 16wire=80 5bit × 16wire=80 10bit 9bit 227bit < 256bit
New	-hitmap of all wires -tdc of all wires (2ns) -adc of all wires (4bits) -clock -total	48bit 5bit × 48=240 4bit × 48=192 9bit 489bit < 512bit

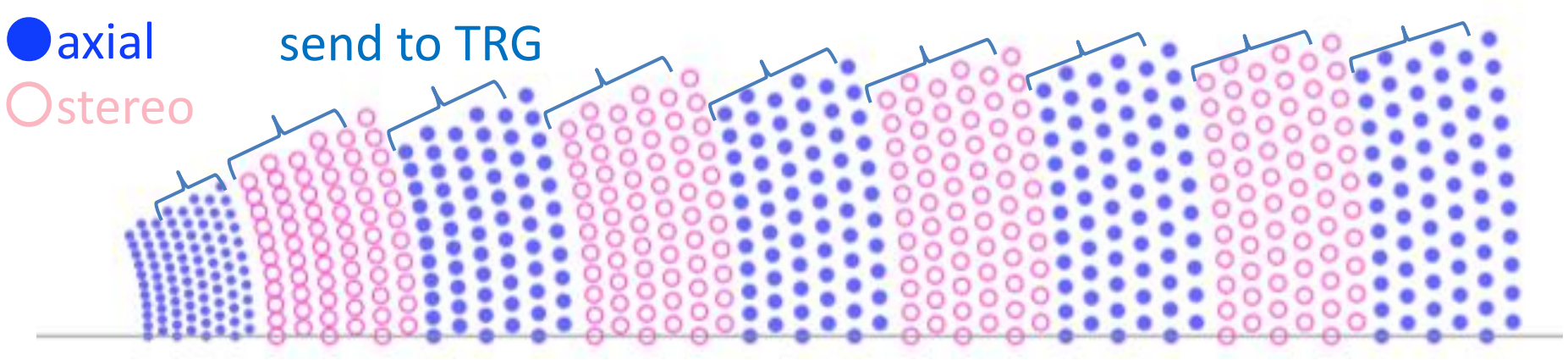
Wire hit existence

-Existence of hit (0:no hit 1:hit) is judged in each wire
  -judged by discriminator on CDCFE

-DAQ: receive the hit existence of all wires within 800ns timing window per an event

-TRG: receive the hit existence of part of wires (~80%, 5 of 6 layers in each super layer) every 32ns timing window

-TRG LS2: it is an option to send all wires
(it is not planned but possible based on the request with R&D)



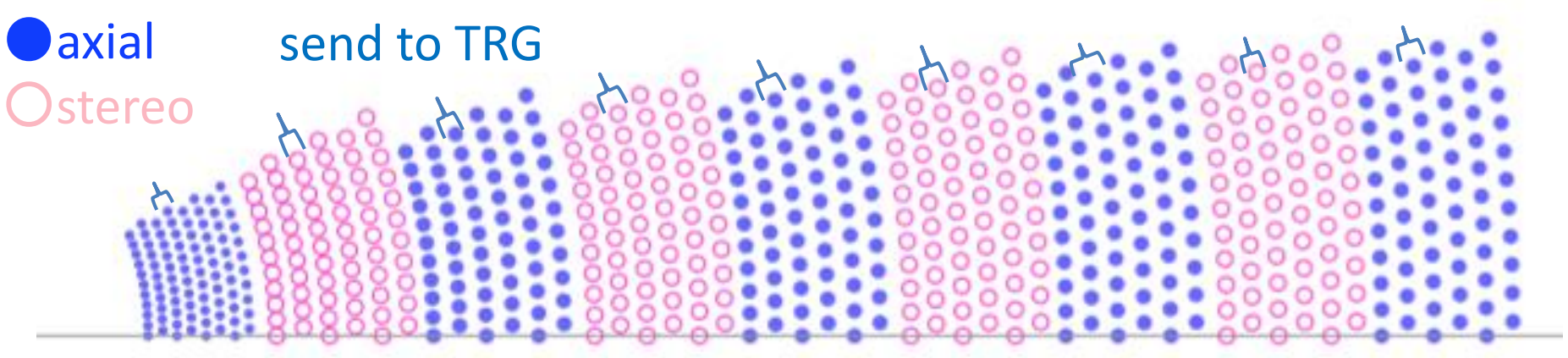
TDC

-Hit timing is measured in each wire
  -judged by discriminator + TDC on CDCFE

-DAQ: receive TDC with 1ns resolution of all wires within 800ns timing window per an event. The firstest and second firstest TDC sent.

-TRG: receive TDC with 2ns resolution of part of wires (~15%, 1 of 6 layers in each super layer) every 32ns timing window.
EventT0 is not known. Absolute value of TDC is meaningless.

-TRG LS2: it is an option to send all wires with 2ns resolution (~80% is planned, based on the request with R&D)



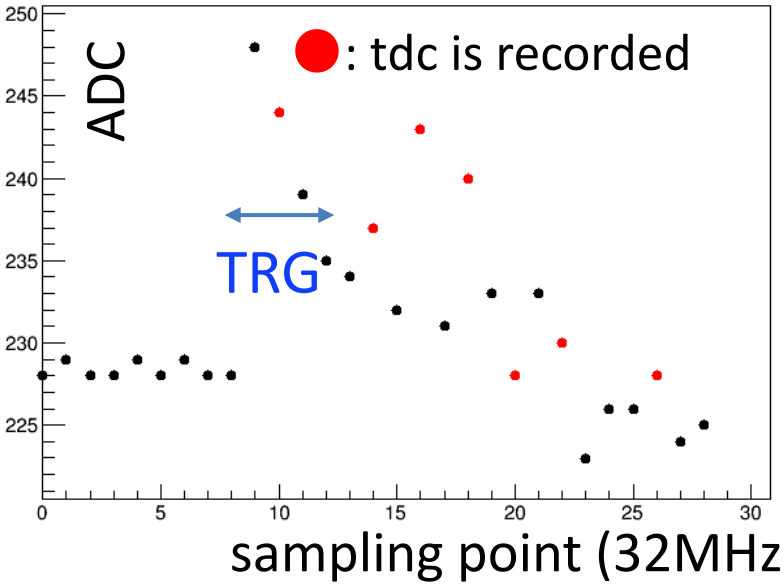
ADC

-Pulse height is sampled every 32MHz and digitized

-DAQ: receive ADC sum of
~25 points for all wire

-TRG: receive no ADC

Example of waveform data



-TRG LS1: receive ADC sum of ~3points for part of wires (~80%, 5 of 6 layers in each super layer) every 32ns timing window.
Resolution is just two bits.
(Just three flags. For example, ADC>5 or ADC>20 or ADC>500).

-TRG LS2: It is possible to add more points and output bits, based on the requests with R&D

Merit of high speed

-With the higher speed, we can send TDC and ADC of all wires to CDCTRG

-Great potential for BG reduction and efficiency improvement for future

-TDC: increase fitting points (x5) to improve z resolution

-ADC: crosstalk and noise reduction

-CDCTRG 2D track

●wire used for track fitting with tdc

CDC wire structure

present fitting

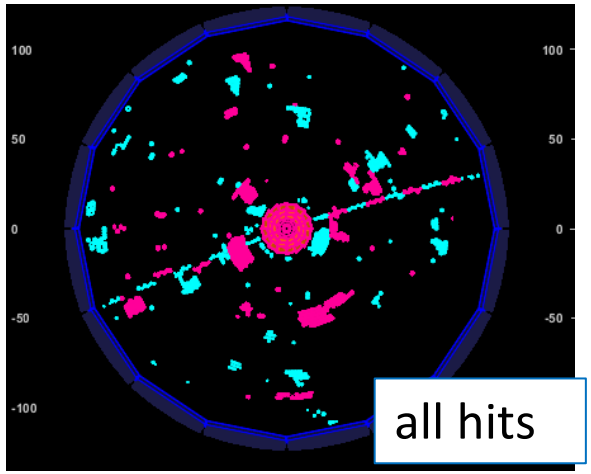
new fitting

●axial

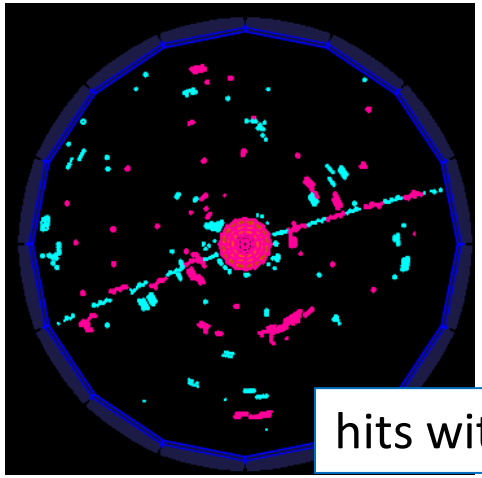
○stereo

◎

IP



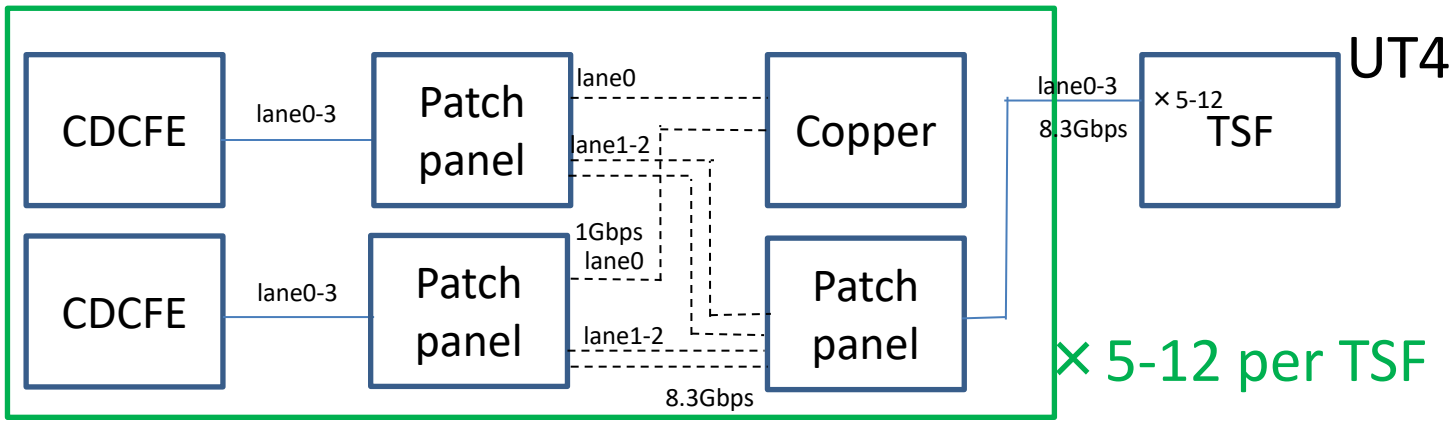
all hits



hits with ADC cut

New CDCFE<->TSF configuration

-Example of cable configuration to separate lane0(B2L) and lane1-2(TRG)



× 20TSF

patch panel
QSFP<->4 × SFP

	CDCFE	patch panel #MPO ch	TSF (UT4)
total#	300	450	20

cable	MPO CDCFE<-> Patch panel	SFP Patch panel <-> Patch panel	MPO Patch panel <-> TSF
total#	300	450	150

MPO cable
SFP cable

Time schedule

-2022-2024:
  -production of UT4
  -preparation of TSF firmware, CDCFE firmware
  -design of new logic, implementation (2D, NN, 3Dhough, any new idea)

-2025:
  -commissioning of new firmware with test bench

-2026(whenever optical module is broken?)
  -installation, commissioning with real setup

-2027
  -gradually use new 2D/NN/3DHough/any new logic for operation
  -priority of new logic is highly depending on operation situation

Time to design the new logic !

-Lets start the upgrade of all CDCTRG modules (2D/NN/3D/3DHough /displaced vertex/GNN) with new input information.
Feasibility study of the simulation is the first step.

-Proposed data format by Koga is below, but it is not final version.
If you have request from your study, it is very welcome.

-I am not sure if 2ns resolution is really needed for example.

Data from a CDCFE to CDCTRG

	data	#bit/32MHz/CDCFE
New	-hitmap of all wires -tdc of all wires (2ns) -adc of all wires (4bits) -clock -total	48 5 × 48=240 4 × 48=192 9 489 < 512

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On-going feasibility study with new information from CDCFE

Module	Developper
CDCFE	Koga (but no progress recently..)
TSF	Koga (but no progress recently..)
2D	Koga
3D	Sudo
NN	Liu, Christian
3DHough	no
Displaced vertex	no?
GNN	Lea, Phillip
Short tracking	no
Any other	no

Join of you and new comer is very welcome !

Summary for LS2

-We plan to update CDCTRG system in LS2, with upgraded CDCFE
- -directly connect TSF to CDCFE
- -input information from CDCFE to CDCTRG will be increased ~twice

-It is time to design all CDCTRG logic with the new input information!
- -lets start the feasibility study
- -any idea is possible
- -your and new students' joining is very welcome

beyond LS2

-There is no practical upgrade plan beyond LS2 yet

-we have many things to do before that..

-maybe, after finishing R&D of present activities, we can consider more.

-Upgrade of hardware (UT5) will proceed continuously to realize possible new logic in future

-Some ideas in my mind for brainstorming:

-upgrade of core logic with new hardware(UT5,UT6) is straightforward

-Combination of VXD and CDC trigger is attractive, after upgrade of VXD

-If luminosity will be stable, it is another option to develop and test new technique for next generation experiments (BelleIII??)

-High precision tracking with extremely large latency (~100μs) for example:
I think it will be not so difficult to prepare large circular buffer on detector FE

backup

Needed hardware and (very) rough cost

-Additional ~10 UT4 boards
  - ~25,000 $ × 10 = ~250,000 $

-The followings are needed for CDCFE upgrade commonly
(even without TRG upgrade)

-Additional ~100 patch panel (or split optical cables)
  - ~300 $ × 100 = ~30,000 $

-Additional optical cables
  -not estimated yet

-New optical transceiver on CDCFE detector side (not Ehut TRG side)
  - ~300 $ × 300 = ~90,000 $

CDC dead channel treatment

-TSF hit rate increased as expected

-both mask case, reason unknown but other TSF MGR3-X rate decrease.