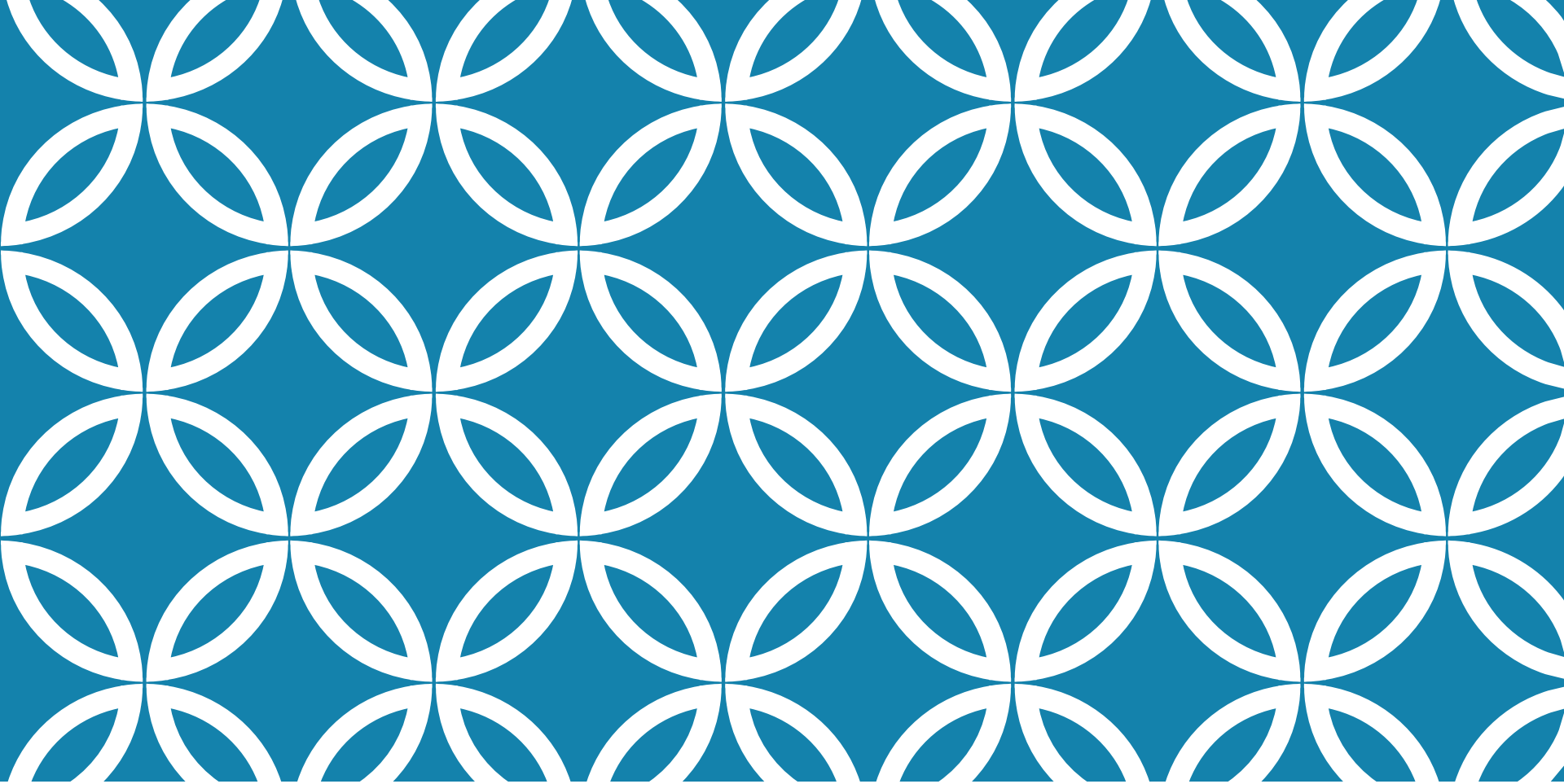
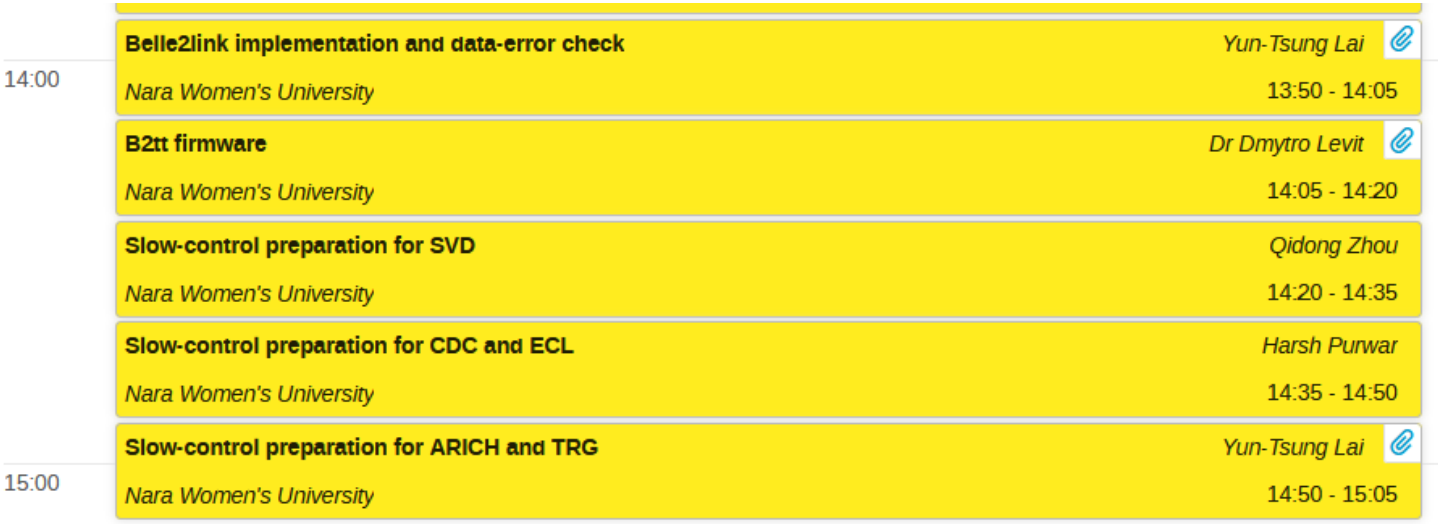


OVERALL STATUS AND COMMISSIONING IN LS1

S. Yamada (KEK)

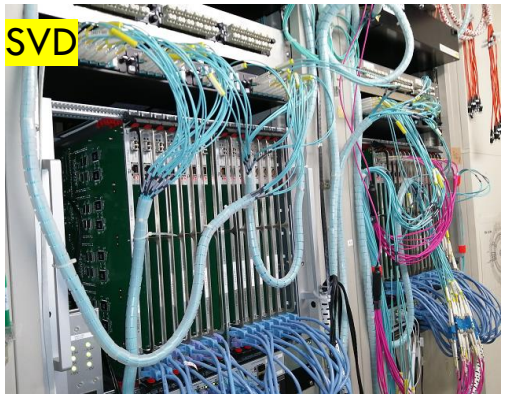
OVERALL STATUS

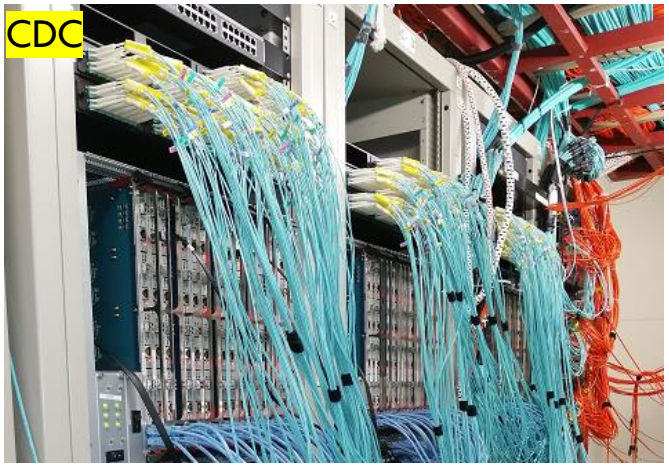
- Basic firmware and software for readout was prepared in 2022
  - TOP and KLM readout system was replaced in 2022 summer shutdown.
  - ARICH readout system was replaced in 2022/23 winter shutdown.
- Readout system for other subsystems will be replaced in LS1.

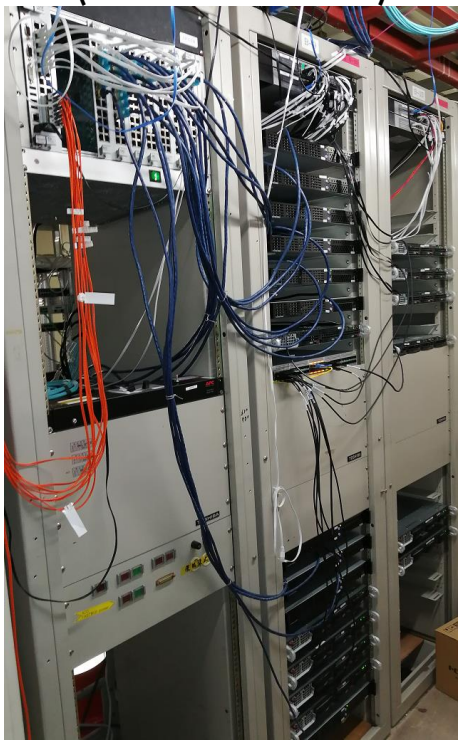


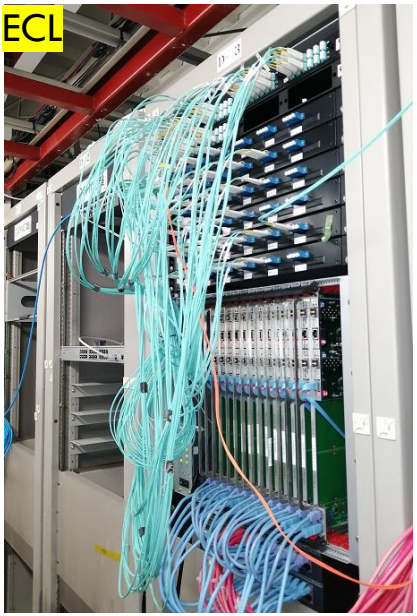
INSTALLATION WORK FOR SVD, CDC, ECL AND TRG IN LS1

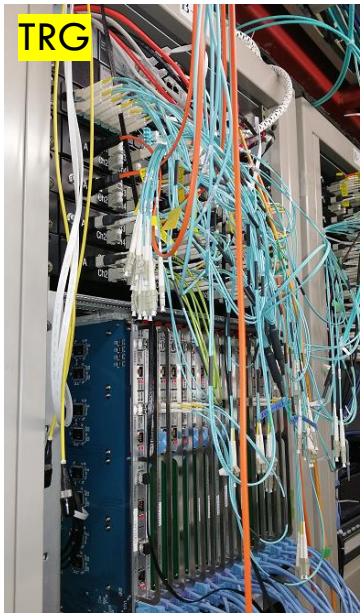
Readout PCs
(PCIe40 servers)











- Slow-control library and local run GUI for each sub-detector has been developed.

-> Now commissioning is ongoing.

COMMISSIONING STATUS

	commissioning status	Observed issues
SVD	➢ A readout test with FADC when IBBelle was running in Jul. and Sep. ➢ Currently, FTB dummy data are used for commissioning.	➢ Data corruption at zs=2.2 (Maybe, not SVD specific trouble)
CDC	➢ Readout test was done when LV was ON. ➢ High-occupancy test was performed.	➢ No serious trouble
TOP	➢ Study of feature-extraction in ROPC by TOP experts.	
ARICH	➢ Not available	
ECL	➢ Used most frequently for commissioning	➢ Persistent BUSY (fixed) ➢ Empty data FIFO
KLM	➢ Dummy data from FEEs will be used for commissioning.	
TRG	➢ Sometimes included in global DAQ in July	➢ No serious trouble (but only short time test)

PCIE40 STRESS TEST WITH LARGER EVENT-SIZE(1)

† : including DAQ overhead

	How to increase event size	Event size
SVD	- Lowering Zs threshold - Dummy data produced by FTB	- 105.4kB/eve† (Zs = 2.4) (2022b physics run : 30-55kB)
CDC	- Occupancy is increased by changing threshold of CDC FEEs	- 105kB/eve† (at peak threshold) (2022b physics run : 20-40kB)
TOP	- Injecting calibration pulses.	
ARICH	- Occupancy is increased by making ARICH HV OFF.	
ECL	- Threshold can be changed - Waveform data can be sent.	
KLM	- Dummy data from KLM FEE.	- 24kB/eve† (2022b physic run : 1-3kB)
TRG	Fixed event size but pre-scale parameter for detailed GDL information can be changed.	

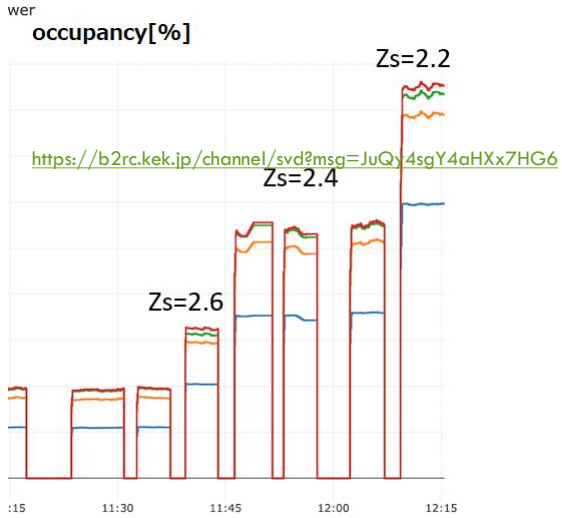
https://dqm.belle2.org/past_runs/show_hlt.htm?rootfile=hlt_exp26/dqm_e0026r001841.root&reffile=refHisto_BEAM.root&canvasfile=hlt_exp26_canvas/dqm_e0026r001841_canvas.root#/phase3/DAQ_main.json

PCIe40 Stress test with larger event-size(2) : Plan

	Status and Plan	Realistic large event for HLT test ?
SVD	- Tested on Sep. 7(Zs thr.) - Dummy data test in preparation	- Zs thr. : Increase the # of hits - Dummy data in FTB
CDC	- Tested on Oct. 28. - CDC DAQ is not available now -> 2023 Spring ?	- Increase the # of hits
TOP	- After the PMT replacement is finished. -> 2023 Spring ?	- Increase the # of hits
ARICH	- After reinstallation of endcap. -> 2023 autumn ?	- Increase the # of hits
ECL	- It can be done now.	- Increase the # of hits (changing threshold) - Change the fraction of events which contains waveform data
KLM	- Tested in 2021 winter and summer	- Dummy data from KLM FEEs :
TRG	- Fixed size but prescale factor might be changed.	

SVD OCCUPANCY IN THE TEST(1)

Exp27 run	Zs (sigma)	Input trigger [kHz]	Occupancy
734	2.8	30	L3 1.1%, L6 2.0%
735	2.6	30	L3 2.0%, L6 3.3%
738	2.4	30	L3 3.6%, L6 5.6%
739	2.2	30	L3 6.0%, L6 8.6%
740	2.0	30	No data due to ferr from FTBs
742	2.1	30	No data due to ferr from FTBs



https://b2rc.kek.jp/channel/svd?msg=JuQy4sgY4aHXx7HG6

- With zs <=2.1, data cannot be taken due to ferr from FTB. (FTB buffer full ?
- Occupancy distribution in different SVD layers are oppoite to the real situation.
  - Real : L3 occu. > L6 occu.

Katsuro-san's estimation of occupancy

Layer	Occupancy (random) [%] beam BG(19ac) (ZS5)		physics/ random		Occupancy (physics) [%] (ZS5)		ZS3/ZS5		Occupancy (physics) [%] w/o noise (ZS3)		Noise occupancy [%] (ZS3)		Translated occ. [%] (ZS3)
3	2.93	×	2.00	=	5.86	×	1.5	=	8.79	+	1.0	=	9.79
4	1.40		2.00		2.80		1.5		4.20		1.0		5.20
5	1.08		2.00		2.16		1.6		3.46		1.0		4.46
6	0.70		2.00		1.40		1.7		2.38		1.0		3.38

https://b2rc.kek.jp/channel/svd?msg=gBB7en63od5cYpbgS

SVD OCCUPANCY IN THE TEST(2)

DATA CORRUPTION IN THE SVD TEST

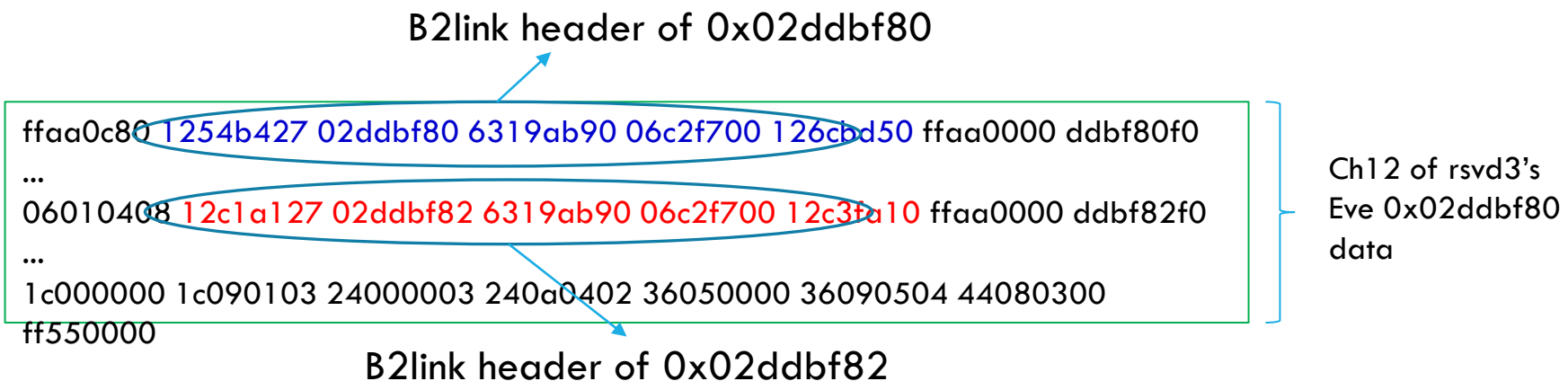
- With zs=2.2, we tried to perform a long term test but DAQ stopped in 1-2 hours.
- Data corruption was observed.

Error message : header and trailer mismatch

[2022-09-08 17:45:05] [DEBUG] RSVD3 : dmastart 2095956[FATAL] thread 2 : ch=12 : ERROR_EVENT : mismatch(finesse 12) between header(ctime 0x1254b427 eve 0x02ddbf80) and footer(ctime 0x36090504 eve_crc16 0x44080300). Exiting... : exp 27 run 759 sub 0 : des_ser_PCIe40_main.cc void checkUtimeCtimeTRGType(unsigned int*&, int) 643

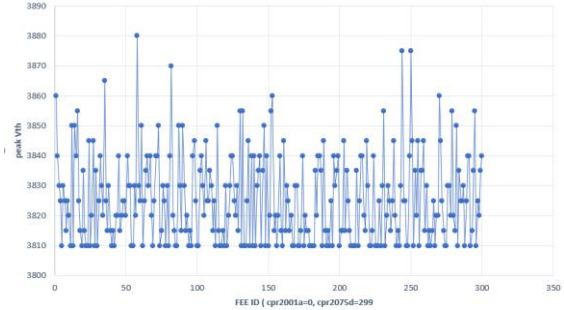
Example : Run759

In data of event 0x02ddbf80, data of 0x02ddbf82 was stored.



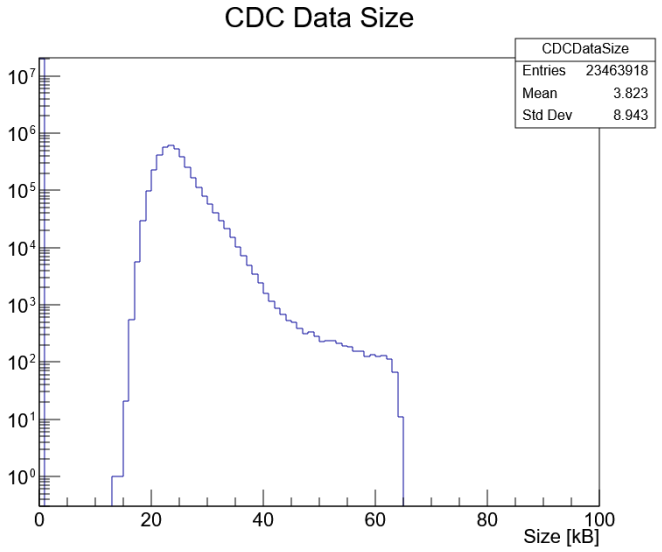
CDC HIGH-OCCUPANCY TEST(1)

- By changing CDC FEE threshold, high-occupancy readout test was performed on Oct. 28
  - There is a threshold with maximum event size.



	Default Threshold [kB]	Peak threshold [kB]
rcdc1	1.5	16.2
rcdc2	1.5	16.5
rcdc3	1.5	14.9
rcdc4	1.5	15.7
rcdc5	1.4	11.3
rcdc6	1.4	15.2
rcdc7	1.4	15.2
total	10.2	105.0

https://dqm.belle2.org/past_runs/show_hlt.htm?rootfile=hlt_exp26/dqm_e0026r001841.root&reffile=refHisto_BEAM.root&canvasfile=hlt_exp26_canvas/dqm_e0026r001841_canvas.root#/phase3/DAQ_main.json



CDC HIGH-OCCUPANCY TEST(2)

- Input : 30kHz Poisson trigger
- Data flow was fine. : 27kHz output due to SVD trigger holdoff limitation
- run 1226 : Persistent BUSY from rcdc1 after 3hours of data-taking
- run 1238 : Persistent BUSY after 5.5 hours data-taking.

When persistent BUSY occrrured in run1226, # of arrived events were the same for all channels.
So, it is likely to be the same error as observed in recl2.
->
Once CDC DAQ is available, we will test again with updated firmare.

```
1=26200 50800003  min=10
0=02040 74000001  busy=none [pcie40a]
 0=02041 90000400  bound=none
  0=02050 aa2baeea  ready tag=2862826 [20]
  1=02051 aa2baeea  ready tag=2862826 [120]
  2=02052 aa2baeea  ready tag=2862826 [276]
```

FAKE ERROR SIGNALS IN LS1 (1)

- Not so frequent during LS1 -> 3 errors in ECL

Fake error in ch2 data in recl3 on Aug. 17

ctime

```
[2022-08-17 18:19:25] [DEBUG] RECL3 : thread 0 : 00000090 : 00000000 004d3c17 00007755 ff550000 ffaa0200 004d3c17 00000000 62fcb29d
[2022-08-17 18:19:25] [DEBUG] RECL3 : thread 0 : 00000098 : 06c1f500 004e4b90 000013ff a5100004 001f0030 00000000 00000000 a5100004
[2022-08-17 18:19:25] [DEBUG] RECL3 : thread 0 : 000000a0 : 001f0030 00000000 00000000 a5100004 001f0030 00000000 00000000 a5100004
[2022-08-17 18:19:25] [DEBUG] RECL3 : thread 0 : 000000a8 : 001f0030 00000000 00000000 a5100004 001f0030 00000000 00000000 a5100004
[2022-08-17 18:19:25] [DEBUG] RECL3 : thread 0 : 000000b0 : 001f0030 00000000 00000000 a5100004 001f0030 00000000 00000000 a5100004
[2022-08-17 18:19:25] [DEBUG] RECL3 : thread 0 : 000000b8 : 001f0030 00000000 00000000 a5100004 001f0030 00000000 00000000 a5100004
[2022-08-17 18:19:25] [DEBUG] RECL3 : thread 0 : 000000c0 : 001f0030 00000000 00000000 004d3c17 0000f4f7 ff550216 ffaa0300 004d3c17
```

In this fake event, 3 errors were reported according to event trailer.

- CRC error
- Event # jump
- Ctime mismatch between hdr and trl

```
data_check_NG_ch(1) <= crc16_check_NG;
data_check_NG_ch(2) <= tt_tag_check_NG;
data_check_NG_ch(3) <= tt_tag_crosscheck_NG;
data_check_NG_ch(4) <= tt_ctime_check_NG;
data_check_NG_ch(5) <= exprun_check_NG;
```

However, ctime in hdr and trl are same.

FAKE ERROR SIGNAL(2) : REPORTED "FAKE" ERROR TYPE

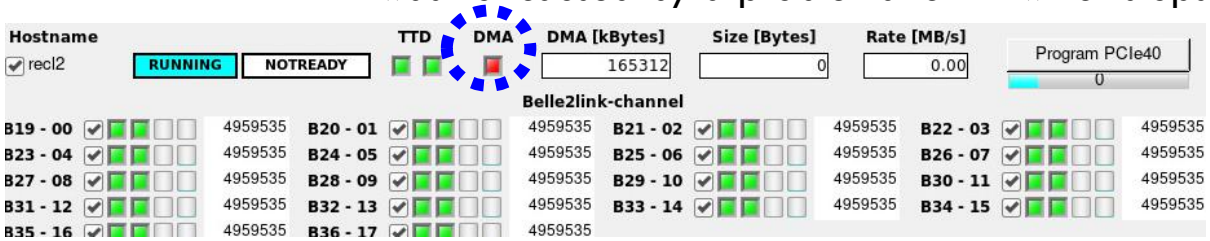
ROPC	Time	Channel #	Reported error	# of fake error events at the time
relc3	2022.5.11 18.15	ch16	Exprun, event # jump	1
relc3	2022.5.11 18.31	ch16	Exprun, event # jump	1
relc3	2022.7.13 15:34	ch6	Exprun, CRC error, event # jump, ctime mismatch	4
relc3	2022.7.17 09:04	ch4	Exprun, CRC error, event # jump, ctime mismatch	4
relc3	2022.8.15 18:19	ch4	CRC error, Event # jump	2

Need to keep running ECL to reproduce fake-error events.

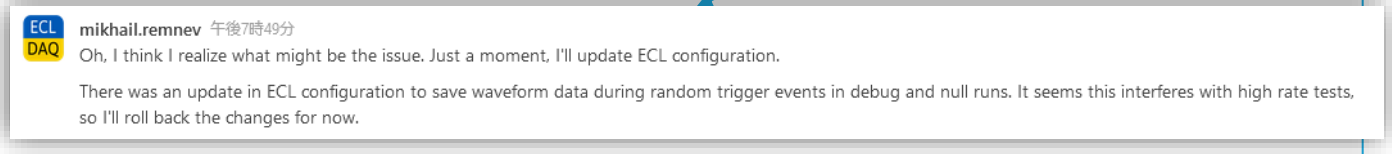
YunTsung provided PCIe40 firmware with signaltap file to investigate this in detail.
- I take over this but I'm sorry that I have not started to use it yet.

ECL PERSISTENT BUSY (1) : SYMPTOM

- Exp27 run24-34
- Persistent busy from ECL PCIe40 was observed a few minutes after a run start.
  - Data reached STORAGE but DAQ soon stopped due to the BUSY signal
    - -> It was not caused by network-connections of DAQ processes
  - BUSY came from DMA FIFO not from input FIFO
    - -> It was not caused by a problematic FEE which stops sending data




```
statlink version 3 (20210107) / PCIE40 firmware version 15.1
memory: OK | ttd: UP |  ttd clk: UP | run=: 34 | trg: 0 | trg type: 7
PLLs:LOCKED | B2L:READY (rx:111 tx:11) | DMA:FULL ( 165312.5kB)
No fee flag is specified
(00)   b2l=UP (gbt=UP rx=UP tx=UP rxsta=READY txsta=READY mask=UNMASK)
(00)   event=4959535   total=1571884.6kB (avg=316.9419B last=242  max=5310
B)
(00)   full=0 check=NG rxcrcerr=1333, check=0
(00)   no b2link error
```



ttd11 $ ttaddr -64 -p

```
0=05040 54000001  busy=none [pcie40a]
 0=05041 70000000  bound=none
  0=05050 8a359941  ready tag=3512641
  1=05051 8a359941  ready tag=3512641
  2=05052 8a359941  ready tag=3512641
  3=05053 8a359941  ready tag=3512641
  4=05054 8a359941  ready tag=3512641
  5=05055 8a359941  ready tag=3512641
  6=05056 8a359941  ready tag=3512641
  7=05057 8a359941  ready tag=3512641
  8=05058 8a359941  ready tag=3512641
  9=05059 8a359941  ready tag=3512641
  10=0505a 8a359941  ready tag=3512641
  11=0505b 8a359941  ready tag=3512641
  12=0505c 8a359941  ready tag=3512641
  13=0505d 8a359941  ready tag=3512641
  14=0505e 8a359941  ready tag=3512641
  15=0505f 8a359941  ready tag=3512641
 1=05042 7000fffc  bound=none
  0=05060 8a359941  ready tag=3512641
  1=05061 8a359941  ready tag=3512641
  2!05062 8a000000  ready tag=0
  3!05063 8a000000  ready tag=0
```

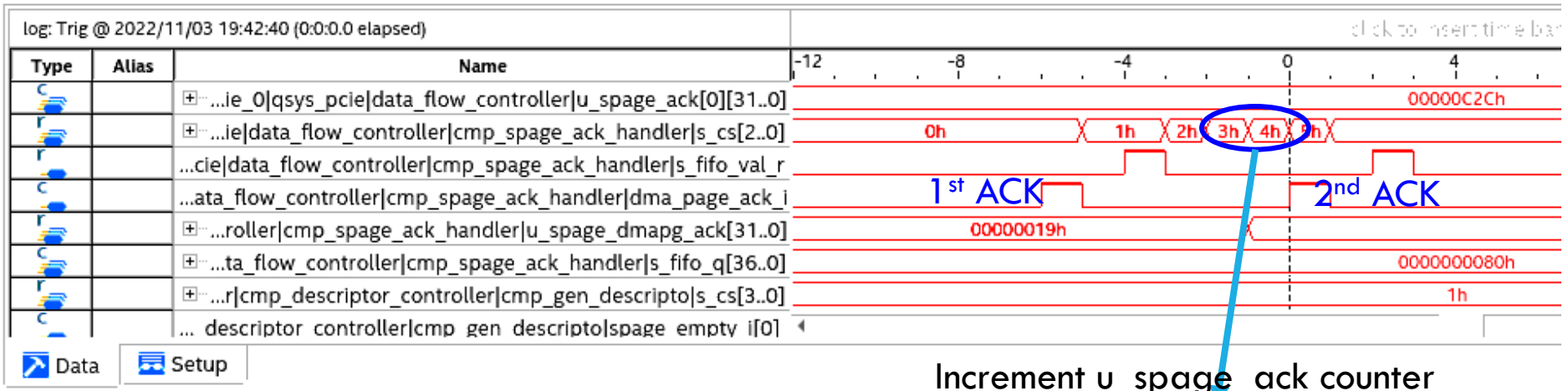
- ECL FEE sometimes sends waveform data of 5kB event/link (# of link per ECL PCIe40 is 18 at most)
- After Mikhail disabled this feature, this BUSY does not happen

ECL PERSISTENT BUSY(2) : DMA ACK SIGNAL IS IGNORED

- After the 1st ACK signal from PCIe core, u_spage_dmapg_ack is incremented. -> O.K.

(I suppose that this ack counter is what driver software uses to decide to read a new superpage.)

- However, after 6clock cycles, another ACK signal arrived and no ACK counter incrementation Happened. -> State machine stayed in IDLE(=0).



Increment u_spage_ack counter

```
when INCREASE_DMA_PAGE_CNT =>
--          u_spage_dmapg_ack <= u_spage_dmapg_ack + 1;
          s_cs              <= CHECK_SPAGE_STATUS;
        ------------------------------------------------------------------------
        -- Check if I pushed the number of DMA page available for the super
        -- page, if yes increase the superpage counter
        ------------------------------------------------------------------------
when CHECK_SPAGE_STATUS =>
          if (u_spage_dmapg_ack = u_dma_pg_avl) then
            u_spage_ack       <= u_spage_ack + 1;
            u_spage_dmapg_ack <= (others => '0');
          end if;
          s_cs <= STORE_CNTS;
```

qsys/hdl/data_flow_controller/spage_ack.vhd

Recently, we made pull-request to modify PCIe40 firmware with reduced the # of states in the state machine to detect 2nd ACK properly in IDLE state.

->

We have not observed the persistent BUSY issue with the update fw this month.

https://stash.desy.de/projects/BIDU/repos/firmware/pull-requests/94/overview

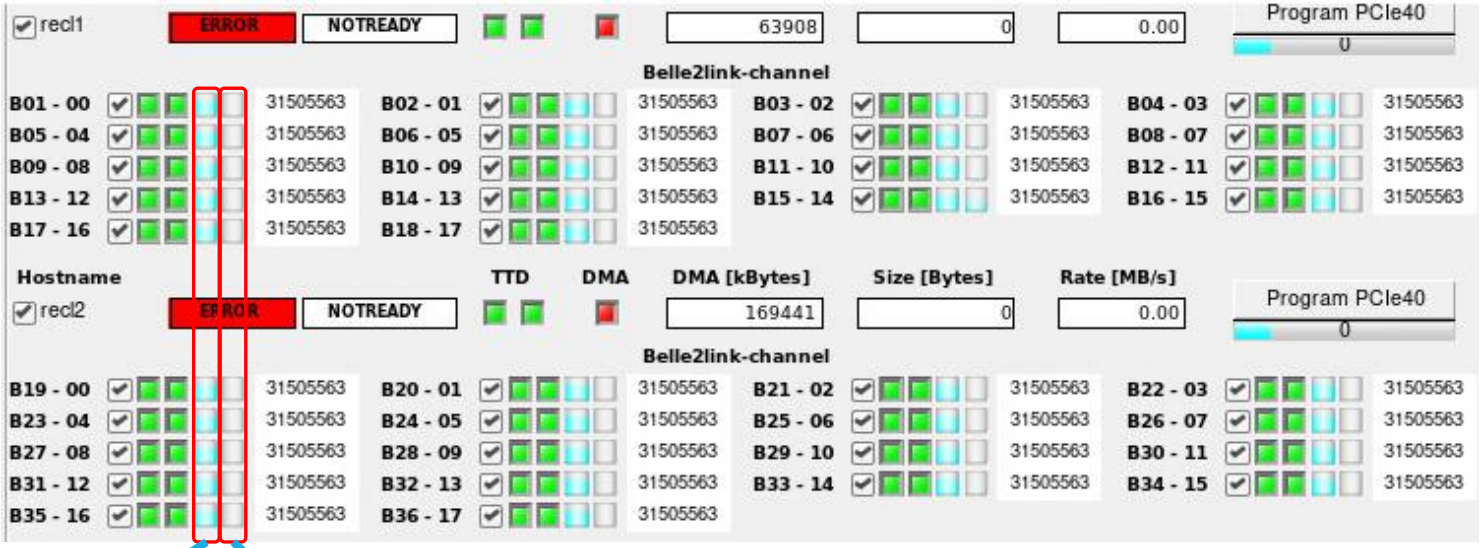
EMPTY DATA-FIFO ERROR (1) : SYMPTOM

- After the update PCIe40 firmware for the persistent BUSY issue, another error was observed in hours of data-taking.
- Same 256bits pattern repeated in channel data slot.
- Event # in header was smaller than the prev. event.

```
[2022-11-11 01:24:11] [FATAL] RECL2 : thread -1 : recl2 ch=0 : ERROR_EVENT : Invalid event_number. Exiting...: cur 32bit eve 45046175 preveve 45046283 for all channels : prun 113585920 crun 113585920
[2022-11-11 01:24:11] [DEBUG] state transit : RUNNING >> ERROR
[2022-11-11 01:24:11] [DEBUG] RECL2 : src/des_ser_PCIe40_main.cc void printEventNumberError(unsigned int*&, unsigned int, unsigned int, int, int) 320
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 00000000 : 00000416 7f7f0438 06c52f00 02af599f 201c8637 636d25aa 00000000 00000000
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 00000008 : 00000038 0000006f 000000a5 000000de 00000113 00000149 00000181 000001b9
...
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 00000038 : ffaa009f 201ea790 00001fff 90100004 201f00a8 201c8637 02af599f 636d25aa
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 00000040 : 06c52f00 201ea790 00001fff 90100004 201f00a8 201c8637 02af599f 636d25aa
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 00000048 : 06c52f00 201ea790 00001fff 90100004 201f00a8 201c8637 02a                25aa
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 00000050 : 06c52f00 201ea790 00001fff 90100004 201f00a8 201c8637 02a   ch0          25aa
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 00000058 : 06c52f00 201ea790 00001fff 90100004 201f00a8 201c8637 02a                25aa
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 00000060 : 06c52f00 201ea790 00001fff 90100004 201f00a8 201c8637 02af599f 636d25aa
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 00000068 : 06c52f00 201ea790 00001fff 90100004 201f00a8 02af599f ff550000 ffaa019f
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 00000070 : 201ea650 00001fff 90100004 201f00a8 201c8637 02af599f 636d25aa 06c52f00
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 00000078 : 201ea650 00001fff 90100004 201f00a8 201c8637 02af599f 636              52f00
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 00000080 : 201ea650 00001fff 90100004 201f00a8 201c8637 02af599f 636   ch1        52f00
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 00000088 : 201ea650 00001fff 90100004 201f00a8 201c8637 02af599f 636              52f00
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 00000090 : 201ea650 00001fff 90100004 201f00a8 201c8637 02af599f 636d25aa 06c52f00
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 00000098 : 201ea650 00001fff 90100004 201f00a8 201c8637 02af599f 636d25aa 06c52f00
[2022-11-11 01:24:11] [DEBUG] RECL2 : thread -1 : 000000a0 : 201ea650 00001fff 90100004 201c8637 ff550000 ffaa029f 201ea8e0 00001fff
```

EMPTY DATA-FIFO ERROR (2) : SYMPTOM

- On GUI, length FIFO is full but data FIFO is empty.
  - In this case, recl1 and recl2 suffered from the trouble at the same time.
    - Due to data size from FEEs or clock trouble from FTSW ??



length FIFO

data FIFO

Length FIFO : event size info. is stored.
Data FIFO : event data

- Data FIFO was read by user-logic when it should not be done (e.g. IDLE state) ?
  -> Actually yes.

EMPTY DATA-FIFO ERROR (3) : COUNTERMEASURE

Read enable was ON for ch0's data FIFO

However, ch0's data FIFO is empty.

- User-logic firmware tried to read data from data FIFO while it was empty.
- I don't know why this happens but currently firmware was updated not to start reading data FIFO when it is empty. (So far, when length FIFO is not empty, user-logic started reading data FIFO.)

COMMISSIONING FOR NEWLY UPDATED FIRMWARE AND SOFTWARE

- So far, commissiong was performed with PCIe40 firmware and software, which has been used in 2022ab run.
  - It is a baseline option for 2023/24 run.
- Recently, Dima-san and Yamagata-san developed new firmware and software for new event-building scheme (software-assisted event-building)
  - This long-term test also needs to be done before deploying in Physics run period.
- Also, IJClab experts are developing firmware with new features (double PCIexpress lanes, optical b2tt)
  - The test has just started. (TakShun-san's talk)

	Software assited event-building	*Dr Dmytro Levit*	
	Nara Women's University	15:25 - 15:45	
	Development at IJClab : Double PCIexpress and optical b2tt	*Tak-Shun Lau*	
16:00	*Nara Women's University*	15:45 - 16:05	
	Interface between FEE and PCIe40	*Dr Dmytro Levit*	
	Nara Women's University	16:05 - 16:20	

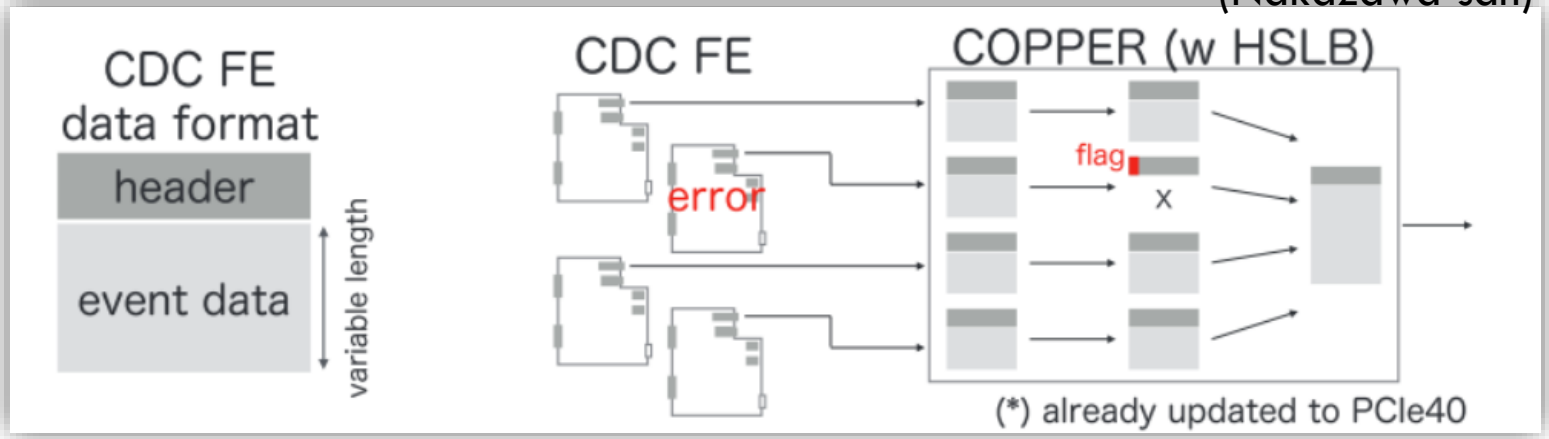
OTHER THINGS TO BE TESTED

TOP FE Migration to PCIe Motivation

(Shahab-san, Harsh-san)

- Currently Feature Extraction and Pedestal subtraction are performed in TOP SCROD PS.
- We have experienced constant PS lockups due to radiation and plan to minimize the usage of SCROD PS.
- There is not enough memory accessible on the carriers or SCROD PL to perform pedestal subtraction or planned future advanced feature extraction.
- Therefore, we plan to move FE and Pedestal Subtraction to PCIe40 system.

(Nakazawa-san)

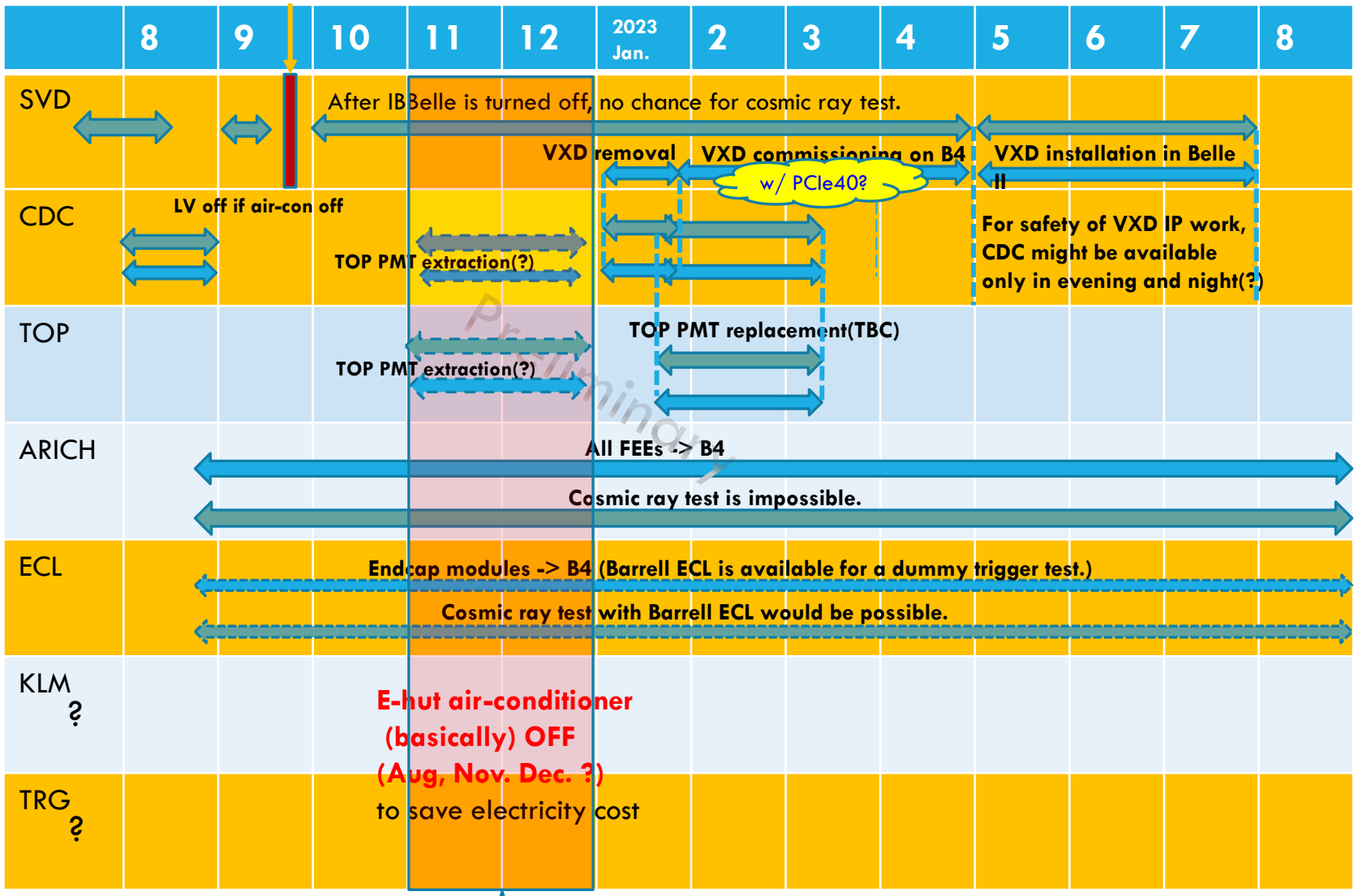


E-hut operation in LS1

Readout test with FEE (dummy trigger) cannot be done

Readout test with sensors(e.g. cosmic ray test) cannot be done

From a Gantt chart at SVD meeting on Mar. 1 :
https://indico.belle2.org/event/6307/contributions/32992/attachments/15590/23376/220222-VXD_installation_2022c_cancelled_v0.pdf



SUMMARY

- Commissioning for newly installed readout system for SVD, CDC, ECL and TRG is ongoing.
  - Readout test with high-occupancy/large event-size was started with available subsystems.
- We observed some issues in LS1 comissiong
  - fake-error events
  - Persistent BUSY
  - Empty FIFO
- We also need to perform a test for newly developed firmware and software.