Implementation of Soft-CDR for b2tt in PCIe40

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Motivation

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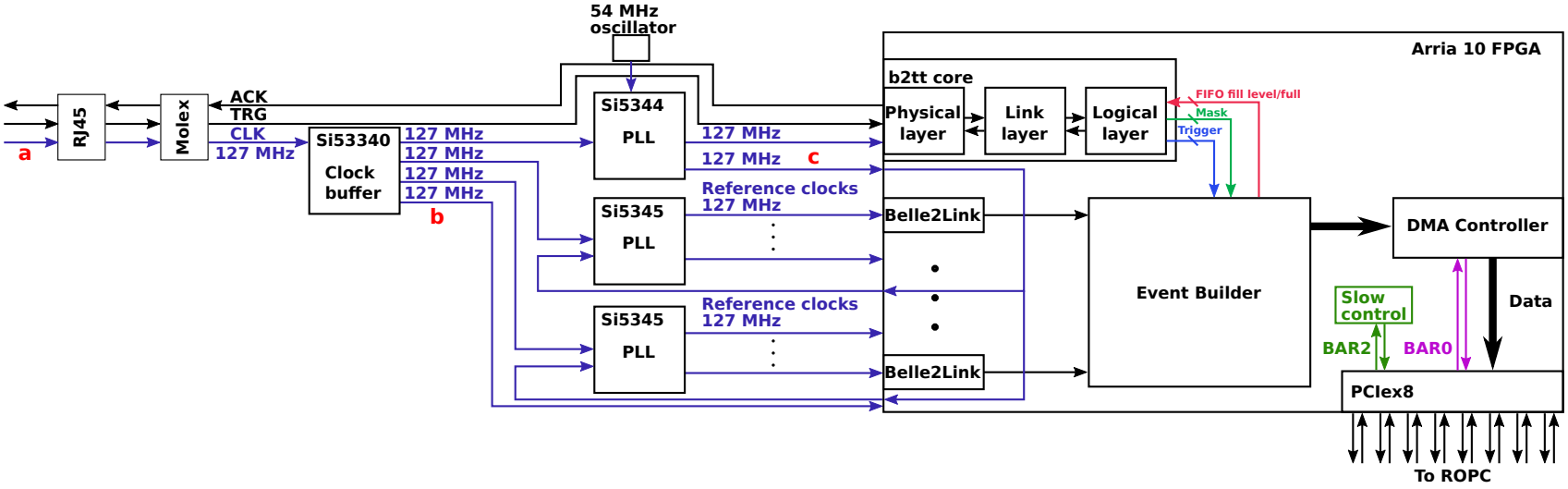
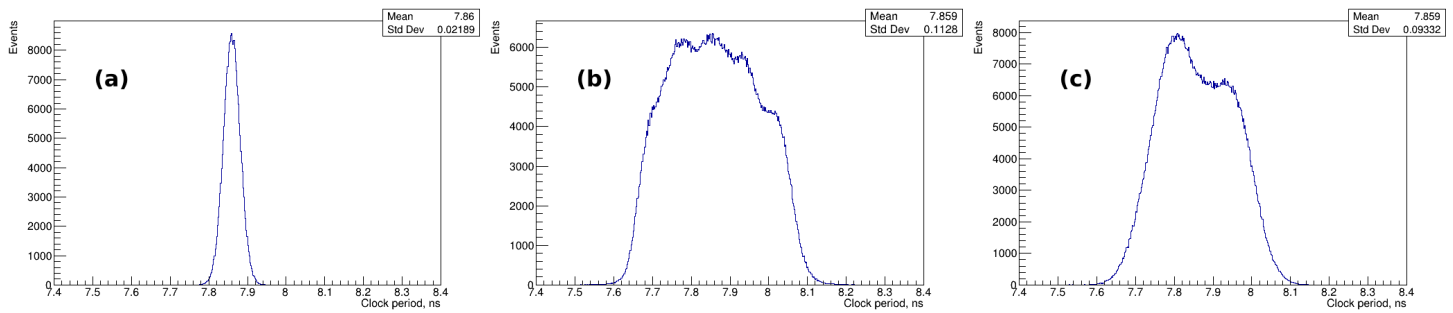
- 20 drops of the b2tt link in 2021c physics run
- Induced noise on CAT-7 cables
- Eliminate one source of noise by using new architecture

Clock Tree in PCIe40 and Jitter Measurements





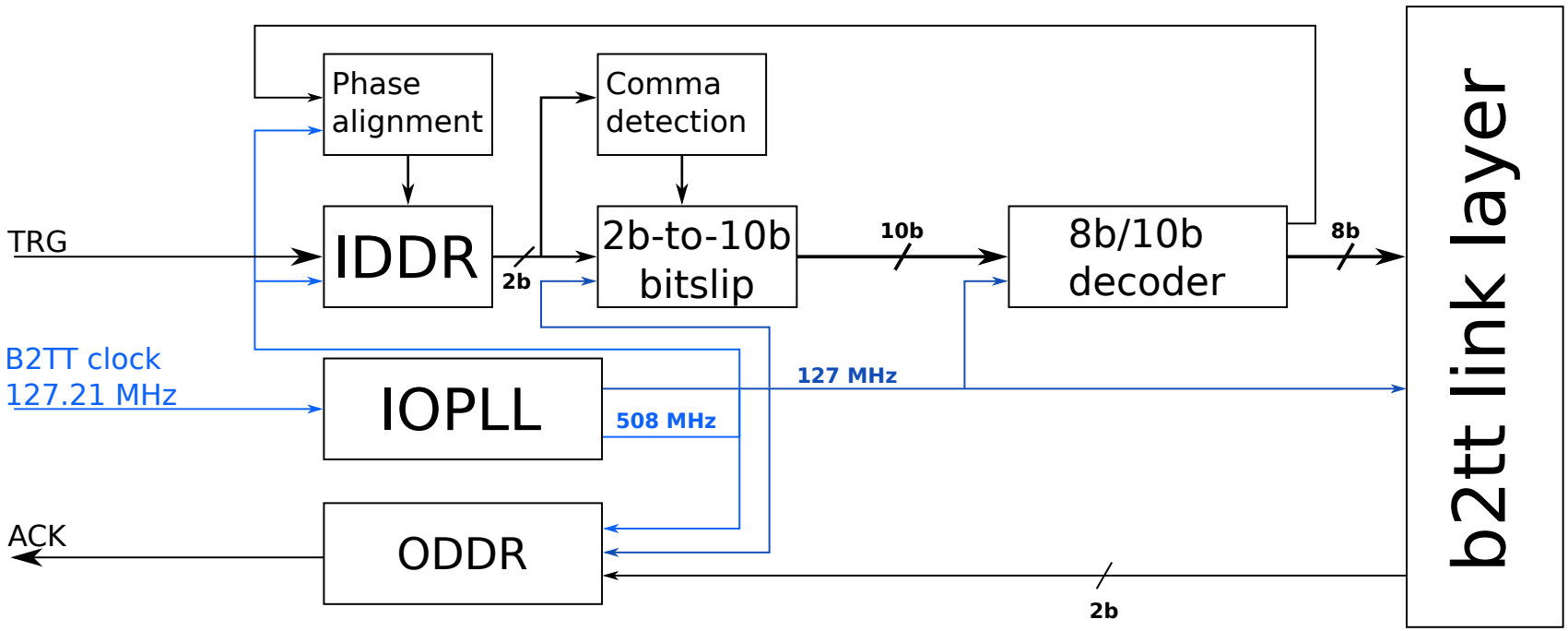
Clock Jitter Measurements

- Crosstalk visible in FTSW clock at PCIe40 input
- PLL cannot fully correct this jitter
  - jitter also affects Belle2Links
- Use on-board 54 MHz oscillatior to generate 127 MHz clock for b2tt
  - 127 MHz clock derived from accellerator clock

  $\Rightarrow$ frequency not constant
  - need clock-data recovery in FPGA to use independent clock source

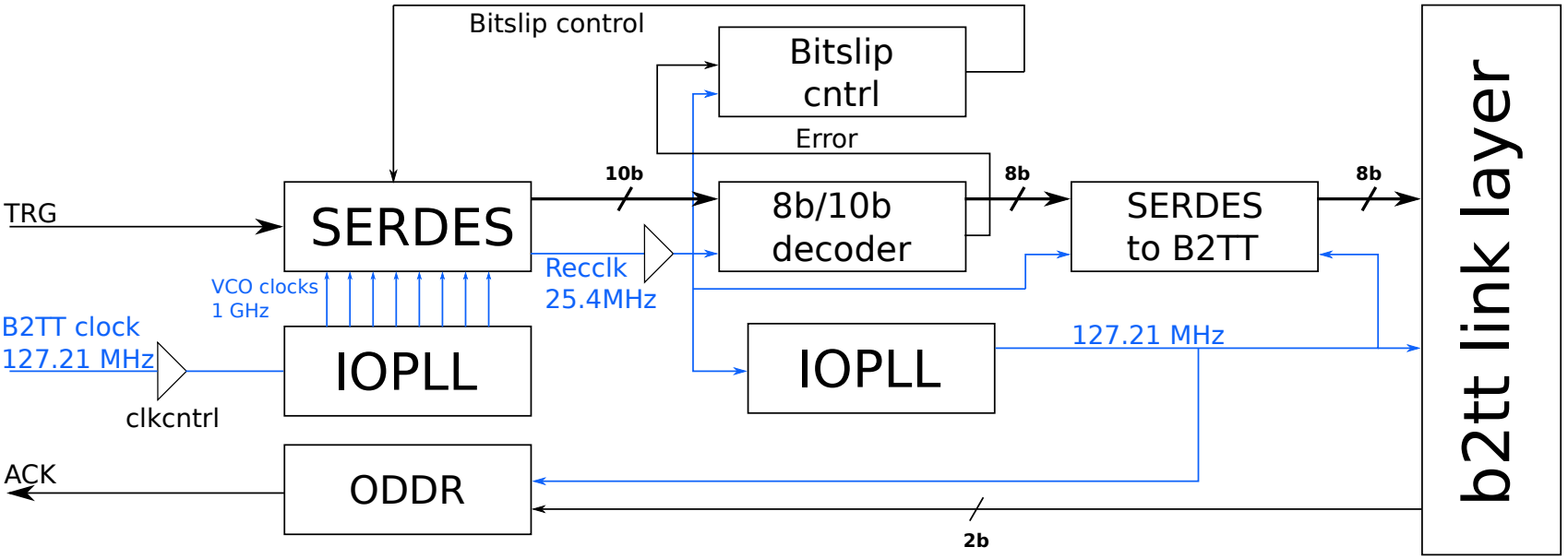
B2tt core

Original b2tt Core



- No phase tracking after lock
- Serialization and deserialization at 508 MHz
  - Occasional timing violations

Soft-CDR-based b2tt core



- Soft-CDR functionality of the Arria10 SERDES
- Continous phase tracking
- Serialization with ODDR component

Commissioning of the Soft-CDR-based b2tt Core

Clock Jitter

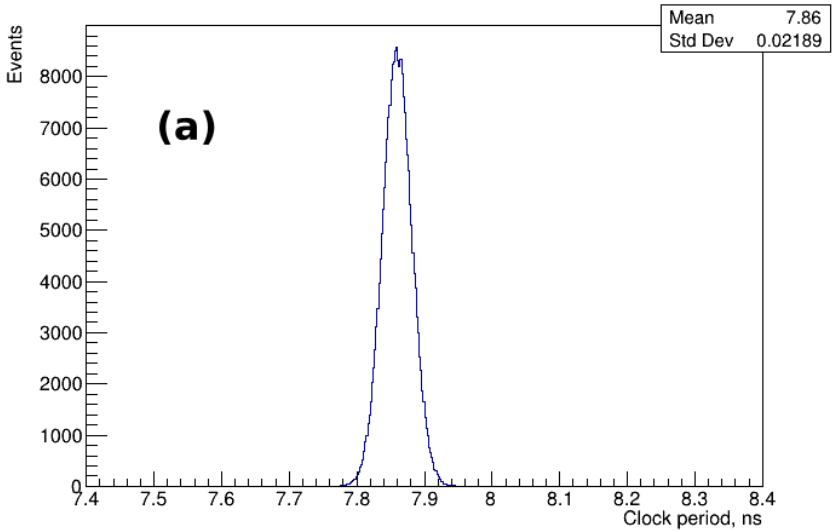


Figure: FTSW output clock

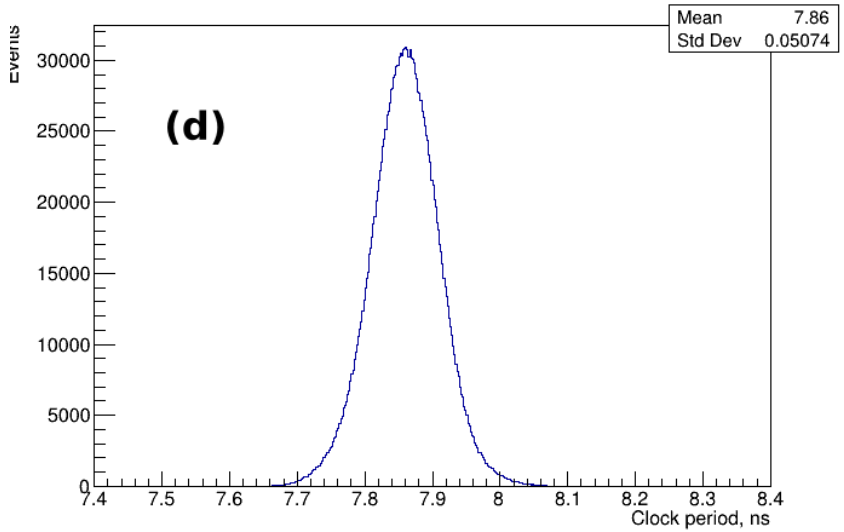
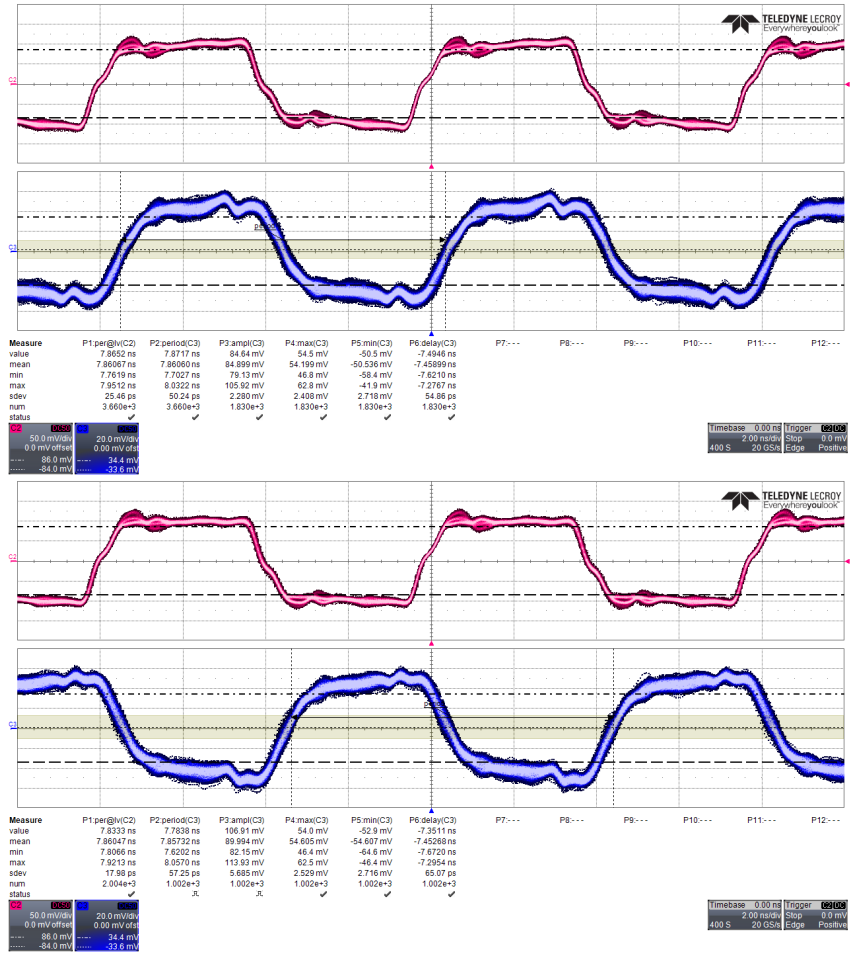


Figure: Recovered clock

- Jitter of the recovered clock 2x of the jitter of the FTSW clock
- Both clocks have Gaussian shape

Phase Ambiguity

- 180° phase ambiguity
- phase not important in the event builder



Trigger Latency

- Lower frequency of the parallel interface of the receiver
  - $\Rightarrow$ higher trigger latency
  - min. 2 clock cycles (173 ns)
- Not critical for the event builder application

Mask Setting Problem

- Channel mask could not be set reliably over b2tt
  - only in Belle II setup
- Problem not observed in B4 testbench nor at LAL

Mask Setting Problem

- Invalid 8b10b character sent after reset
- Triggers realignment by the bitslip controller FSM
- Link misses mask setting command
- Fixed by implementing debouncing logic in the FSM
  - ignore single-character errors
- Stable operation with debouncing logic
  - mask set reliably

System Operation with Soft-CDR-based b2tt Core

- PCIe40 used soft-CDR-based b2tt core since May 18th
- No link drops detected during physics run
  - 3 link drops related to work in eHut
  - does not solve the problem completely

Summary

- Soft-CDR-based b2tt core designed to use a free-running on-board oscillator
- System performance characterized
  - better shape of the jitter and smaller than in the original core
  - Belle2Links profits from reference clock with lower jitter
- System with new core used for 22 days during physics data taking
  - stable operation
  - **still susceptible to external noise**
- Transition to optical link should solve the noise problem