



Slow-control preparations for CDC & ECL

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Detector Initialization

(Detector slow control)

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- ▶ Before reading good sensible data, the sub-detector FEs need to be initialized or configured, also referred as detector slow control (SLC).
 - ▶ Setting thresholds, readout window sizes, taking pedestals, etc.
- ▶ SLC also includes detector monitoring – humidity, temperatures, voltages, etc.
- ▶ Happens through the readout board (*PCIe40*), which *interacts with the FEE over the same **B2L** (or optical link)*.
- ▶ **CDC & ECL**
 - ▶ Both subdetectors use **daq_slc** library for detector initialization, monitoring and archiving.

Need for changes in SLC libraries

Specifically for CDC & ECL

- ▶ COPPER board → connects to a max. of 4 frontends (through HSLBs)
- ▶ New PCIe40 board → connects to a max. of 48 frontends
- ▶ COPPER & HSLB library functions need to be replaced with those in PCIe40 software library
- ▶ New NSM nodes need to be incorporated in the existing NSM network
- ▶ Additionally, we want to keep support for the COPPER boards in **daq_slc**, at least for some time after the DAQ upgrade is complete
 - ▶ This helps to quickly switch back to COPPER boards in case an unknown issue/bug surfaces with the upgraded setup
 - ▶ Also, having everything in the same library allows us to distribute it to all ROPCs and other servers downstream, irrespective of the choice of readout board

Current state of SLC for CDC & ECL

- ▶ All necessary modifications in slow-control functions for CDC and ECL have already been made and thoroughly tested at KEK

	CDC	ECL
DAQ SLC	●	●
Config & DB files	●	●
NSM variables & EPICS PVs	●	●
CSS RC GUI	●	●
DAQ restart entries For ROPCs, HLTs, & STOREs	●	●
TTD entries Header files & DB tables (<i>ttdb</i> , <i>namedb</i> , <i>maskdb</i>)	●	●
DAQ Local run	●	●
Global run	●	●
High-rate tests	●	●
Long-term stability	●	●
Unpackers CDC, ECL, & ECLTRG	●	●
DQM plots for COSMICs	●	●

Hardware changes made in E-Hut

- 3 new ROPCs for ECL (**recl1**, **recl2**, **recl3**)
- 7 new ROPCs for CDC (**rcdc1**, **rcdc2**, ..., **rcdc7**)
- All members of **cdc/ecl** and **daq** groups can login to these machines from **bdaq**
- Other necessary equipment for DAQ upgrade has also been setup in E-hut
 - 1 PCIe40 board/ROPC
 - 25G ethernet cards
 - Patch panels near COPPER crates for easy connection to the PCIe40 boards
 - Necessary optical fibers

Software changes

- ▶ PCIe40 firmware and software aims at keeping most software functionalities of COPPER boards intact.
- ▶ To avoid confusion though, the low-level COPPER commands like, **reghs**, **readhs**, **statbs**, etc. have been renamed for PCIe40. Any script using these commands need to be updated for it to work with PCIe40.
- ▶ The following software repository have been changed:
 - ▶ **daq_slc**
 - ▶ **daq_restart**
 - ▶ **daq_rc_gui**
 - ▶ **DAQ software** (part of basf2)
 - ▶ Unpacker module (part of basf2), offline standalone unpacker (if exists!)
 - ▶ Any other monitoring/initialization/configuration codes/scripts based on these...

New SLC Commands

PCIe40 equivalents

- ▶ The basic register read/write function now has a different syntax:

reghs -[a...d] fee32 [addr] [value] → pcie40_regconfig --ch [0...47] --fee32 -r/w [addr] [value]

- ▶ Note: **pcie40_regconfig** can also be used to read/write registers on PCIe40.
- ▶ **pcie40_regconfig** does not support N-times read/write, like **reghsx** did, but you can loop.
- ▶ A sequence of addr, value pairs with a single call to **pcie40_regconfig** is also not supported but again you can loop.
- ▶ **pcie40_regconfig** also doesn't support writing registers to multiple channels (or FEEs) at the same time in a single call (work in progress).

- ▶ Other equivalent commands:

staths -[a...d] → pcie40_statlink --ch [0...47] --fee

readhs -[#events] -[a...d] [file] → pcie40_dmalhighrate --mode <MODE> --file <FILENAME> --nEvents <#EVTS>

- ▶ **MODE (required)** can either be **0**, **1**, **2**, or **3**:
0 for data, or **1** for internal generator, or **2** for writing all data to a file, or **3** for writing only FEE data to file.
- ▶ No equivalent of **tesths** exists for PCIe40. B2Links are established automatically.

Examples of FE register access

reghs

```
[purwar@b3ropc02 Scripts]$ pcie40_regconfig --ch 1 --fee32 -r 0x15  
reg0015 = 00000e74
```

```
[purwar@b3ropc02 Scripts]$ pcie40_regconfig --ch 1 --fee32 -w 0x15 0xe10 (always in hex)  
Write 0x00000e10 to register 0x0015
```

```
[purwar@b3ropc02 Scripts]$ pcie40_regconfig --ch 1 --fee32 -r 0x15  
reg0015 = 00000e10
```

staths

```
[purwar@b3ropc02 Scripts]$ pcie40_statlink --ch 1 --fee  
statlink version 3 (20210107) / PCIE40 firmware version 15.2  
memory: OK | ttd: UP | ttd clk: UP | run=: 245 | trg: 0 | trg type: 15  
PLLs:LOCKED | B2L:READY (rx:111 tx:11) | DMA:FREE ( 253693.4kB)  
CDC serial 129 version 67  
(01) b2l=UP (gbt=UP rx=UP tx=UP rxsta=READY txsta=READY mask=UNMASK)  
(01) event=280603112 total=-1660774.9kB (avg=-5.9186B last=38 max=194 B)  
(01) full=0 feecrcerr=242 check=NG rxcrcerr=4319, check=0  
(01) no b2link error
```

Changes in CDC naming conventions

Affects **only** CDC

- Changes have been made in naming conventions for NSM variables, database entries, EPICS PVs (or aliases) in ***daq_slc***.
- Idea is to get rid of COPPER and HSLB references from the names to avoid PCIe40 to COPPER mapping everywhere.

Reference	Current setup (COPPER/HSLB)	Upgraded setup (with PCIe40)
DB entries	cdc:fee:CPR20XX:y:suppress:	cdc:I:fee:PCIE40LINKJJ:suppress:
NSM variables	CPR20XX@cdc[j]:tem	PCIE40LINKJJ@cdc[i]:tem
EPICS PVs	CDC:CPR20XX:FEE:Y:Tem:F	CDC:I:FEE:JJ:Tem:F
	XX: {00..75} Y: {A..D}, y: {a..d} j: {0..3}	I: {1..7} JJ: {0..43} i: {0..299}

Mapping from CDC COPPERs to PCIe40s

Current System

COPPER IDs	# B2Links
2001-2009	36
2010-2017	32
2018-2025	32
2026-2034	36
2035-2042	32
2043-2050	32
2051-2059	35
2060-2067	32
2068-2075	32
75 CPRs	299

New System

ROPC	PCIe40LINK Nodes	# B2Links	COPPER/HSLB
rcdc1	0-42	43	2001a - 2011c
rcdc2	0-42	43	2011d - 2022b
rcdc3	0-42	43	2022c - 2033a
rcdc4	0-42	43	2033b - 2043d
rcdc5	0-42	43	2044a - 2054c
rcdc6	0-42 (5)	42	2054d - 2065b
rcdc7	0-41	42	2065c - 2075d
TOTAL	7 PCIe40s/ROPCs	299	

Mapping from ECL COPPERs to PCIe40s

Current System

COPPER IDs	# B2Links
5001-5009	18
5010-5018	18
6001-6008, cpr13001	17
27 CPRs	53

New System

ROPC	PCIE40LINK Nodes	# B2Links	COPPER/HSLB
recl1	0-17	18	5001a – 5009b
recl2	0-17	18	5010a - 5018b
recl3	0-16	17	6001a – 6008b, cpr13001
TOTAL	3 PCIe40s/ROPCs	53	

daq_restart

- ▶ Necessary modifications in **daq_restart (restart.sh script)** have already been made for:
 - ▶ 7 new CDC ROPCs: (**rcdc → rcdc1, rcdc2, ..., rcdc7**) and,
 - ▶ 3 new ECL ROPCs: (**recl → recl1, recl2, recl3**)

restart.sh rcdc start/stop

restart.sh recl start/stop

- ▶ Necessary modifications for assigned HLT worker nodes and store server for local runs have also been made.

New CDC RC GUI

Console RCControlMain.opi RC SVD RC CDC

100% 100%

RC_CDC

Run # : 10 CDC@RC:cosmic:2...

READY	STORE_RCDC	READY
START	RC_HLT_RCDC	READY
ABORT	CDC	READY
BOOI	TTD_CDC	READY

FTSW #200 ERROR resettt stattt

Trigger type aux Run start at 2022-06-25 04:36:55

Trigger limit -1 Run time 28[sec]

Dummy rate -1 [Hz] Trigger in 1000.6 [Hz]

Max time 13000: [us] Trigger out 0.0 [Hz]

Max trig 10 Input count 28093

Output count 0

STORE_RCDC READY

Run type cdc eb2rx input

Event rate [kHz] 0

Event size [kB] 0

Event counter 0

Flow rate [MB/s] 0

File size [MB] 0

of files 0

CDC

Run # : 10

READY	RCDC1	READY
START	RCDC2	READY
ABORT	RCDC3	READY
BOOI	RCDC4	READY
	RCDC5	READY
	RCDC6	READY
	RCDC7	READY

RC_HLT_RCDC Run # : 0

READY	HLTIN_RCDC	READY
START	HLTOUT_RCDC	READY
ABORT	EB1_RCDC	READY
BOOI	HTWK13_RCDC	READY
	HTWK14_RCDC	READY
	DQM_RCDC	READY

rcdc1 rcdc2 rcdc3 rcdc4 rcdc5 rcdc6 rcdc7

Hostname rcdc1 TTD DMA DMA [kBytes] Size [Bytes] Rate [MB/s]

Belle2link-channel

		READY	NOTREADY	TDD	DMA	DMA [kBytes]	Size [Bytes]	Rate [MB/s]	Program PCIe40
020 - 00	✓	✗	✗	0	0	276 - 02	✓	0.00	0
047 - 04	✓	✗	✗	0	0	231 - 06	✓	0.00	0
046 - 08	✓	✗	✗	0	0	230 - 10	✓	0.00	0
027 - 12	✓	✗	✗	0	0	189 - 14	✓	0.00	0
026 - 16	✓	✗	✗	0	0	188 - 18	✓	0.00	0
007 - 20	✓	✗	✗	0	0	161 - 22	✓	0.00	0
006 - 24	✓	✗	✗	0	0	160 - 26	✓	0.00	0
039 - 28	✓	✗	✗	0	0	159 - 30	✓	0.00	0
038 - 32	✓	✗	✗	0	0	158 - 34	✓	0.00	0
019 - 36	✓	✗	✗	0	0	157 - 38	✓	0.00	0
018 - 40	✓	✗	✗	0	0	156 - 42	✓	0.00	0

Some tips (Updated on Feb. 18, 2022)

- * How to program PCIe40 firmware
- Push "Program PCIe40" and wait until the progress-bar reaches "█"
- Mask was set as before program PCIe40, refresh OPI to confirm.

* Mask/unmask channels

- Update channel checkboxes and push "Save & apply Mask".

* Load and apply the last saved mask setting

- Push "Load & Apply Mask" and then checkboxes should be updated

- Refresh OPI to confirm the update.

Load & Apply Mask

Save & Apply Mask

Info in the new RC GUIs

ROPC RC State

Hostname	TTD	DMA	DMA [kBytes]	Size [Bytes]	Rate [MB/s]	Program PCIe40
rcdc1	READY	READY	0	0	0.00	0
rcdc2	NOTREADY	READY	0	0	0.00	0
rcdc3	READY	READY	0	0	0.00	0
rcdc4	READY	READY	0	0	0.00	0
rcdc5	READY	READY	0	0	0.00	0
rcdc6	READY	READY	0	0	0.00	0
rcdc7	READY	READY	0	0	0.00	0

Belle2link-channel

020 - 00	READY	READY	0	120 - 01	READY	READY	0	276 - 02	READY	READY	0	200 - 03	READY	READY	0
047 - 04	READY	READY	0	091 - 05	READY	READY	0	231 - 06	READY	READY	0	291 - 07	READY	READY	0
046 - 08	READY	READY	0	090 - 09	READY	READY	0	230 - 10	READY	READY	0	290 - 11	READY	READY	0
027 - 12	READY	READY	0	153 - 13	READY	READY	0	189 - 14	READY	READY	0	243 - 15	READY	READY	0
026 - 16	READY	READY	0	152 - 17	READY	READY	0	188 - 18	READY	READY	0	242 - 19	READY	READY	0
007 - 20	READY	READY	0	119 - 21	READY	READY	0	161 - 22	READY	READY	0	199 - 23	READY	READY	0
006 - 24	READY	READY	0	118 - 25	READY	READY	0	160 - 26	READY	READY	0	198 - 27	READY	READY	0
039 - 28	READY	READY	0	089 - 29	READY	READY	0	159 - 30	READY	READY	0	289 - 31	READY	READY	0
038 - 32	READY	READY	0	088 - 33	READY	READY	0	158 - 34	READY	READY	0	288 - 35	READY	READY	0
019 - 36	READY	READY	0	151 - 37	READY	READY	0	157 - 38	READY	READY	0	287 - 39	READY	READY	0
018 - 40	READY	READY	0	150 - 41	READY	READY	0	156 - 42	READY	READY	0				

Controls and Status Indicators (Left Side)

- (un)Mask channel B2L Mask
- B2L Status
- FIFO Status
- #Events

System Status (Top Left)

- RC_CDC: READY
- Run #: 10
- CDC@RC:cosmic:2...
- STORE_RCDC: READY
- RC_HLT_RCDC: CDC
- TTD_CDC: READY

System Status (Top Right)

- Run #: 10
- RC CDC: READY
- RCDC1: READY

System Status (Bottom Left)

- FTSW #200: ERROR
- Trigger type: Run start
- Trigger link: Run time
- Dummy rate: Trigger in
- Max time: Trigger out
- Max trig: Input count
- Max trig: Output count
- STORE_RCDC: READY
- Run type: cdc
- Event rate [kHz]: 0
- Event size [kB]: 0
- Event counter: 0
- Flow rate [MB/s]: 0
- File size [MB]: 0
- # of files: 0

System Status (Bottom Right)

- Program PCIe40: 0

New ECL RC GUI

The figure shows a screenshot of the RC ECL control interface, titled "RC ECL & RCControlMain.opi". The interface is divided into several sections:

- Top Left:** A window for the "RC_ECL" module. It displays the run number (Run # : 1692) and various status indicators for components like STORE_RECL, RC_HLT_RECL, ECL, and TTD_ECL, all of which are currently "RUNNING". It also shows trigger parameters: Trigger type (poisson), Trigger limit (-1), Dummy rate (1000 [Hz]), Max time (35143; [us]), and Max trig (12). Run start at 2022-04-05 12:44:40.
- Top Middle:** A window for the "ECL" module, showing similar status for RECL1, RECL2, and RECL3 components.
- Bottom Left:** A window for the "RC_HLT_RECL" module, listing components like HLTIN_RECL, HLTOUP_RECL, EB1_RECL, HLTWK14_16_RECL, HLTWK12_13_RECL, and DQM_RECL, all in "RUNNING" state.
- Central Panel:** A large area containing two buttons: "Load & Apply Mask" and "Save & Apply Mask". Below these buttons is a section with some tips for applying a mask, including instructions on how to program PCIe40 firmware, push checkboxes, and refresh OPI.
- Right Side:** A detailed monitoring section for Belle2link-channel. It lists hostnames (rec1, rec2, rec3) and their corresponding TTD, DMA, DMA [kBytes], Size [Bytes], and Rate [MB/s] metrics. Each entry includes a "Program PCIe40" button. The table is organized into three main sections: "Belle2link-channel" for each hostname, and "B19 - 00" through "ETM - 16" for specific channel details.

Thank you for your time and attention.

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