Development at IJClab: Double PClexpress and optical b2tt

LAU Tak-5hun On behalf of IJClab 30^{+h} November 2022





People in IJClab and their responsibilities

- Responsible scientific: Patrick Robbe
- Responsible technique: Daniel Charlet
- Software developments (drivers, low level libraries):
 Monique Taurigna, Eric Jules
- Firmware developments (interface): Eric Plaige
- Tests and high level software: Tak-Shun Lau

Collaboration with KEK, Hawaii University, Nagoya University

Developments on PCIe40

- Move to quartus 21.3 from 18.1
- Double PCI (The one that I'm working on.)
 - 1. For the moment, uses 1 PCI x8 lane: 50 Gb/s limit.
 - 2. 2 PCI x8 lanes are available in the PCIe40 board: 100 Gb/s transfer is possible.
 - 3. New firmware (git branch doublepci) under test where both PCI lanes are available.
- Optical b2tt (Start working on.)
 - 1. PCle40 has two free SFP optical connections:

 One link for 'data' transmission in the two directions, one link for 'clock'.
 - 2. development ongoing

```
6     - <ipxact:version>18.1
19 + <ipxact:version>21.3

//pxact:version>
```

```
117
     124
                pcie_0_status_rst_n
                                            => pcie_0_status_rst_n,
                                                                        -- SOrtie di PCTe
      125 +
                pcie 1 status rst n
                                            => pcie 1 status rst n,
                                                                        -- SOrtie di PCIe
118 126
119
     127
                pcie 0 perst
                                                    pcie 0 perst,
120
     128
                pcie_0_npor
                                                    pcie 0 perst.
    129
                pcie 0 refclk
                                                    pcie_0_refclk,
     130
      131 +
                pcie_1_perst
                                                    pcie_1_perst,
      132 +
                pcie_1_npor
                                                    pcie_1_perst,
                pcie 1 refclk
      133 +
                                                    pcie 1 refclk,
      134 +
      135 +
123
     136
                pcie_0_reconfig_clk
                                            => pcie_0_reconfig_clk, --Not required in A10
124 137
                pcie 0 reconfig clk locked => pcie 0 reconfig clk locked,
125
                pcie 0 reconfig rst n
                                            => pcie 0 reconfig rst n,
126
127 140
                pcie_0_hip_serial_rx(7 downto 0)
                                                            pcie_0_hip_serial_rx,
      141 +
                    pcie 1 hip serial rx(7 downto 0)
                                                                pcie 1 hip serial rx,
128
     142
129
     143
                                                            pcie_0_hip_serial_tx,
                pcie_0_hip_serial_tx(7 downto 0)
                pcie_1_hip_serial_tx(7 downto 0)
                                                            pcie_1_hip_serial_tx,
```

```
153 + A10_SFP1_TFC_TX : OUT STD_LOGIC;
154 + A10_SFP1_TFC_RX : IN STD_LOGIC;
```

https://indico.belle2.org/event/6872/contributions/37049/attachments/16869/25132/BelleII DAQUpgrade 30May 2022.pdf

PCIe400 (not typo)

- New development started in France for a new version of the board
 - => PCle400
- Aim at having a board in 2026 with 4x more bandwidth:
 - 40 bi-directional links at 56 Gb/s
 - 32 Gb internal memory
 - 400 Gb Ethernet interface
 - PCI express Gen 4
- This is an intermediate step for a board with 800 GbE interface for 2032.

https://indico.belle2.org/event/6872/contributions/37049/attachments/16869/25132/BelleII DAQUpgrade 30May 2022.pdf

Current status on "doublepci"

• There is a stable "doublepci" firmware.

quartus21	master	48 links	v15.4 (sof.LAL, sof.KEK, pof.KEK)	New DMA, user logic and b2tt. Soft CDR for b2tt, fixes for PCIe stability. To be used for development.	v9.5	exp26 run33 (top, arich, klm); deployed during the maintenance day of May 11, 2022 exp26 run250(arich,klm), exp26 run254(top): bellell_KEK_v15.4_36ch.sof
doublepci	master	48 links	v17.0 (sof.LAL, sof.KEK, pof.KEK)	First version with double pci interface. To be used for tests only.	v9.5	

- The firmware has already passed few tests, including slow control test and data readout test, in the IJC lab.
- It is now being tested with the KEK b2ropc.

Test in IJClab

 Setup on BIOS menu to avoid bugs: Advanced >>Chipset Configuration>>North Bridge>>IIO Configuration>>II01 Configuration. 8x8 configuration is needed to choose.

Slow Control Test.

```
[belle2daq@pc1-belle2 Scripts]$ python2 testSLC.py --channel 9 --detector CDC 1000
0
Total number of errors = 0
[belle2daq@pc1-belle2 Scripts]$ ■
```

Data Reading Test.

```
event_no = 0000125c / local_event_count = 4700
         event_no = 000012c0 / local_event_count = 4800
        event_no = 00001324 / local_event_count = 4900
 DEBUG] event_no = 00001388 / local_event_count = 5000
DEBUG] event_no = 000013ec / local_event_count = 5100
 DEBUG] event_no = 00001450 / local_event_count = 5200
         event_no = 000014b4 / local_event_count = 5300
        event_no = 00001518 / local_event_count = 5400
 DEBUG] event_no = 0000157c / local_event_count = 5500
DEBUG] event no = 000015e0 / local event count = 5600
        event_no = 00001644 / local_event_count = 5700
        event_no = 000016a8 / local_event_count = 5800
        ] event_no = 0000170c / local_event_count = 5900
] event_no = 00001770 / local_event_count = 6000
 DEBUG] event_no = 000017d4 / local_event_count = 6100
         event_no = 00001838 / local_event_count = 6200
 DEBUG] event_no = 0000189c / local_event_count = 6300
  DEBUG] event no = 00001900 / local event count = 6400
 DEBUG] event_no = 00001964 / local_event_count = 6500
 DEBUG] event no = 000019c8 / local event count = 6600
 DEBUG] event_no = 00001a2c / local_event_count = 6700
DEBUG event no = 00001a90 / local event count = 6900
DEBUG event no = 00001a90 / local event count = 6900
DEBUG event no = 00001b58 / local event count = 7000
DEBUG event no = 00001b58 / local event count = 7000
DEBUG event no = 00001b5 / local event count = 7100
        ] event_no = 00001ce8 / local_event_count = 7400
  DEBUG] event no = 00001d4c / local event count = 7500
 DEBUG] event no = 00001db0 / local event count = 7600
 DEBUG1 event no = 00001e14 / local event count = 7700
 DEBUG1 event no = 00001e78 / local_event_count = 7800
 DEBUG] event_no = 0000ledc / local_event_count = 7900
DEBUG] event_no = 00001f40 / local_event_count = 8000
        | event_no = 00001fa4 / local_event_count = 8100
| event_no = 00002008 / local_event_count = 8200
        event_no = 0000206c / local_event_count = 8300
         event_no = 000020d0 / local_event_count = 8400
        event_no = 00002134 / local_event_count = 8500
        event_no = 00002198 / local_event_count = 8600
 DEBUG] event no = 000021fc / local event count = 8700
        event_no = 00002260 / local_event_count = 8800
        event no = 000022c4 / local event count = 8900
 DEBUG] event_no = 00002328 / local_event_count = 9000
DEBUG] event_no = 0000238c / local_event_count = 9100
        ] event_no = 000023f0 / local_event_count = 9200
] event_no = 00002454 / local_event_count = 9300
         event_no = 000024b8 / local_event_count = 9400
 DEBUG] event_no = 0000251c / local_event_count = 9500
DEBUG] event_no = 00002580 / local_event_count = 9600
        event_no = 000025e4 / local_event_count = 9700
 DEBUG1 event no = 00002648 / local event count = 9800
| DEBUG | event_no = 000020ab / local_event_count = 9900 | |
| DEBUG | event_no = 00002710 / local_event_count = 10000 | |
| DEBUG | event_no = 00004e20 / local_event_count = 20000 | |
```

Test in KEK

- The coming test is the speed test, to see whether the firmware can be push to the limit 100 Gb/s.
- The trigger rate has been tried to push to 4000000 Hz, but it was still too far from the limit, only 281.74 Mb/s.
- Our plan is to try to increase the size of the test-event.

 Instead of using the test-event in the "copper", the event directly generated by PCIe40 seems more useful.
- Using the event generated by PCIe40 itself can also ensure the transfer rate limit is not from the other components.
- To use the data generated by PCIe40, the disabled generator would need to be enabled again.

 The firmware is kept modifying and testing.

```
//pcie40_enableGenerator(0);
//pcie40_useDataFromGenerator(0);
pcie40_disableGenerator(0);
pcie40_useDataFromFibers(0);
```

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```
data_flow_controller_data <= scientific_data when pio_cmd13(9) = '1' else data_out_test;
data_flow_controller_wren <= wr_scientific_data when pio_cmd13(9) = '1' else wr_en_test;
data_flow_controller_data <= scientific_data; -- when pio_cmd13(9) = '1' else data_out_test;
data_flow_controller_wren <= wr_scientific_data; -- when pio_cmd13(9) = '1' else wr_en_test;
```

Plan on Optical b2tt

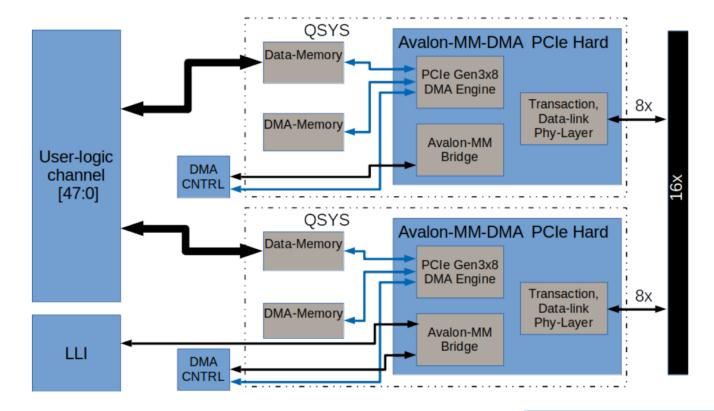
- Use fibers for PCle40-FTSW connection instead of LAN cable
- The FTSW upgrade is also necessary.
- I'm joining for modifying and testing the firmware.

Conclusion

- The firmware is kept updating and testing.
- The "doublepci" shows no error for data reading test and slow control test, but not yet the rate test.
- The optical b2tt firmware is under developing.
- A new board is under developing.

Appendix: The Double DMA interface

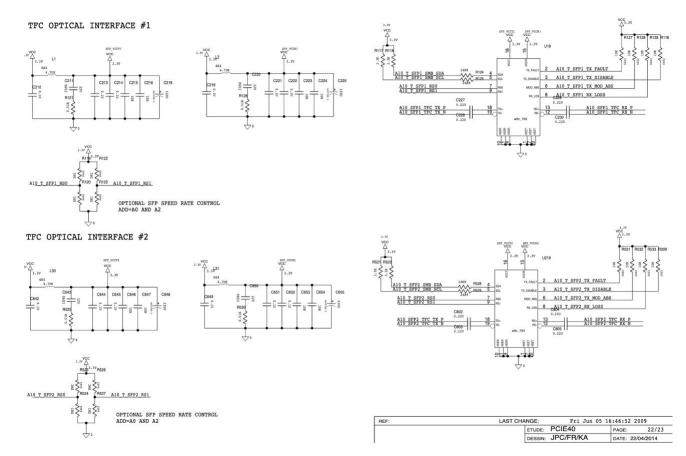
Increase data rate from PCIe40 to PC server by using the 2 DMA interfaces available (instead of 1 now)



https://indico.belle2.org/event/5891/contributions/31346/attachments/14699/22105/Belle2 DAQB2GM 17Jan2022.pdf

Appendix: B2TT via optical links

- Try to use b2tt directly with optical links into the PCIe40 board.
- Two optical SFP interfaces available on the PCle40 board and not used at the moment.



https://indico.belle2.org/event/5891/contributions/31346/attachments/14699/22105/Belle2 DAQB2GM 17Jan2022.pdf