Development at IJClab : Double PCIexpress and optical b2tt

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On behalf of IJClab
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People in IJClab and their responsibilities

- Responsible scientific: Patrick Robbe
- Responsible technique: Daniel Charlet
- Software developments (drivers, low level libraries): Monique Taurigna, Eric Jules
- Firmware developments (interface): Eric Plaige
- Tests and high level software: Tak-Shun Lau

Collaboration with KEK, Hawaii University, Nagoya University

Developments on PCIe40

- Move to quartus 21.3 from 18.1

```
6   -   <ipxact:version>18.1</ipxact:version>
19  +   <ipxact:version>21.3</ipxact:version>
```

- Double PCI (The one that I'm working on.)

  1. For the moment, uses 1 PCI x8 lane : 50 Gb/s limit.
  2. 2 PCI x8 lanes are available in the PCIe40 board: 100 Gb/s transfer is possible.
  3. New firmware (git branch doublepci) under test where both PCI lanes are available.

```
117 124     pcie_0_status_rst_n         =>  pcie_0_status_rst_n,    -- SOrtie di PCIe
    125 +   pcie_1_status_rst_n         =>  pcie_1_status_rst_n,    -- SOrtie di PCIe
118 126
119 127     pcie_0_perst                =>      pcie_0_perst,
120 128     pcie_0_npor                 =>      pcie_0_perst,
121 129     pcie_0_refclk               =>      pcie_0_refclk,
122 130
    131 +   pcie_1_perst                =>      pcie_1_perst,
    132 +   pcie_1_npor                 =>      pcie_1_perst,
    133 +   pcie_1_refclk               =>      pcie_1_refclk,
    134 +
    135 +
123 136     pcie_0_reconfig_clk         =>  pcie_0_reconfig_clk, --Not required in A10
124 137     pcie_0_reconfig_clk_locked =>   pcie_0_reconfig_clk_locked,
125 138     pcie_0_reconfig_rst_n       =>  pcie_0_reconfig_rst_n,
126 139
127 140     pcie_0_hip_serial_rx(7 downto 0)    =>      pcie_0_hip_serial_rx,
    141 +       pcie_1_hip_serial_rx(7 downto 0)    =>      pcie_1_hip_serial_rx,
128 142
129 143     pcie_0_hip_serial_tx(7 downto 0)    =>      pcie_0_hip_serial_tx,
    144 +   pcie_1_hip_serial_tx(7 downto 0)    =>      pcie_1_hip_serial_tx,
```

- Optical b2tt (Start working on.)

  1. PCIe40 has two free SFP optical connections:
     One link for 'data' transmission in the two directions, one link for 'clock'.
  2. development ongoing

```
153 +   A10_SFP1_TFC_TX              : OUT       STD_LOGIC;
154 +   A10_SFP1_TFC_RX              : IN        STD_LOGIC;
```

https://indico.belle2.org/event/6872/contributions/37049/attachments/16869/25132/BelleII_DAQUpgrade_30May2022.pdf

PCIe400 (not typo)

- New development started in France for a new version of the board

  => PCIe400

- Aim at having a board in 2026 with 4x more bandwidth:

  40 bi-directional links at 56 Gb/s

  32 Gb internal memory

  400 Gb Ethernet interface

  PCI express Gen 4

- This is an intermediate step for a board with 800 GbE interface for 2032.

https://indico.belle2.org/event/6872/contributions/37049/attachments/16869/25132/BelleII_DAQUpgrade_30May2022.pdf

Current status on “doublepci”

- There is a stable “doublepci” firmware.

quartus21	master	48 links	v15.4 (sof.LAL, sof.KEK, pof.KEK)	New DMA, user logic and b2tt. Soft CDR for b2tt, fixes for PCIe stability. **To be used for development.**	v9.5		exp26 run33 (top, arich, klm); deployed during the maintenance day of May 11, 2022 exp26 run250(arich,klm), exp26 run254(top): belleII_KEK_v15.4_36ch.sof
doublepci	master	48 links	v17.0 (sof.LAL, sof.KEK, pof.KEK)	First version with double pci interface. **To be used for tests only.**	v9.5		

- The firmware has already passed few tests, including slow control test and data readout test, in the IJC lab.

- It is now being tested with the KEK b2ropc.

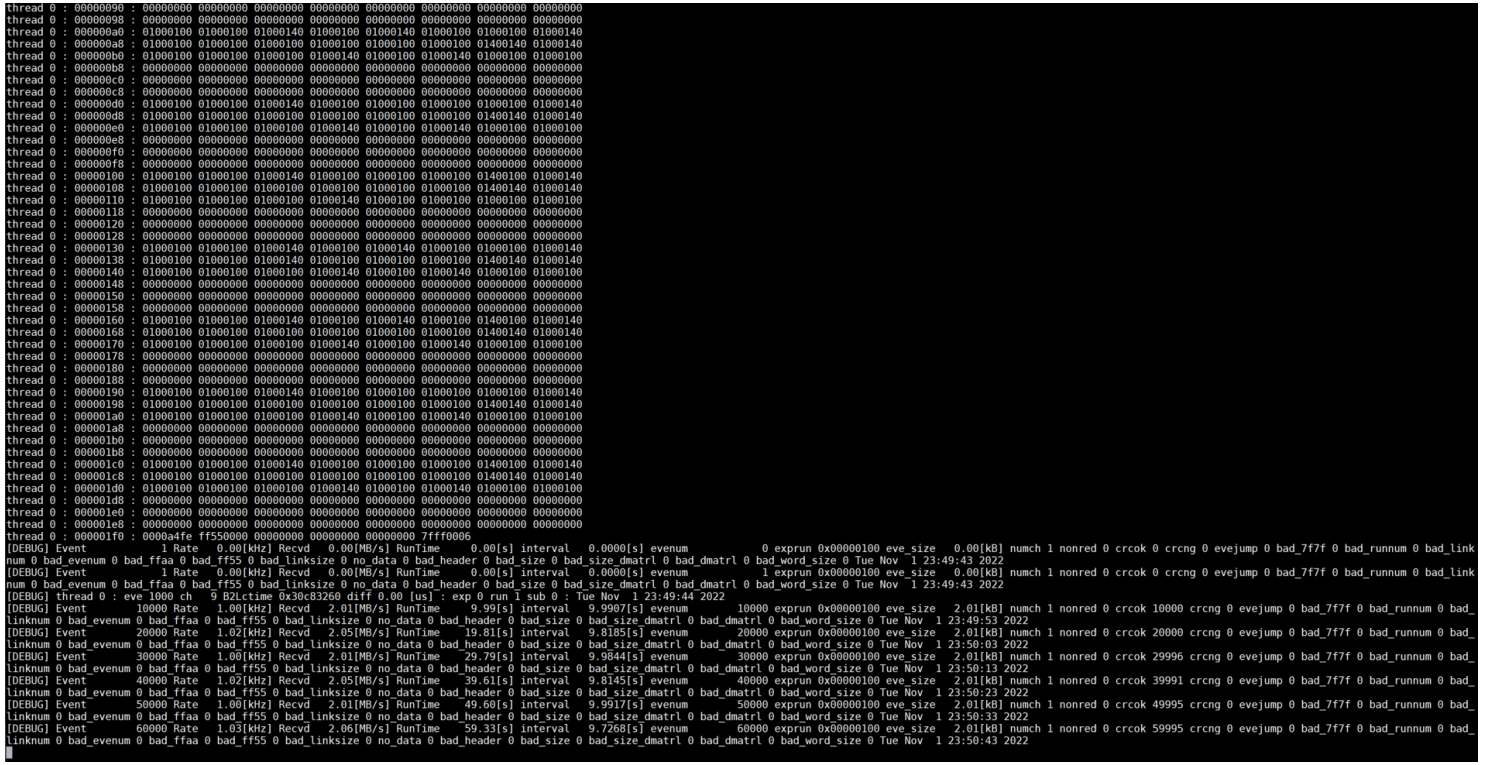
Test in IJClab

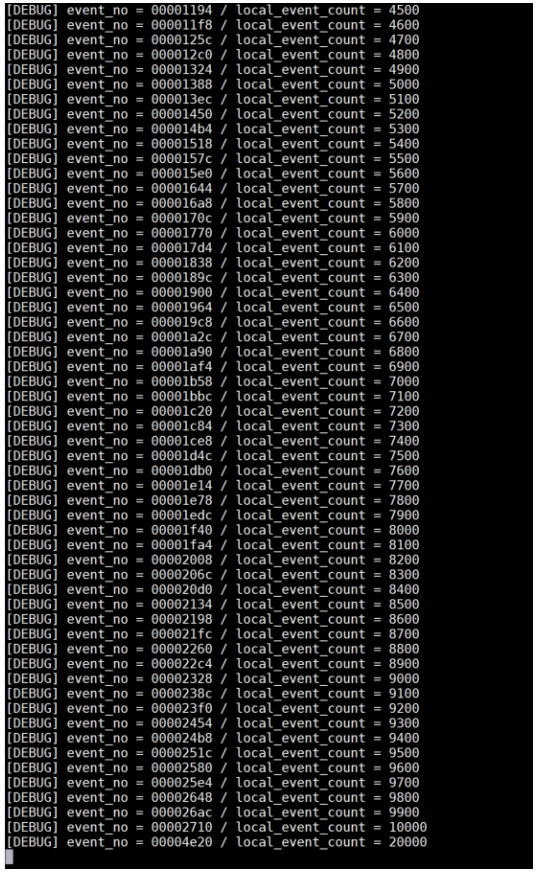
- Setup on BIOS menu to avoid bugs: Advanced >>Chipset Configuration>>North Bridge>>IIO Configuration>>II01 Configuration. 8x8 configuration is needed to choose.

- Slow Control Test.

```
[belle2daq@pc1-belle2 Scripts]$ python2 testSLC.py --channel 9 --detector CDC 1000
0
Total number of errors = 0
[belle2daq@pc1-belle2 Scripts]$
```

- Data Reading Test.





Test in KEK

- The coming test is the speed test, to see whether the firmware can be push to the limit 100 Gb/s.
- The trigger rate has been tried to push to 4000000 Hz, but it was still too far from the limit, only 281.74 Mb/s.
- Our plan is to try to increase the size of the test-event.

  Instead of using the test-event in the “copper”, the event directly generated by PCIe40 seems more useful.
- Using the event generated by PCIe40 itself can also ensure the transfer rate limit is not from the other components.
- To use the data generated by PCIe40, the disabled generator would need to be enabled again.

  The firmware is kept modifying and testing.

```
49  //pcie40_enableGenerator( 0 ) ;
50  //pcie40_useDataFromGenerator( 0 ) ;
51  pcie40_disableGenerator( 0 ) ;
52  pcie40_useDataFromFibers( 0 ) ;
```

```
413  -   data_flow_controller_data <= scientific_data when pio_cmd13(9) = '1' else data_out_test;
414  -   data_flow_controller_wren <= wr_scientific_data when pio_cmd13(9) = '1' else wr_en_test;
     413 +   data_flow_controller_data <= scientific_data; --  when pio_cmd13(9) = '1' else data_out_test;
     414 +   data_flow_controller_wren <= wr_scientific_data; --  when pio_cmd13(9) = '1' else wr_en_test;
```

Plan on Optical b2tt

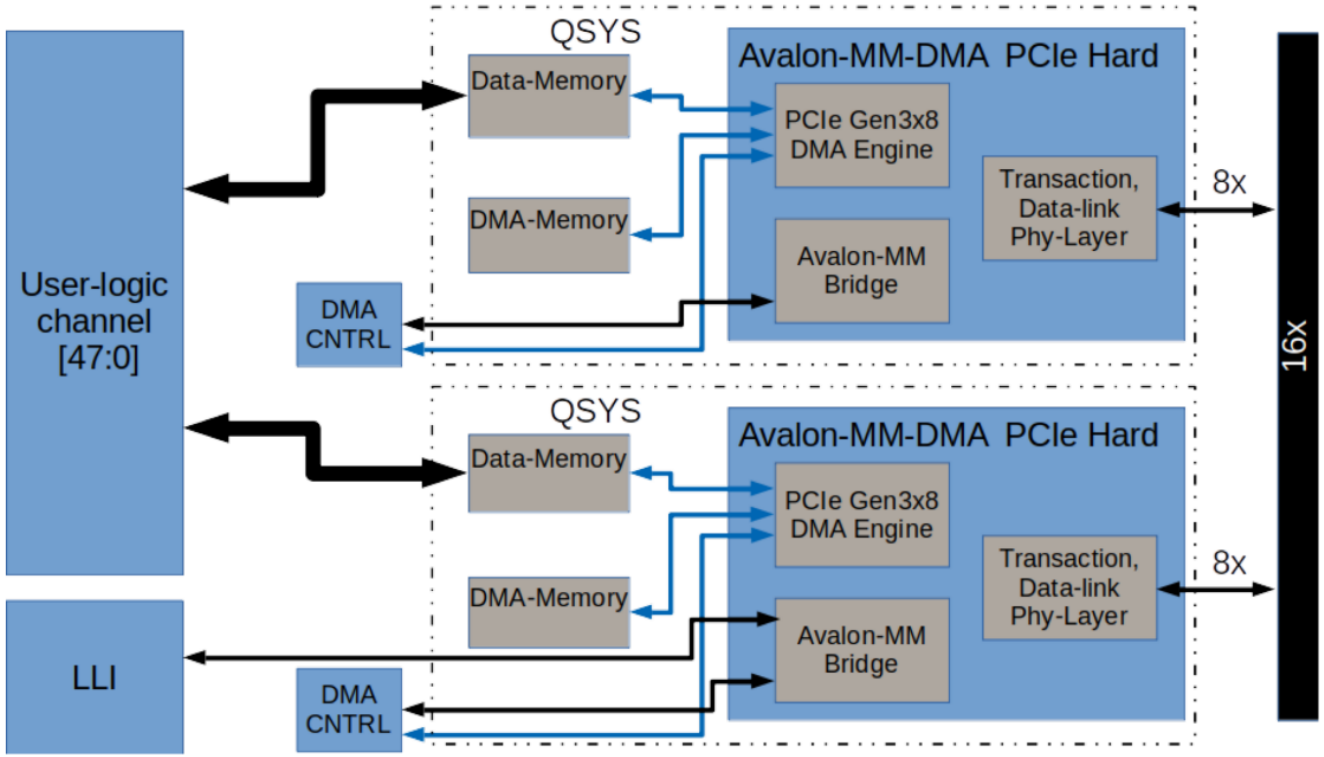
- Use fibers for PCIe40-FTSW connection instead of LAN cable
- The FTSW upgrade is also necessary.
- I’m joining for modifying and testing the firmware.

Conclusion

- The firmware is kept updating and testing.
- The “doublepci” shows no error for data reading test and slow control test, but not yet the rate test.
- The optical b2tt firmware is under developing.
- A new board is under developing.

Appendix :
The Double DMA interface

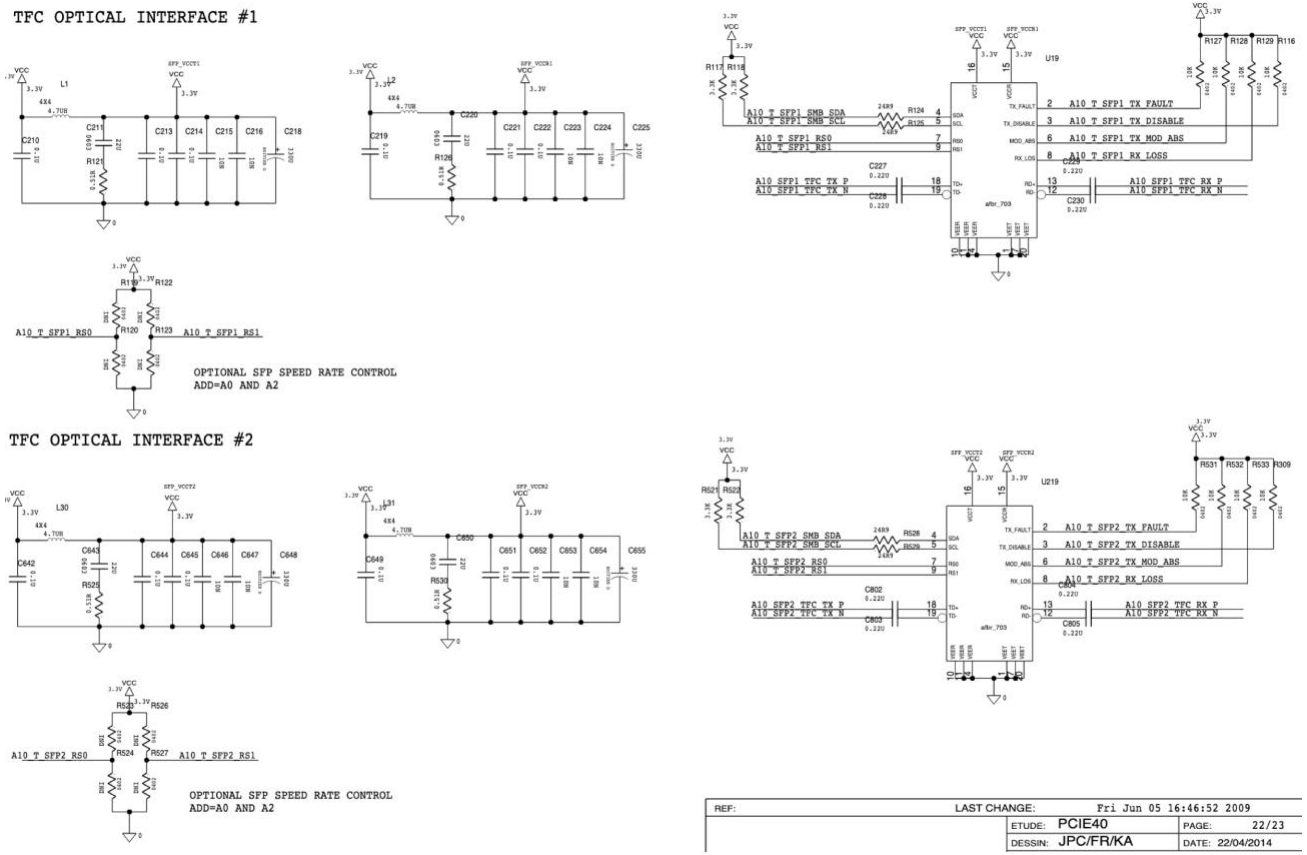
- Increase data rate from PCIe40 to PC server by using the 2 DMA interfaces available (instead of 1 now)



https://indico.belle2.org/event/5891/contributions/31346/attachments/14699/22105/Belle2_DAQB2GM_17Jan2022.pdf

Appendix : B2TT via optical links

- Try to use b2tt directly with optical links into the PCIe40 board.
- Two optical SFP interfaces available on the PCIe40 board and not used at the moment.



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