Belle2Link Upgrade Project

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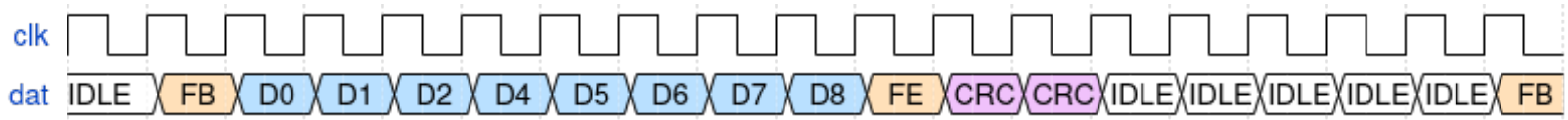
Belle2Link Overview

- Purpose: transmission of data and configuration information between FEE and read-out electronics
- Medium: multimode optical fiber
- Hardware: Xilinx and Intel FPGA
- Signaling rate: 2.5 Gb/s
- Encoding: 8b10b

Data Flow on the Belle2Link



- Data/Slow control frame layout
  - 2 commas for begin/end of frame
  - up to 9 data words
  - 2 words with CRC
  - 5 IDLE words: artificial throttling
- Maximum link efficiency: $\frac{9}{18} = 50\,\%$

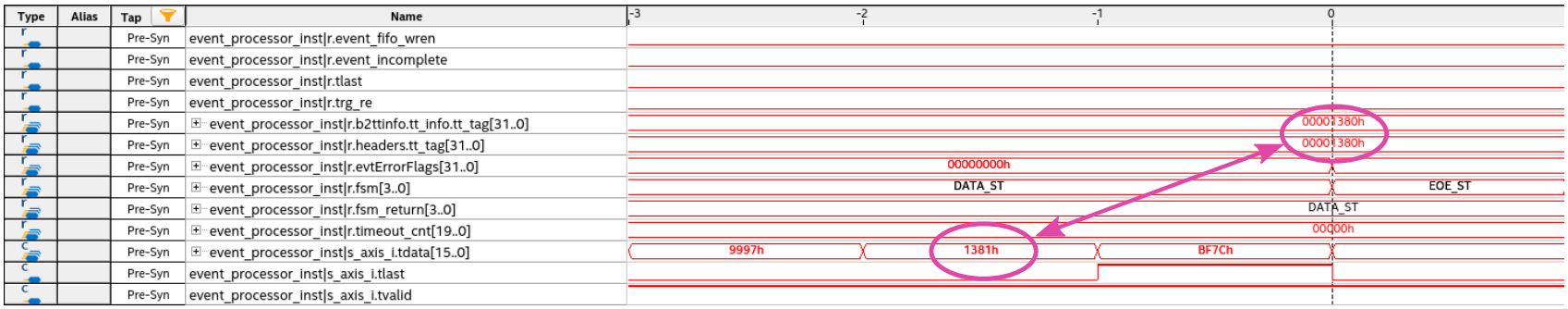
Motivation

Belle2Link Upgrade Project

- Prepare Belle2Link for higher data rates
  - can still be done while keeping singaling rate
  - faster data transport from FEE
- Reduce probability of data loss
  - improve DAQ efficiency
- Upgrade "under the hood"
  - backwards compatibility
  - no change in link initialization
  - keep interface to FEE
  - add optional signal

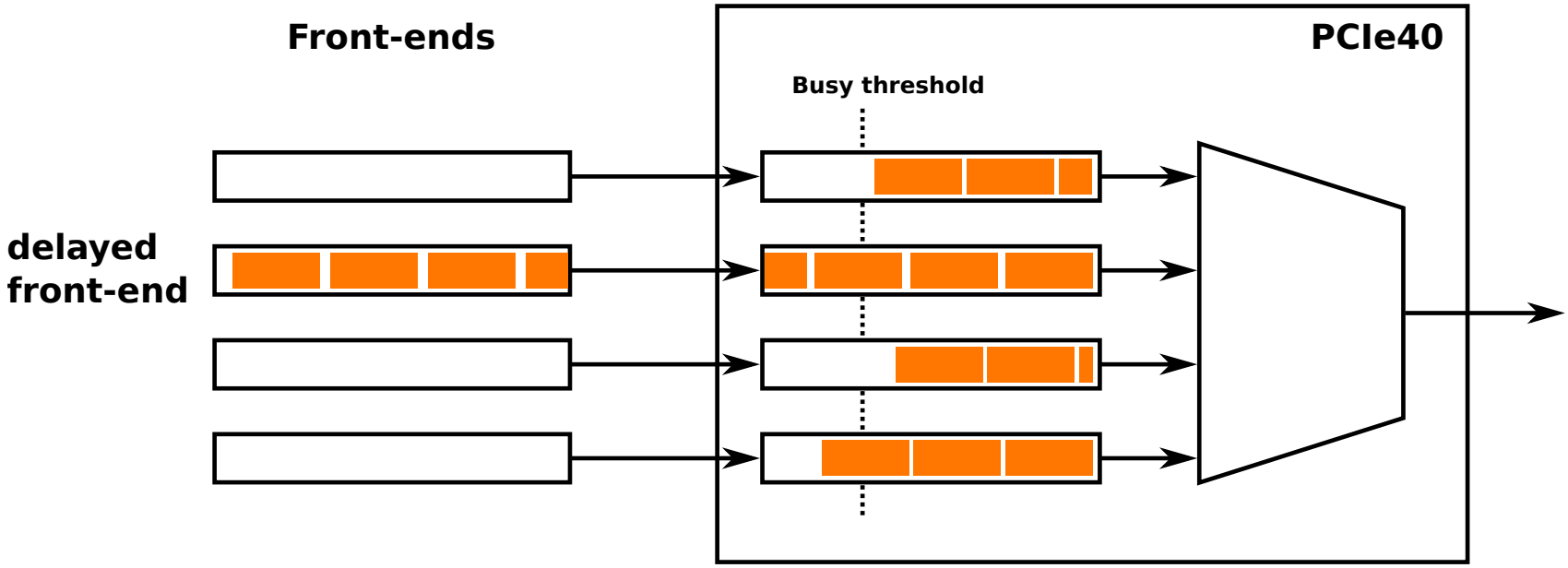
PCIe40 Handling Delayed Data

- In general, **no problems** with data delay up to 6 ms on one channel even at high trigger rates (22 kHz)
  - only if **far from throughput limit**
- **Data mismatch** if operated at throughput limit
- Event mixup in the channel with delayed data



- Two events merged to one
  - lost last data word of the first event
- System stability depends on the error rate
  - can recover if slightly above throughput limit
  - no recovery if far above limit

Backpressure Problem



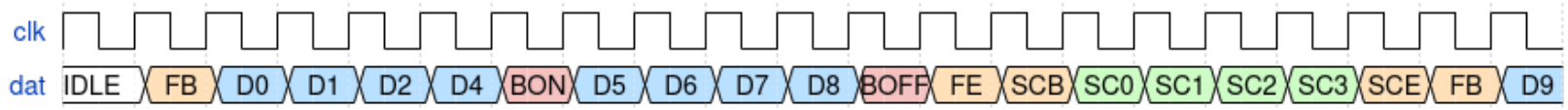
- Data in front-ends after busy issued
- Starts at constant delay if event size is constant
  - time needed to transmit event

Possible Solutions

- Implement data throttling for B2L data in PCIe40
  - end the event if FIFO is close to being full
  - problematic for the HLT
- Add backpressure to B2L
  - can be implemented as a suggestion to keep backward compatibility
  - front-ends with buffer will be able to hold data to prevent FIFO overflow
  - front-ends without buffer will behave in the same way as now
  - data throttling is still needed

Backpressure

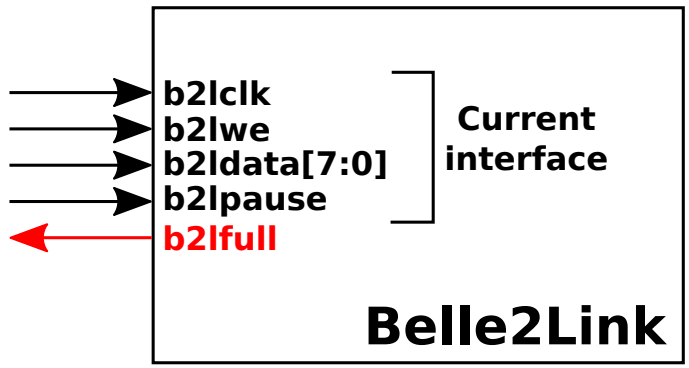
Backpressure mechanism



- Transmit backpressure k-character (0xDC) with the status of bacpressure
- Set flag to indicate condition to the backpressure
- Select timing to be able to receive all data in Belle2Link FIFO
  - 64 words
- Backwards compatible to original behaviour
  - Belle2Link will continue to send data with backpressure ON

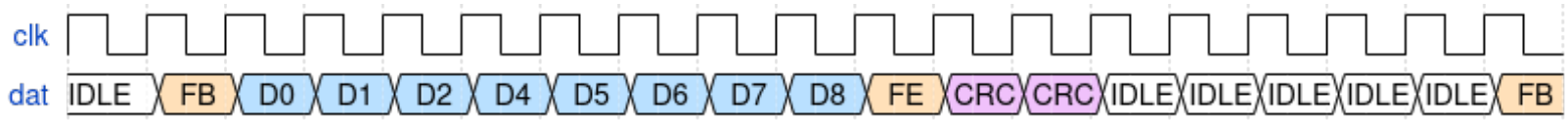
Backpressure mechanism

- **b2lfull** signal
  - PCIe40 to FEE
- **'0'**: normal operation
- **'1'**: "Please stop sending data if you can"



Increase of the Throughput

Data Flow on the Belle2Link



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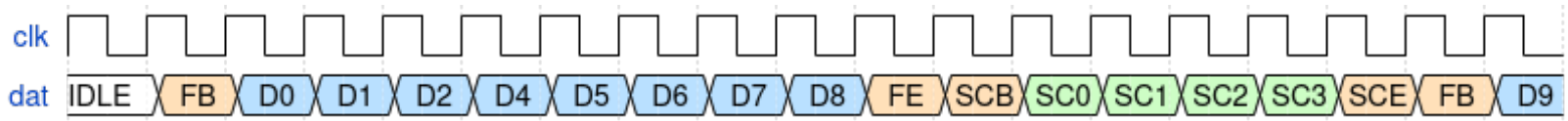
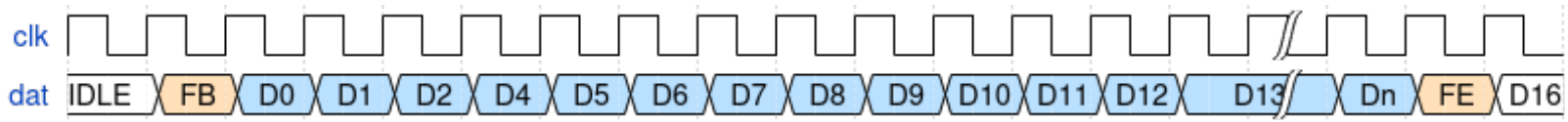
Bypass Idle States and CRC



- Remove IDLE states and CRC words
- CRC not used at the moment
  - no reason to use if no retransmission
  - better use error counter based on the 8b10b decoder error signal
- Maximum link efficiency: $\frac{9}{11} = 82\,\%$

Uninterrupted Data Flow



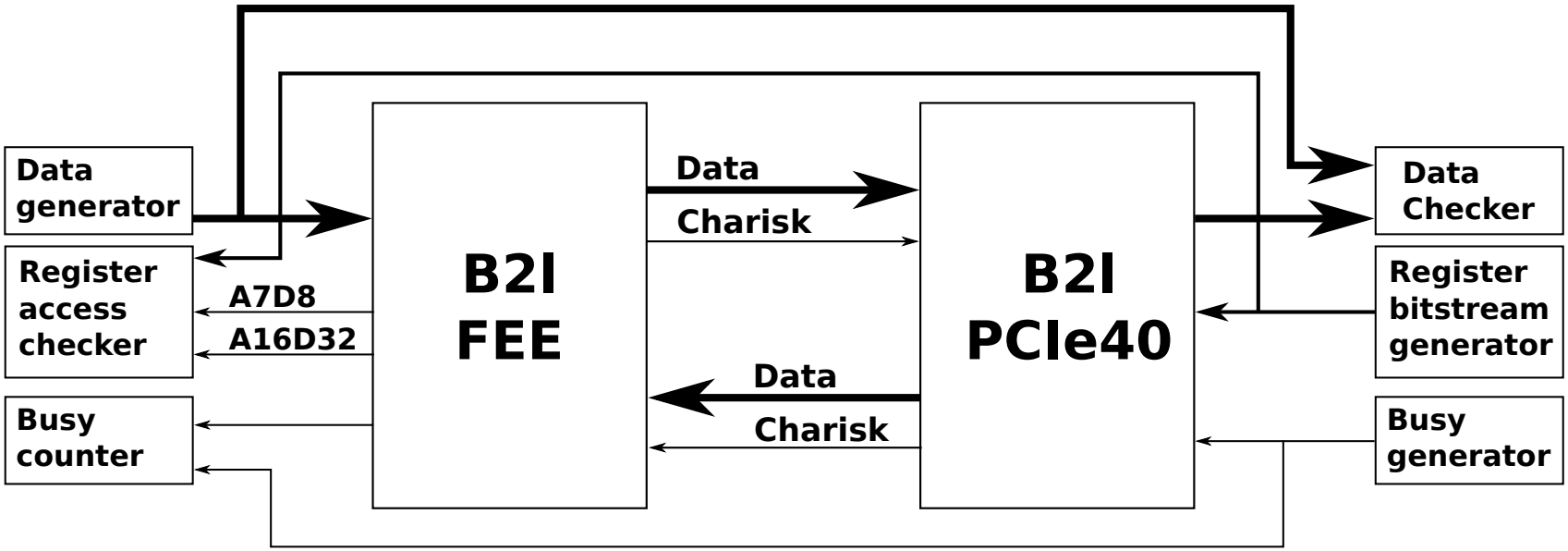
- Transmit full data Uninterrupted
- Maximum efficiency goes to 100 % for long frames
- Long delay for slow control frames

Slow control Preemption

- Interrupt data frame to transmit slow control frame
- Schedule to delay slow control frames if data FIFO fill level high
- Maximum efficiency goes to 100 % for long frames
- Will require substential change to the source code
  - **interface to the FEE will not be changed**

Tests in Simulation

Simulation Setup



- Fully automatic checks
- Data checks
  - UVVM BFMs for AXI4Stream
  - use existing adapters to B2L interface
- Register checks
  - A7D8, A16D32, bitstream interfaces
- Busy checks
  - count number of rising/falling edges on both sides of the link

Simualtion Result

- Simulated conditions:
  - backpressure transmission
  - removal of the IDLE and CRC states
- Simulation completed successfully

```
# ** Note: Full flag statistics
#    Time: 262605520 ns  Iteration: 0  Instance: /belle2link_tb
# ** Note: Src/dst: falls = 1458938 / 1458938, rises = 1458939 / 1458939
#    Time: 262605520 ns  Iteration: 0  Instance: /belle2link_tb
# ** Note: Diff: falls = 0, rises = 0
#    Time: 262605520 ns  Iteration: 0  Instance: /belle2link_tb
# UVVM:
# UVVM:      ================================================================================
# UVVM:      *** FINAL SUMMARY OF ALL ALERTS ***
# UVVM:      ================================================================================
# UVVM:                                  REGARDED   EXPECTED  IGNORED      Comment?
# UVVM:                NOTE         :      0          0         0         ok
# UVVM:                TB_NOTE      :      0          0         0         ok
# UVVM:                WARNING      :      0          0         0         ok
# UVVM:                TB_WARNING   :      0          0         0         ok
# UVVM:                MANUAL_CHECK :      0          0         0         ok
# UVVM:                ERROR        :      0          0         0         ok
# UVVM:                TB_ERROR     :      0          0         0         ok
# UVVM:                FAILURE      :      0          0         0         ok
# UVVM:                TB_FAILURE   :      0          0         0         ok
# UVVM:      ================================================================================
# UVVM:      >> Simulation SUCCESS: No mismatch between counted and expected serious alerts
# UVVM:      ================================================================================
# UVVM:
# UVVM:
# %% DONE  PASSED  AlertLogTop  Passed: 4334194  Affirmations Checked: 4334194  at 262605520 ns
```

Summary

- Proposed changes to the Belle2Link
  - all changes backwards compatible
  - no changes in link initialization

1. Backpressure transmission to FEE to prevent FIFO overflow in PCIe40
   - successfully verified
2. Increase of the throughput by removing IDLE states and CRC
   - successfully verified
3. Transmission of long frames and preemtion by slow control frames
   - development not started yet