

TOP DAQ in 2022 runs

HARSH PURWAR

University of Hawaii at Mānoa (UHM), High Energy Physics Group
Dept of Phys & Astr, Honolulu, HI, USA

Email: purwar@hawaii.edu

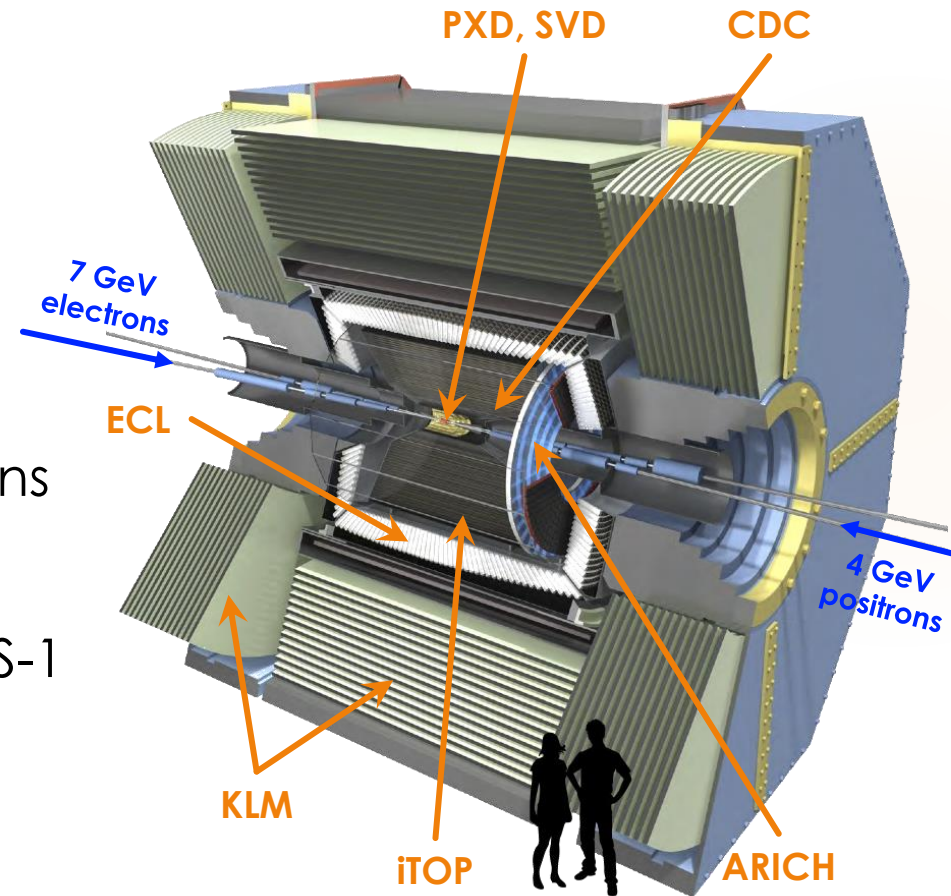
Martin Bessner, Hülya Atmacan, Yinghui Guan, Kazuki Kojima, Akane Maeda, Ryogo Okubo, & Noritsugu Tsuzuki



Outline of the talk

2

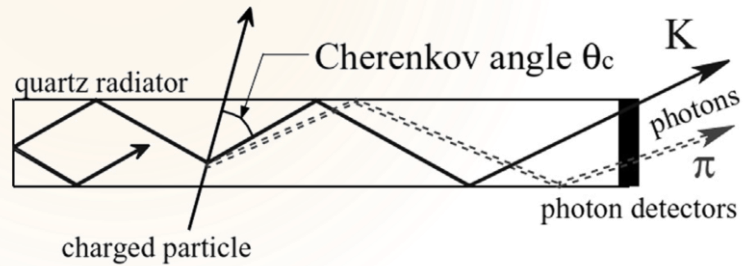
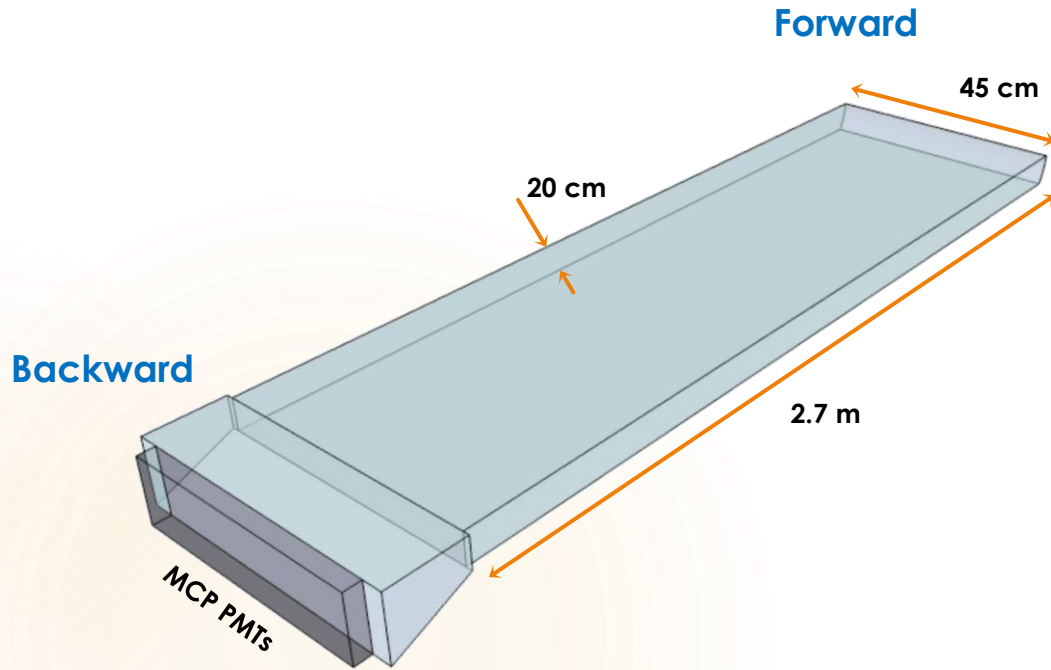
- ▶ Introduction to iTOP detector
- ▶ Detector initialization, control & DQM
- ▶ Improvements made in iTOP Operations
- ▶ Hardware issues & replacement plans
- ▶ Other planned development during LS-1



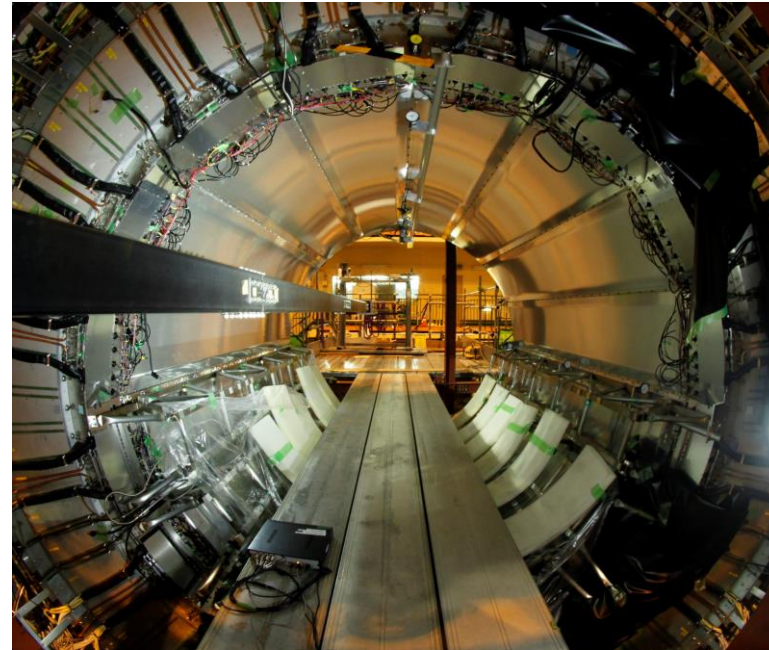
Harsh Purwar, HEPG, UHM, Honolulu, HI, USA
Nov. 29th, 2022

iTOP

Imaging time of propagation detector at Belle II

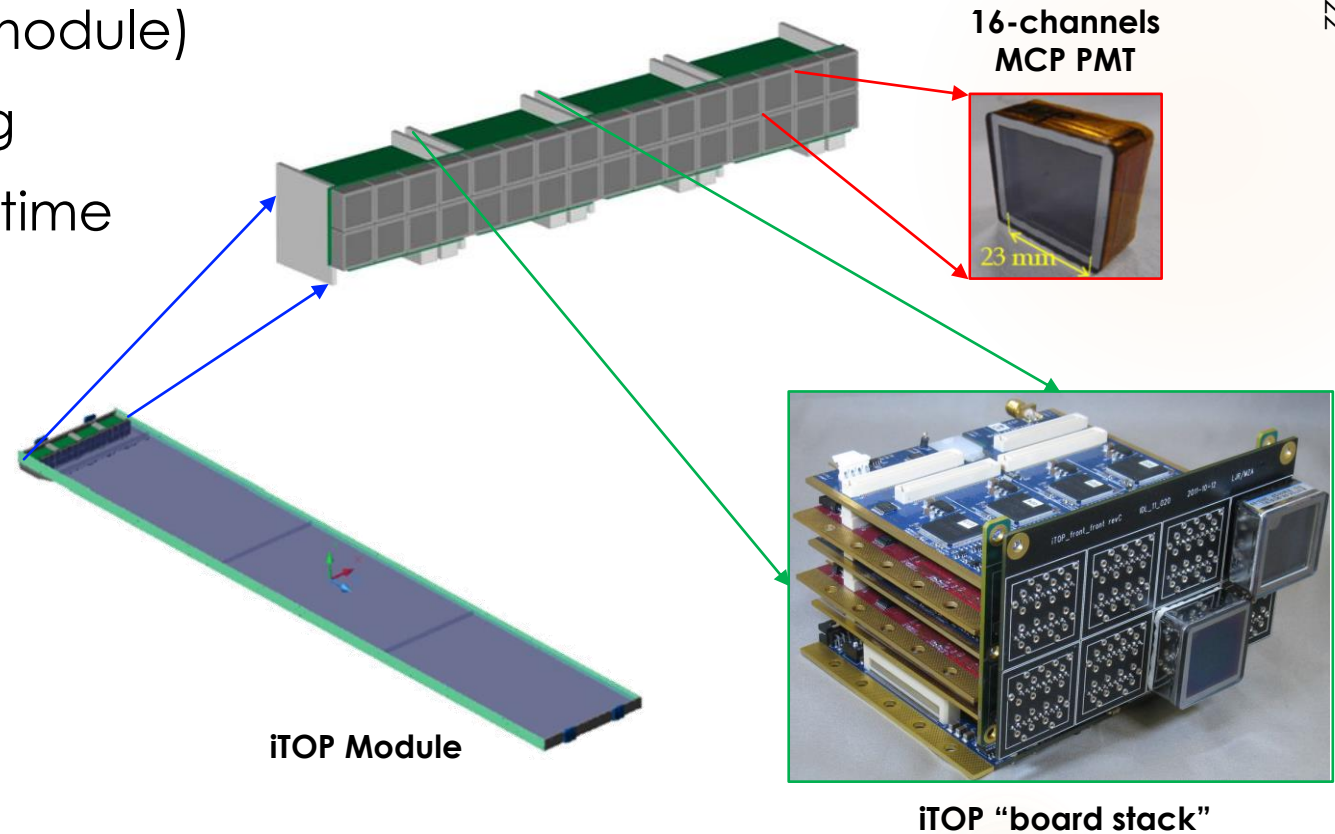


16 quartz modules arranged azimuthally around the beam pipe near the IP



Micro Channel Plate (MCP) Photomultiplier Tubes (PMT)

- ▶ 32 16-channels MCP PMTs per iTOP module (512 ch/module)
- ▶ single photon counting
- ▶ 10^6 gain, under 100 ps time resolution



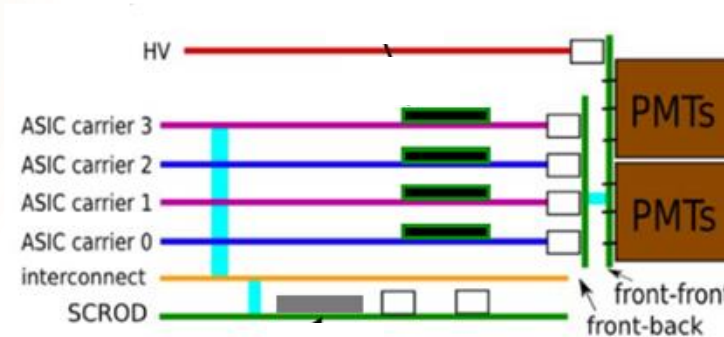
iTOP "board stack"

TOP board stack assembly

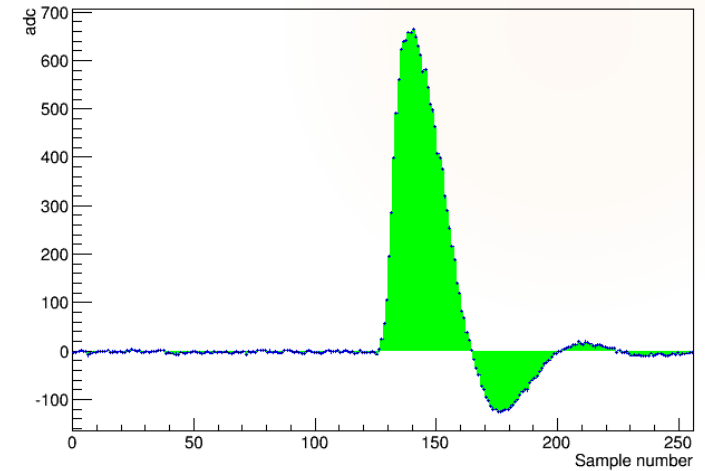
Carrier board – 4 ASIC per carrier



TOP board stack



Example waveform



Readout/Digitization of PMT pulses

IRSX Waveform Sampling ASICs

- ▶ PMTs instrumented by waveform sampling IRSX ASIC based electronics
 - ▶ 2.7-4 GHz sampling IRSX ASICs developed at U. Hawaii
 - ▶ IRSX continuously sample PMT signals, 8 channels/ASIC
 - ▶ Digitize PMT pulses with zero deadtime, $\sim 10 \mu\text{s}$ analog circular buffer
 - ▶ Design goal: $< 50 \text{ ps}$ time resolution
- ▶ IRSX ASICs integrated into “board stack” front end electronics
 - ▶ Front end board stack contains 16 ASICs (128 channels)
 - ▶ FPGA based data collector board (SCROD) receives digitized ASIC data
 - ▶ 4 board stacks per iTOP module (512 channels)
 - ▶ Performs threshold triggering and provides trigger info to Belle II trigger GDL

Recap

- ▶ A charged particle hits the iTOP quartz bar, produces Cherenkov photons.
- ▶ These photons totally internally reflect and eventually reach the MCP PMTs located on the rear end of the bar.
- ▶ TOP board stacks are used to readout the PMT pulses and extract useful info from these (like, energy, time, pulse width) after pedestal subtraction.
- ▶ The IRSX ASICs also provide trigger information to Belle II trigger Global Decision Logic.
- ▶ The formatted data from TOP SCROD boards is then readout by the readout board (PCIe40) via Belle2Link (optical fiber link).

iTOP Detector Initialization, Control & DQM

iTOP Detector Initialization

(Detector slow control)

- ▶ Before reading good sensible data, the iTOP sub-detector FEs need to be initialized or configured, also referred as detector slow control (SLC).
 - ▶ Setting thresholds, readout window sizes, taking pedestals, etc.
- ▶ SLC also includes detector monitoring – PMT hit rates, temperatures, voltages, etc.
- ▶ *Happens through the readout board (PCIe40), which interacts with the FEE over the same **B2L** (or optical link).*
- ▶ **iTOP**
 - ▶ Uses standalone python scripts and GUIs for detector initialization
 - ▶ daq_slc library for monitoring and archiving

iTOP run control & monitoring GUIs

Available to all TOP shifters

Run control panel

Other monitoring variables: temp., LV, etc.

PMT hit rate monitoring panel

PMT hit rate monitoring panel

iTOP Power-cycle & Config. GUI

Available to iTOP shifters (simplified version) & iTOP experts (full version)

The screenshot displays the iTOP Power-cycle and Configuration GUI. The window title is "TOP Power-cycle and Configuration GUI - developed at UHM, Honolulu, Hawaii, USA". The interface is divided into several sections:

- Top Status Bar:** Shows "MASTER FTSW (184): RUNNING", "Exp: 27 Run: 1143 (0)", "TOP FTSW (65): ERROR (LOCAL)", "Exp: 0 Run: 0 (0)", and "TOP HV UNKNOWN".
- Channel Selection:** Two columns of checkboxes for "RTOP - 1" and "RTOP - 2", each with 31 channels (s01a-ch00 to s08a-ch31 and s09a-ch00 to s16a-ch31).
- Slot Configuration:** Four panels for slots s10a-ch04, s10b-ch05, s10c-ch06, and s10d-ch07. Each panel shows a list of 32 entries with numerical values and status indicators.
- Bottom Control Panel:** Includes checkboxes for "Configure", "Pedestals", "Cal pulses: Enabled", "Waveform RO: Disabled", "Set/Scan Thresholds", "Lookback", "Readout Win", "Post-config regs", "FEE Firmware", and "Save pedestals to file".
- Action Buttons:** "Power-cycle" and "Configure" buttons with a power icon.

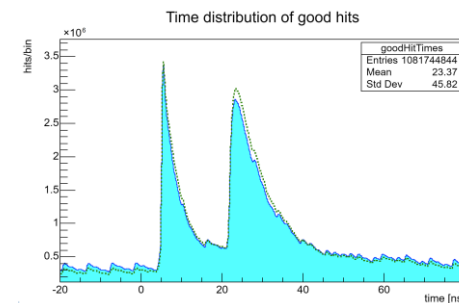
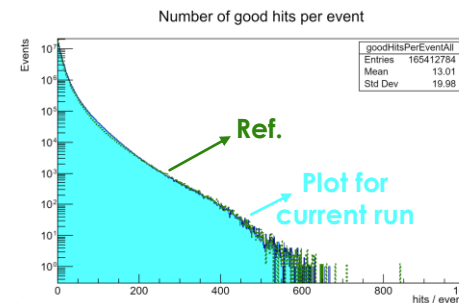
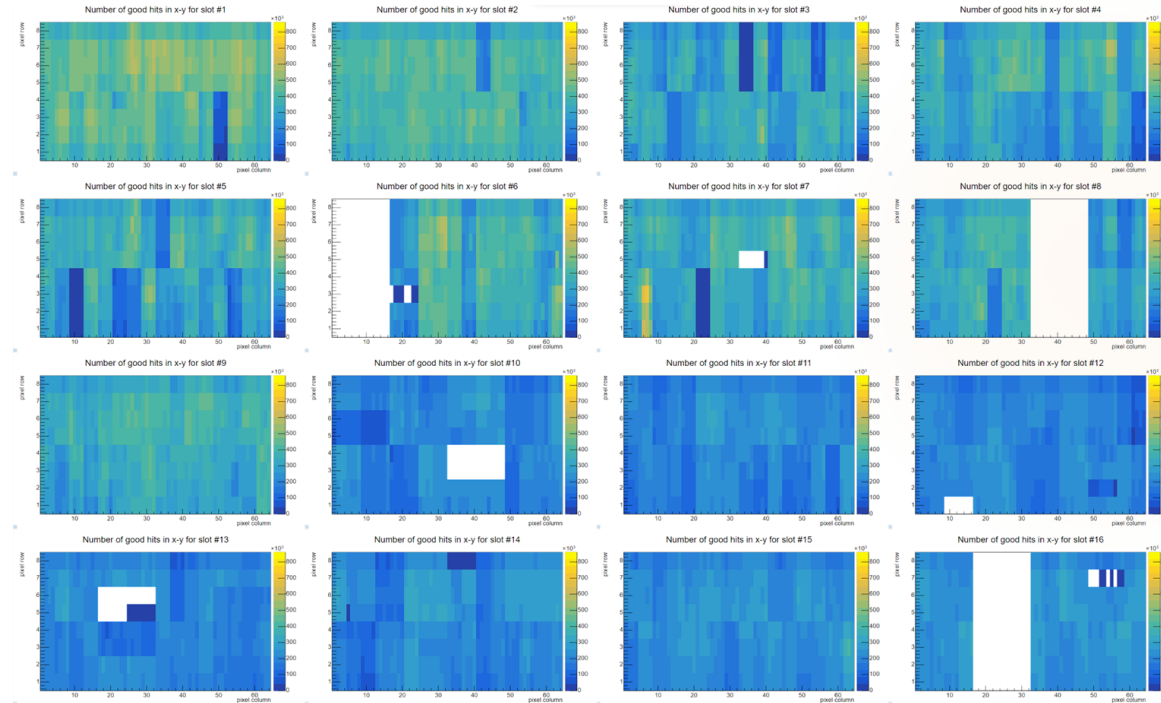
iTOP Data Quality Monitoring (DQM) plots

12

Harsh Purwar, HEPG, UHM, Honolulu, HI, USA
Nov. 29th, 2022

- ▶ Several DQM plots are available to iTOP shifters and CR shifters to monitor the quality of iTOP data being recorded almost in real time.
- ▶ These plots are extremely helpful in troubleshooting a detector hardware malfunction during a run or if the initialization for one or more iTOP frontends is incorrect for a physics or cosmic run.
- ▶ A well studied reference plot is shown on top of the plot for the current (or ongoing) run for quick comparison.

Examples of DQM plots for iTOP
(run 25, exp. 400)



iTOP Data Quality Monitoring (DQM) plots

13


- ▶ Several DQM plots are available to iTOP shifters and CR shifters to monitor the quality of iTOP data being recorded almost in real time.
- ▶ These plots are extremely helpful in troubleshooting a detector hardware malfunction during a run or if the initialization for one or more iTOP frontends is incorrect for a physics or cosmic run.
- ▶ A well studied reference plot is shown on top of the plot for the current (or ongoing) run for quick comparison.
 - ▶ A difference plot could also be helpful to quickly look at anomalies during the run.
 - ▶ Automatic error/notifications in RC in case the difference is greater than some set threshold is another useful feature that could be added.
- ▶ As of now, DQM plots are only available for global runs (no DQM plots for iTOP local runs)


Issues, Improvements and Plans

Recent improvements in iTOP Operations

15

- ▶ Recovering dead/bad iTOP board stacks during a run
- ▶ iTOP Power-cycling GUI made available to iTOP shifters – takes tons of load off iTOP experts
 - ▶ As a result, reduced the number of masked board stacks in runs
- ▶ Improved masking scheme (more robust and consistent)
- ▶ Significantly faster and automated recovery procedures
- ▶ RC alerts for all known iTOP or DAQ - related issues

 elastalert @rocket.cat Bot 7:09 AM
TOP stops run at 2022-05-26 07:08 JST ▼
TOP causes 100% DAQ dead time.
If it stopped the run then a boardstack needs to be masked.

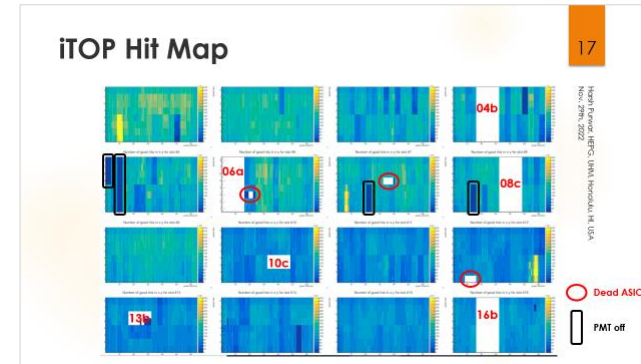
 elastalert @rocket.cat Bot 7:09 AM
TOP scrod stop/reset at 2022-05-26 07:09 JST ▼
TOP boardstack s02b stopped.
CR shifters: Please stop, abort and run the maskstoppedBS.py script to mask this boardstack. Then start a new run.
Contact TOP shifter in case of problems.
TOP shifter: Please check and document this.

Current iTOP hardware issues

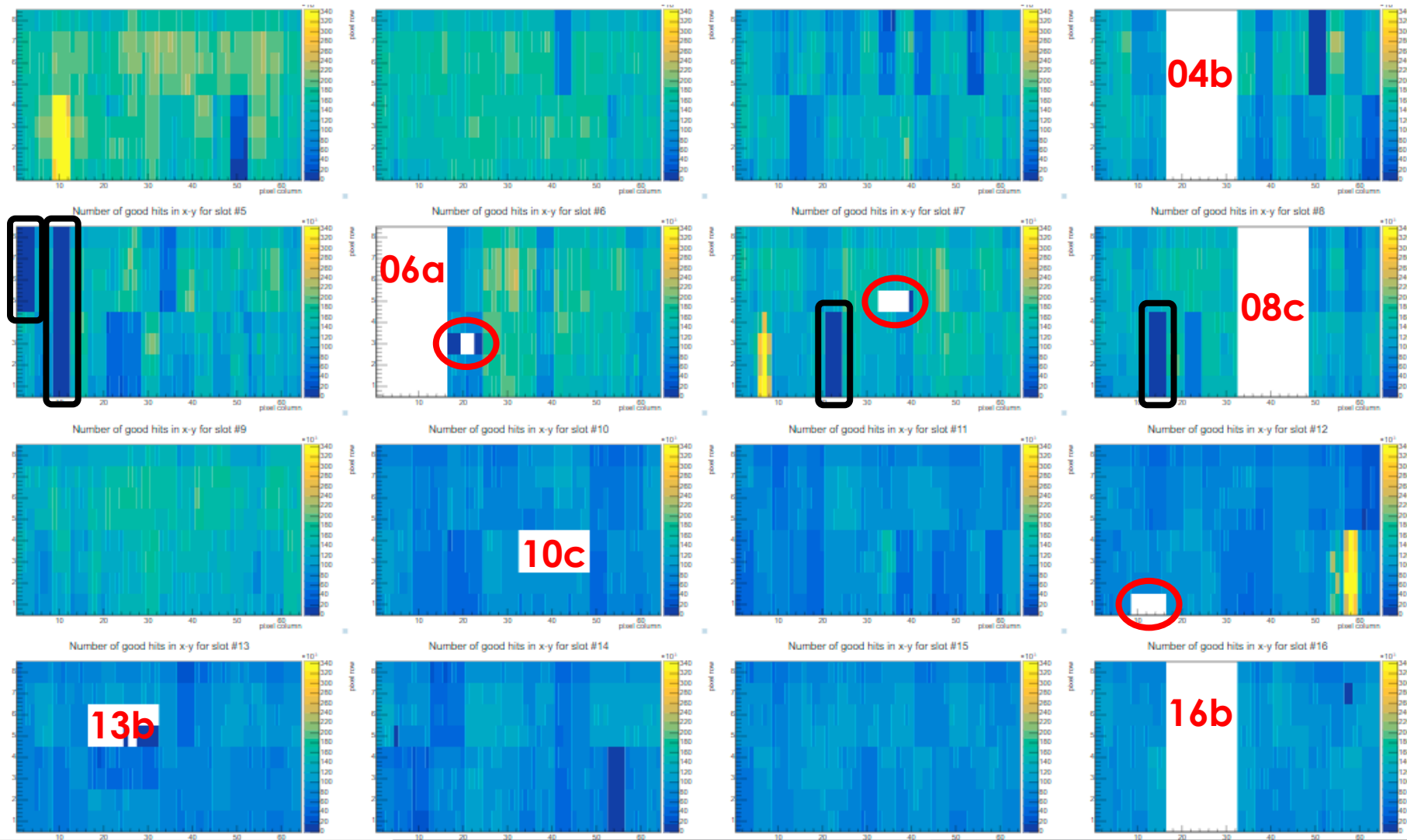
To be fixed during LS1

16

- ▶ Dead board stacks – to be replaced during LS-1
 - ▶ s04b, s13d – Lost JTAG connection
 - ▶ s05a – no calibration pulses
 - ▶ s06a – B2link down (broken transceivers?)
 - ▶ s08c – bad low voltage connection
 - ▶ s10c – 1 carrier sends no hits – uses old firmware
 - ▶ s10d – Often goes into “bad state” & causes large deadtime
 - ▶ s13b – sends suspect trigger data and is missing one carrier
 - ▶ s07a, s14c – Needs to cool down before programming
 - ▶ s16b – DDR memory failure – Slot 16 has **already been unmounted and is in process of replacement or repair**
- ▶ All MCP PMT modules in slot 16 will be checked
 - ▶ to confirm the QE in Nov-Dec at Nagoya
 - ▶ to investigate the reason for hot PMTs
- ▶ Replacement of several other PMTs will also be carried out during LS-1 depending on the QE analysis of slot 16 PMTs



iTOP Hit Map



○ Dead ASIC
▭ PMT off

Planned improvements during LS-1

18

- ▶ Hardware replacements (Inami, Bessner)
- ▶ Migration of TOP Pedestal subtraction and Feature extraction from TOP FEE (currently done in SCROD PS) to TOP ROPCs (Kohani)
- ▶ Saving TOP Pedestals in top db and retrieving these values during LOAD operation for online pedestal subtraction (Purwar)
 - ▶ Acquiring TOP pedestals **in parallel** for all TOP frontends using PCIe40 – May need minor modifications in pcie40_regconfig command (need to be able to write multiple registers for different channels at the same time)
- ▶ Improvements in Automated recovery scripts – provide a TOP recovery GUI to CR shifters (Bessner)
- ▶ Auto masking on known error and auto unmask board stacks after recovery/power-cycle on the next beam stop (Bessner, Purwar)

Thank you for your time and attention.

- Harsh Purwar
purwar@hawaii.edu