

SVD readout

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SVD readout system overview



FADC and FTB boards

FADC board



- 10-bit ADC, finite Impulse Response (FIR) filtering, and data formatting w/ Zero-Suppression
- Provide SVD standalone data taking
 - Pedestal, noise, calibration, IV runs
- Altera(Intel) Stratix IV
 - reprogrammable through VME



FTB board



- transmits FADC data to DAQ via b2link
 - 1.27 Gbps
 - and also to DATCON via aurora link
- 1U board
- Xilinx(AMD) Spartan-6 FPGA
 - reprogrammable by FTSW

SVD PCIe40 migration

Expected data rate



- Expectation of total SVD event size: 90 kB
- Expectation of total SVD data rate @ 30kHz: 2.7 GB/s
- **5 PCIe40/ROPC sets** for SVD
 - Expected SVD data rate per ROPC @ 30kHz: about 540 MB/s (= 2.7 GB/s / 5 ROPC)
 - Max. bandwidth of PCIe40/ROPC: about 870 MB/s (w/o software CRC calculation)
 - may be improved in the future by changing the network configuration from 10Gbps to 25Gbps.

COPPER #

SVD PCIe40 test status

SVD data rate test results on Sep 7, 2022

| ZS cut [SNR] | CRC check in ROPC | Input trigger [kHz] | Output trigger [kHz] | Average SVD hit occupancy | Data rate @ RSVD1 [MB/s] |
|-----------------|-------------------------|---------------------------|----------------------------|---|--------------------------------|
| 3.0 | ON | 30 | 27 | L3: 0.5%, L4: 1.0%, L5: 1.1%, L6: 1.1% | 205 |
| 2.8 | ON | 30 | 27 | L3: 1.1%, L4: 1.7%, L5: 1.9%, L6: 1.9% | 312 |
| 2.6 | ON | 30 | 27 | L3: 2.0%, L4: 3.0%, L5: 3.1%, L6: 3.3% | 463 |
| 2.4 | ON | 30 | 23 (13% deadtime) | L3: 3.6%, L4: 5.1%, L5: 5.6%, L6: 5.6% | 640 |
| 2.4 | OFF | 30 | 27 | same as above | 742 |
| 2.2 | OFF | 30 | 25 (7% deadtime) | L3: 6.0%, L4: 8.0%, L5: 8.4%, L6: 8.6% | 1006 |
| 2.0/2.1 | OFF | | | SVD ferr (possibly FADC FIFO full due to the FTSW busy handling issue) \rightarrow BU | JSY from PCle |

Tested with the SVD noise increased by lowering the ZS threshold.we increased ZS threhold.

- Limit w/ CRC check in ROPC: about 640 MB/s per ROPC
- Limit w/o CRC check in ROPC: about 1000 MB/s per ROPC
- Long-term stability is to be checked (ongoing w/ FTB dummy data)

Tool Setup for SVD PCIe40

GUI prepared by Z. Qidong



Channel Map between FTB and PCIe40

| | rsvd1 | rsvd2 | rsvd3 | rsvd4 | rsvd5 |
|-------|--------|--------|--------|--------|--------|
| ch.0 | FTB#1 | FTB#13 | FTB#23 | FTB#36 | FTB#44 |
| ch.1 | FTB#2 | FTB#14 | FTB#24 | FTB#37 | FTB#45 |
| ch.2 | FTB#3 | FTB#15 | FTB#25 | FTB#38 | FTB#46 |
| ch.3 | FTB#4 | FTB#16 | FTB#26 | FTB#39 | FTB#47 |
| ch.4 | FTB#5 | FTB#17 | FTB#27 | FTB#40 | FTB#48 |
| ch.5 | FTB#6 | FTB#18 | FTB#28 | FTB#41 | FTB#49 |
| ch.6 | FTB#7 | FTB#19 | FTB#29 | FTB#42 | FTB#50 |
| ch.7 | FTB#8 | FTB#20 | FTB#30 | FTB#43 | FTB#51 |
| ch.8 | FTB#9 | FTB#21 | FTB#31 | | FTB#52 |
| ch.9 | FTB#10 | FTB#22 | FTB#32 | | |
| ch.10 | FTB#11 | | FTB#33 | | |
| ch.11 | FTB#12 | | FTB#34 | | |
| ch.12 | | | FTB#35 | | |

• GUI for the SVD experts is being prepared by K. Hara.

- FTB ID, data mode, data rate to be added

A script to read and write the FTB data mode for all FTBs is prepared.

– b2svd@rsvd1: ~/svd_daq_pcie40/ftb_mode_nsm.py

Now only FTB dummy data (random pattern) are available for SVD PCIe40 test

– Hopefully, I will implement another FTB dummy data with the real data format.

VXD commissioning during VXD reinstalation

Commissioning plan of new VXD in B4 clean room

Assembled VXD (2018)



VXD commissioning (2018)



TT-IO in e-hut





- VXD will be replaced with new VXD in LS1. Before the installation, the new VXD is to be tested in the B4 clean room with cosmic ray data taken by scintillator triggers.
 - Roughly check S/N ratio, efficiency, and alignment
 - Had the same commissioning in 2018
- Necessary setup for the data taking should already exist:
 - Optical cables for b2link and b2tt signals are installed between e-hut and B4 clean room.
 - Triggers (NIM signal) are provided with LEMO cable. There is a TT-IO module in e-hut installed to convert it to the AUX signal which is connected to FTSW#233.
 - Can we still use the same setup for the commissioning? Maybe we have to change the FTSW to #184 for the global DAQ?
 - All 32 ONSEN inputs to EB2 are to be activated, setup already prepared
- VXD has to occupy the global DAQ during this commissioning period
 - Anticipated 2-3 weeks (TBD by examining the necessary statistics) in summer or autumn 2023

3/6-mixed sample mode

Benefits of 6/3-mixed sample mode

Mitigation of trigger deadtime

- Trigger deadtime in 6-sample mode:
 - more than 1% at 25kHz trigger rate
 - about 3% at 30kHz trigger rate
- Trigger deadtime in 3-sample mode:
 - less than 1% at 30kHz
 - about 1% at 50kHz

Reduction of the DAQ data size

- Expected total SVD data rate at 30kHz: 2.7 GB/s
- In the COPPER system, the ROPC bandwidth was merginal.
 - ~250MB/s x 9 ROPCs = ~2.3GB/s
- In the new PCIe40 system, the bandwidth should be enough.
 - ~640MB/s x 5 ROPCs = ~3.2GB/s
 - ~870MB/s x 5 ROPCs = ~4.4GB/s (if CRC check in ROPC software can be omitted)



Not mandatory for the PCIe40 readout system

Tracking performance: 6-sample vs. 3-sample



- In future high beam-BG conditions, we anticipate the BG rejection with a hit-time selection will be required to maintain the tracking performance.
- Applying hit-time selection of |t_{svD}|<50ns, the tracking performance was compared between 6-sample and 3-sample.
- While in 6-sample the fake track rate is improved mode by a lot, in 3-sample the improvement is small.

Possible further BG rejection in 3-sample mode

• The tracking group is improving the tracking algorithm:

- 1. Perform usual tracking
- 2. Extract precise event T0 information from the SVD hits associated to tracks
- 3. Re-estimate quality of tracks using the T0 information
- 4. Distinguish the physics tracks and BG tracks based on the estimated quality
- The implementation of the new algorithm is ongoing.

 With the improved track reconstruction, we may improve the rejection of BG tracks even in the 3-sample mode.

 Need to study the tracking performance again once the above improvement is implemented.

Current statement regarding 3/6-mixed sample mode

Still the 3-sample mode is our possible option.

- With the tracking algorithm improvement, the BG rejection in 3-sample mode could be improved.
- Also, if the L1 rate reaches 30kHz with a moderate BG condition (SVD occupancy ~1-2%), we should use the 3-sample mode to reduce the trigger deadtime even without rejecting BG.

Since from rel 7 we are using SVD event T0 as default, we are now studying in SVD what would be the impact of the use of 3 sample data on the event T0 resolution, and also as a function of the threshold to switch to 3 sample (the ECL TC Emax).

Fine triggers for 3-sample mode

ECLTRG

- It changes the requirement of the trigger timing resolution.
 - Small trigger timing jitter is required (less than about 15ns (TBC))
- Modification of the CDCTRG format to replace some of the CDC event T0 information with the CDC ADC information is planned to improves the noise rejection.
 - It degrades the CDC trigger time resolution down to about 25ns.
- If enough fraction of ECLTRG has good timing resolution, possibly we can use only the fine ECLTRG for the 3-sample mode.
 - More than 40% of "fine" triggers are preferable to reduce the deadtime at 30kHz well.
 - Currently, the fraction of the fine ECLTRG is about 30%.
 Current threshold of fine ECLTRG is 200ADC, that can be decreased.
- We requested to prepare DQM/Mirabbele plots
 - Plot of the fraction of fine ECLTRG (w/o HLT filtering)
 - Plot of the ECL maxE distribution
 - to understand the relation between the threshold and fraction of "fine" triggers online, and any changes in the distribution run-by-run.



Input E (ADC)

e26 run#

Y. Unno (43rd B2GM)

Summary

SVD PCIe40

- 5 PCIe40/ROPC are installed. So far, they are running fine.
- Max data rate per PCIe40/ROPC w/o CRC check is about 1000 MB/s
- Need the long-term stability check.

DAQ for VXD commissioning in VXD reinstallation

- Readout PXD/SVD data with scintillator triggers
- We like to occupy the global DAQ for 2-3 weeks (TBD) in summer autumn 2023

3/6-mixed sample mode

- 3-sample data reduce trigger deadtime at a future trigger rate close to 30kHz
- 3/6-mixed sample mode is our option
 - With the tracking algorithm improvement, the BG rejection in 3-sample mode could be improved.
 - Also, if the L1 rate reaches 30kHz with a moderate BG condition (SVD occupancy ~1-2%), we should use the 3-sample mode to reduce the trigger deadtime even without rejecting BG.
- Fine ECLTRG threshold to be adjusted
- Requesting new DQM plots of ECLTRG



Expected data rate of SVD



- SVD online occupancy (= hit occupancy under physics trigger and ZS3) is required to calculate the data rate.
- While future SVD occupancy at the design machine parameter is estimated by the beam background MC scaling with measured data/MC factors, the estimation is under the random trigger and ZS5.

 Corrections for physics/random and ZS3/ZS5 (and electrical noise) are to be applied to estimate the occupancy under physics trigger and ZS3.

Physics trigger occupancy VS. Random trigger occupancy (cont'd)

Occupancy Ratio: Physics trigger (w inj. veto) / Poisson trigger (w/o inj. veto)



• the effect of the injection BG is diluted by a given injection rate and a short BG duration.

 While the ratio is not very stable and sometimes flactuates according to the bad background condition and the injection veto setting, we can reasonably say that it was <u>about 2.0 or</u> <u>less</u> during exp.22

ZS3 occupancy vs. ZS5 occupancy



https://confluence.desy.de/pages/viewpage.action?pageId=238049220