

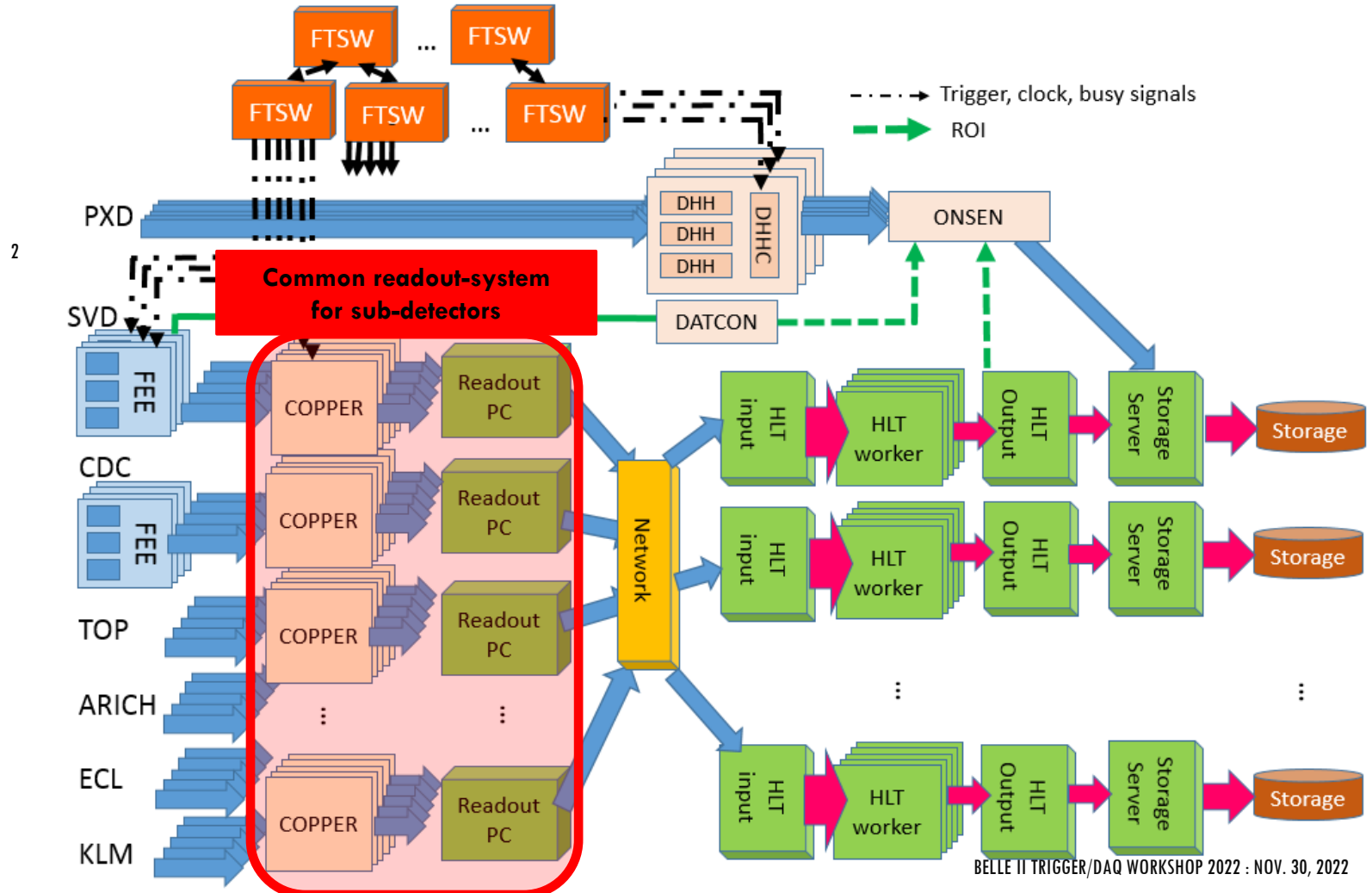


HISTORY OF COPPER BASED READOUT

S. Yamada (KEK)

READOUT SUBSYSTEM IN BELLE II DAQ


- Readout data from FEEs of six sub-detectors
 - Receive data from FEE
 - Formatting, data-checking and partial event-building
 - Send data to event builder(eb1) and HLT



DATA PROCESSING ON COPPER READOUT BOARD

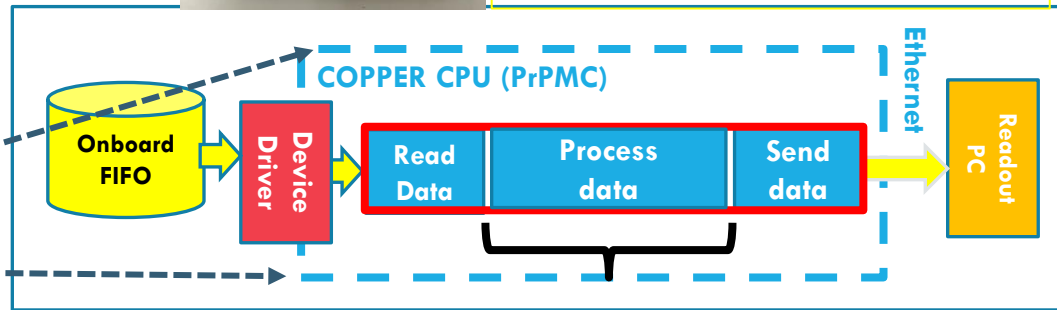
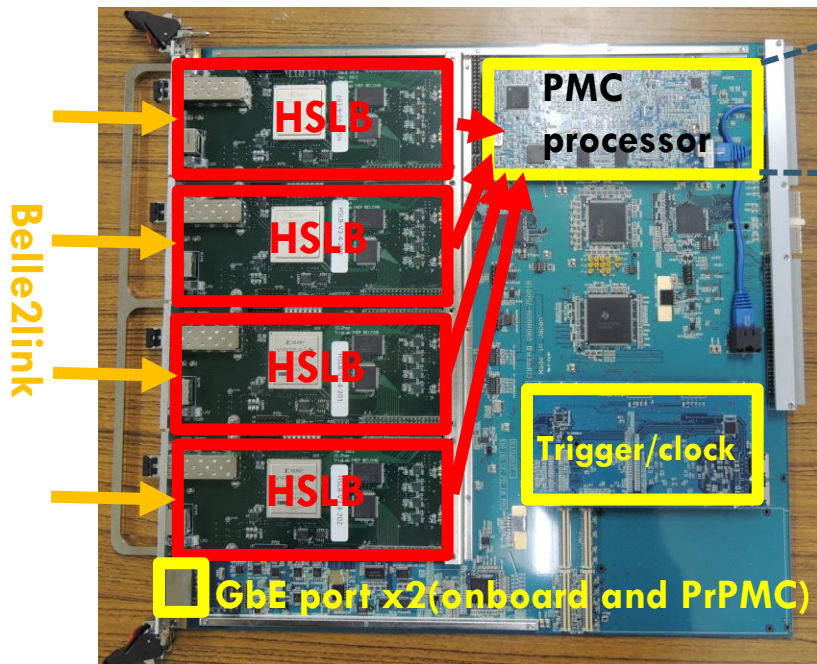
- Readout board : COPPER (COmmon Pipelined. Platform for Electronics Readout)
 - Versatile DAQ board developed at KEK
 - can be equipped with various I/O cards and CPU card
 - HSLB : Data receiver
 - TTRX : communicate with the trigger timing distribution system
 - PrPMC : Data processing

PrPMC on COPPER



- CPU: Intel Atom 1.6GHz Z530P
- DDR2 SDRAM 512MB
- PXE boot from ROPC
- Gigabit Ethernet x1

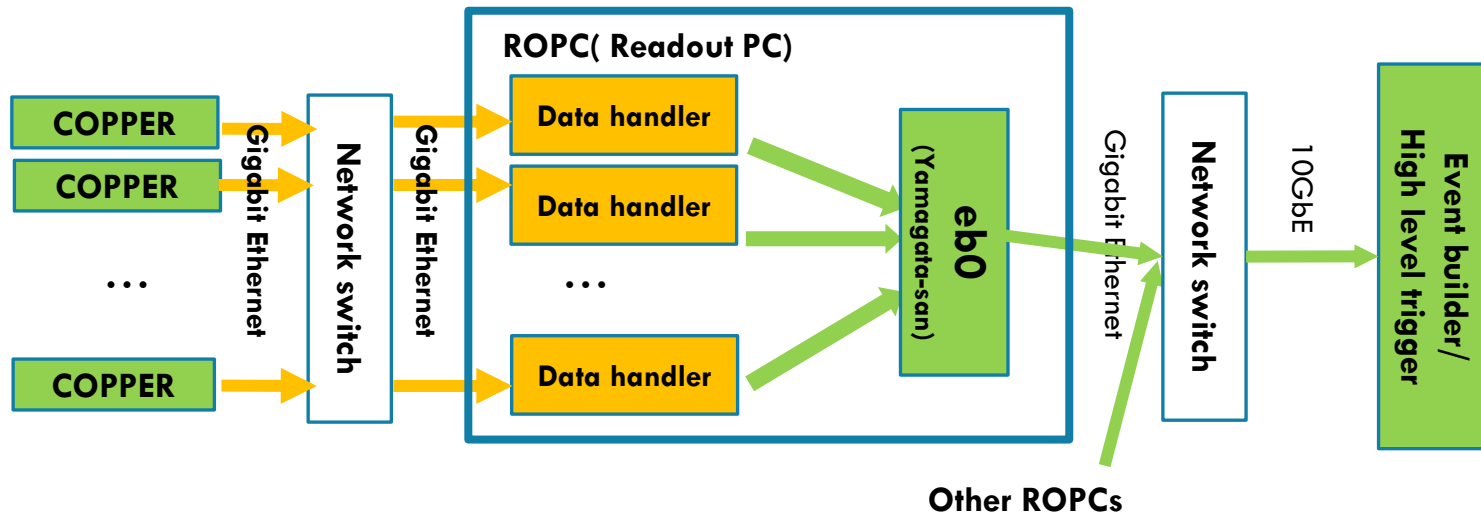
COPPER board



- **Data processing on COPPER CPU**
 - Data formatting (Add header and trailer to raw data)
 - Plain data check
 - Event # incrementation, check magic word etc.
 - Add XOR checksum
 - Report data-flow status to slow control

DATA PROCESSING ON READOUT PC

- Several COPPER boards are connected with a ROPC(readout PC) via Ethernet
- DAQ process for each COPPER data stream is running and doing the following;
 - data check
 - Calculate CRC16 and compare CRC value attached by FEE
 - XOR checksum calculated by software on COPPER
 - Data size reduction
 - merging redundant header/trailer attached by b2link and COPPER
 - Reduction by 15MB/s/ROPC at 30kHz trigger rate(<- 5COPPERs/ROPC, 4HSLB/COPPER)
- Eb0(event builder 0) performs partial event-building and send data to an input node of HLT.



DATA VALIDITY CHECK ON READOUT-SUBSYSTEM

Data corruption after b2link is checked by readout system.

Checksum in data-flow

RawCOPPER XOR

This part is not available in PCIe40 system

Stored in data

COPPER driver XOR

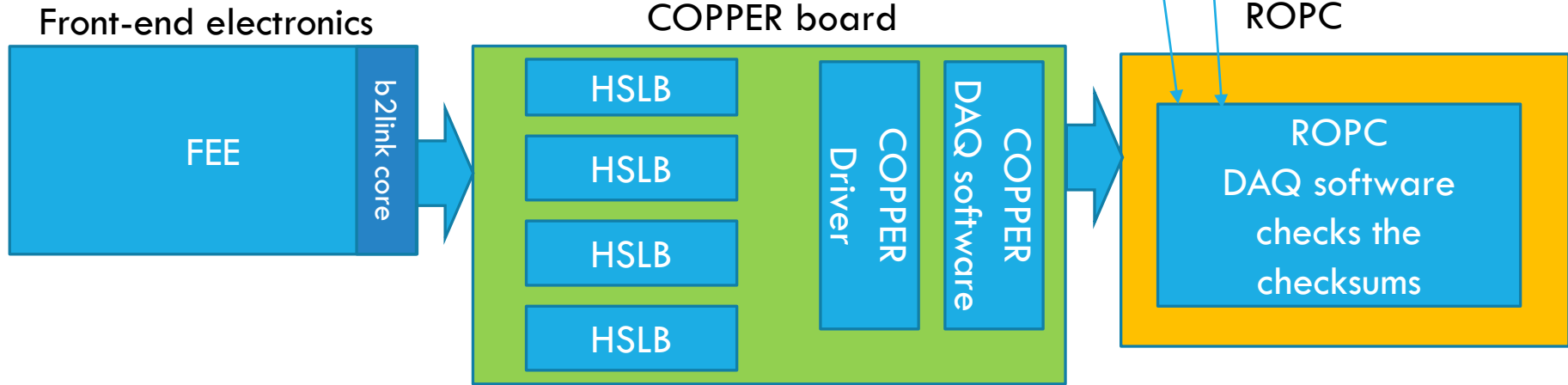
Not stored, because most of COPPER header is removed.

b2link packet CRC
(CRC value per packet)

Error count is stored in data

b2link event CRC
(CRC value per event)

CRC info. is stored in data.



COPPER modules in E-hut

ECL

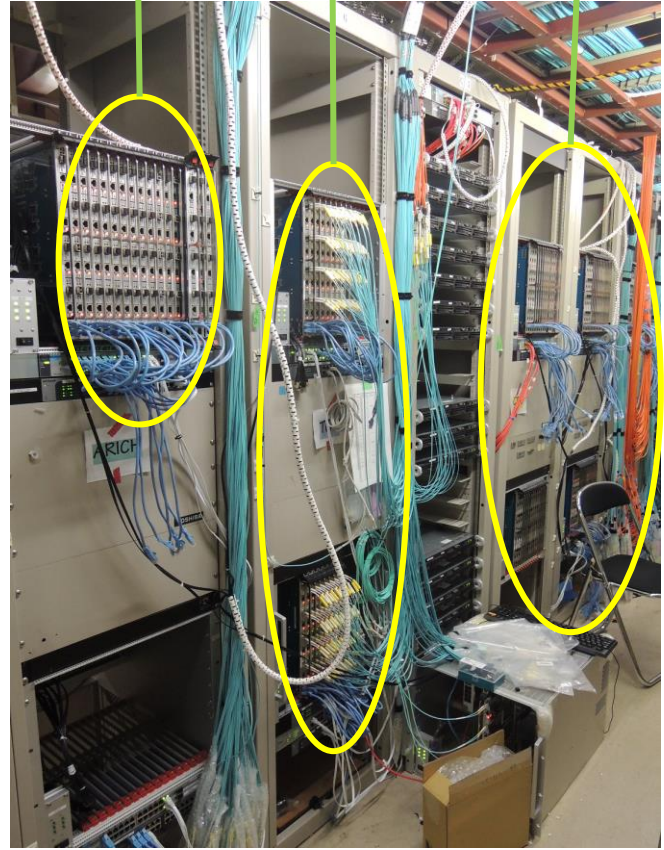
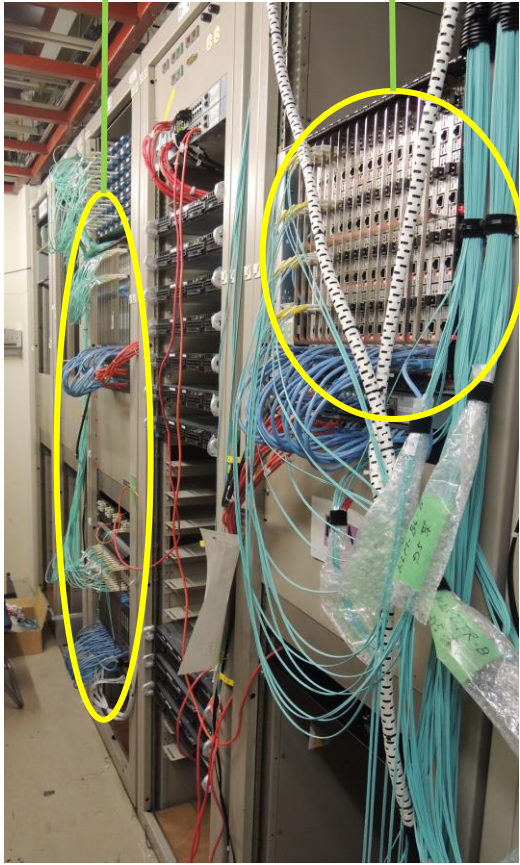
KLM

ARICH

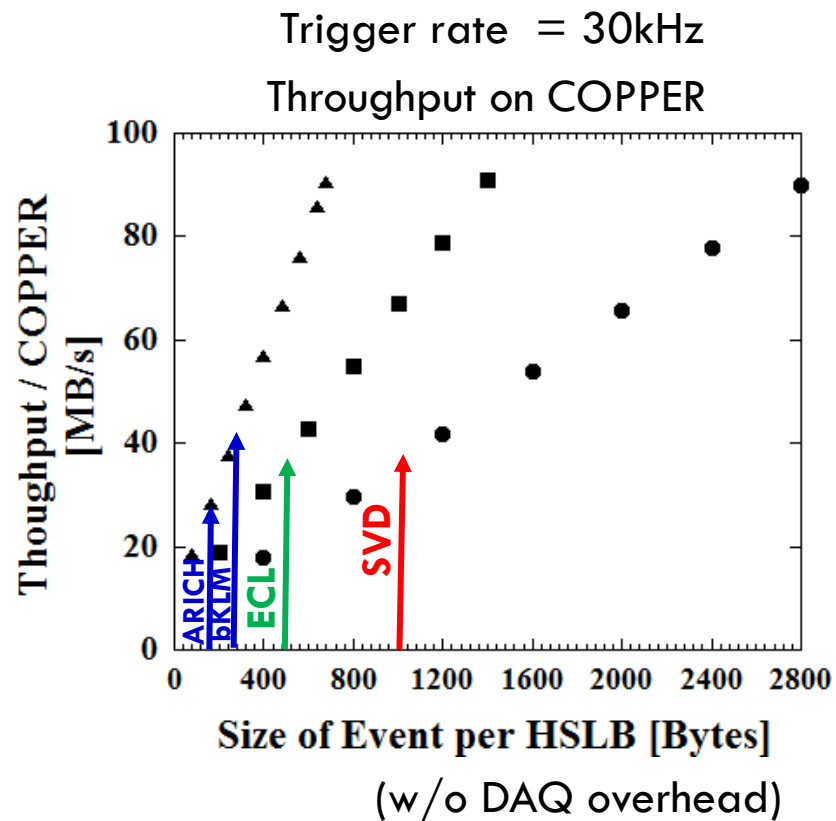
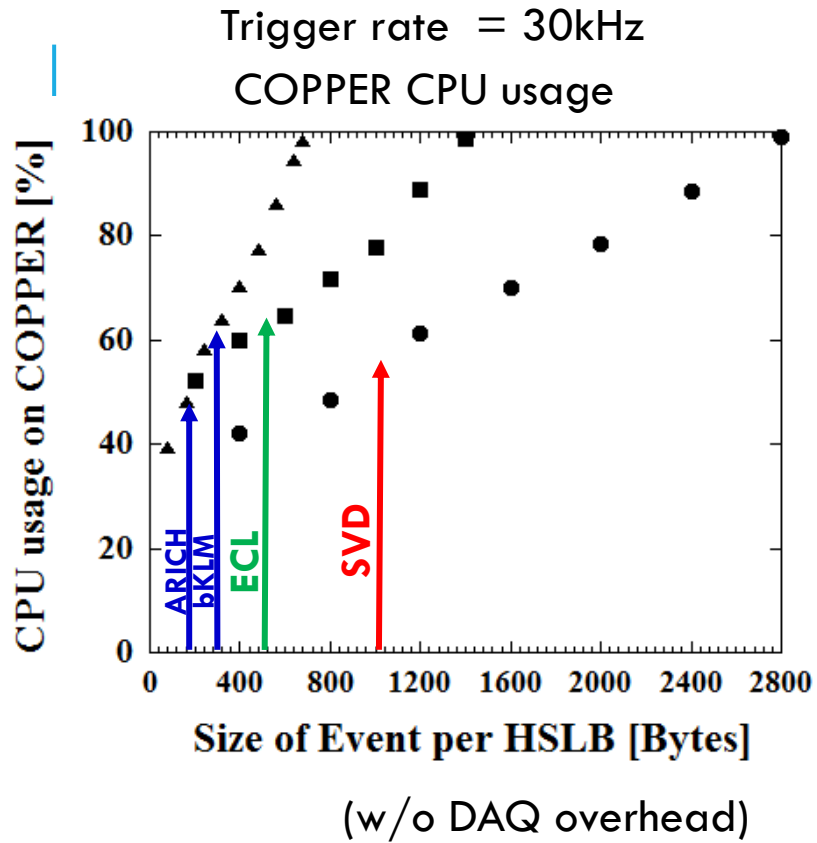
TOP

CDC

SVD



Performance of COPPER readout system

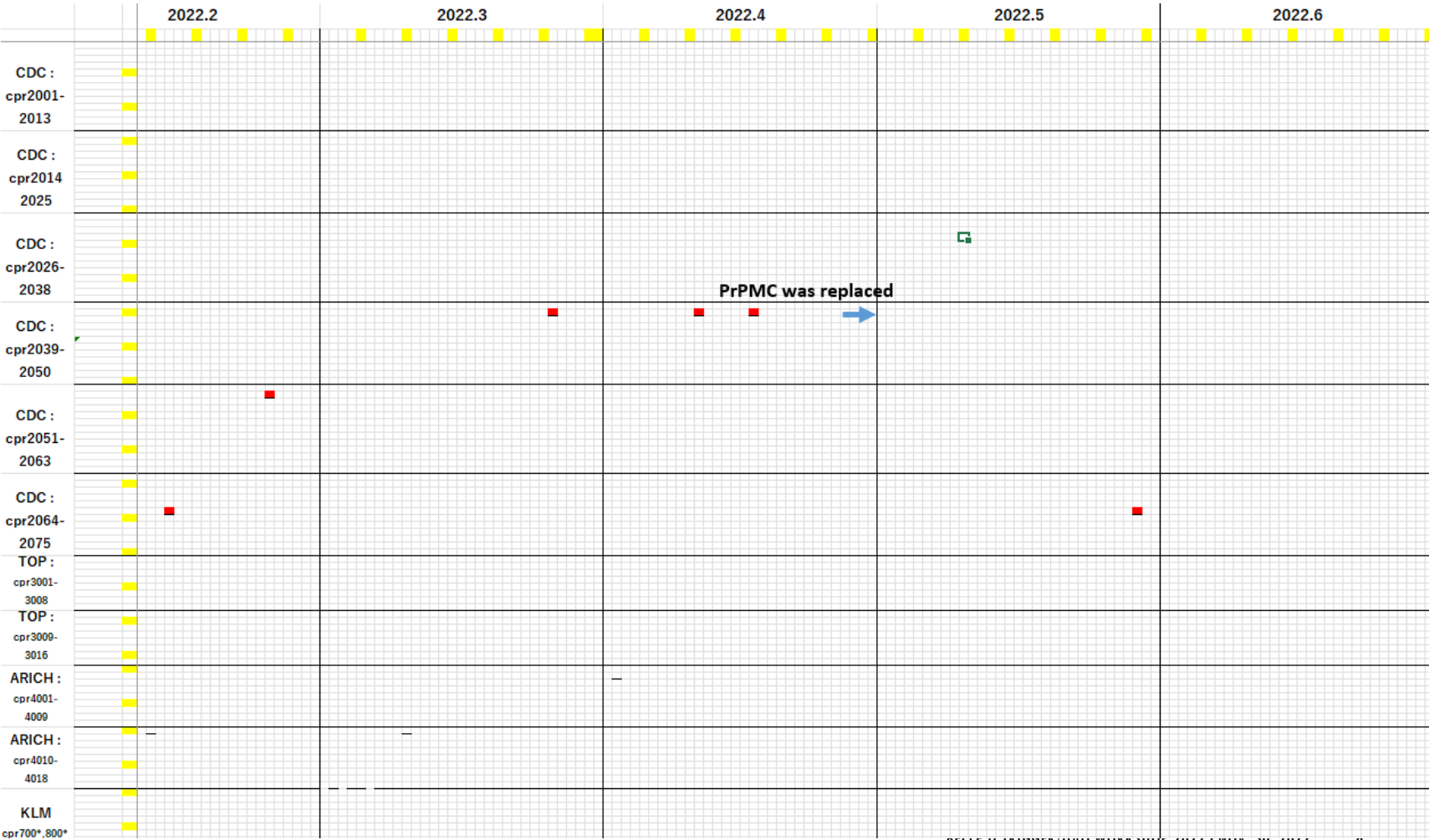


- SVD arrow uses the largest event fragments over 48 FEEs (-> layer3).
- Other sub-detectors arrows uses averaged value over all FEEs.

➤ Actually, the bottleneck is usually the bandwidth from ROPC(GbE) to HLT.

REMAINING TROUBLE : FREEZING COPPER-CPU

- This issue only happens in CDC, TOP, ARICH and KLM.
 - Their COPPER board is equipped with 4 HSLBs
 - SVD : 1 HSLB, ECL and TRG : 2 HSLB
 - So, it might be related with power-consumption ?



HISTORY OF THE COPPER-FREEZING ISSUE

2013 : kernel? -> fixed

- CPU froze when processing high-rate data.
- Fixed by installing light-weight Linux kernel (disable unnecessary options)

2016 : high temperature -> fixed

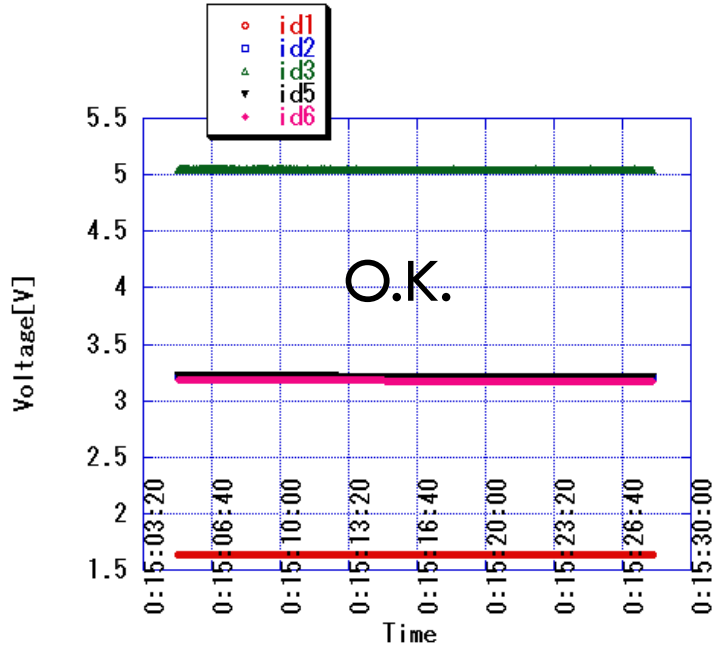
- CPU automatically reboots sometimes.
- CPU temperature rose more than 70degree. Air-flow in racks was changed to cool COPPERs and the problem is gone.

REINFORCING POWER-SUPPLY OF COPPER CRATE

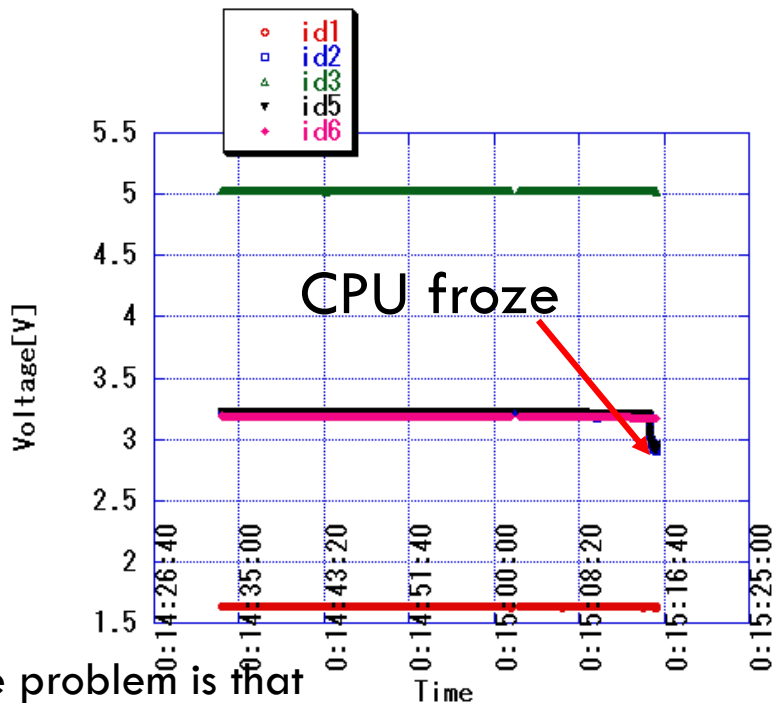
- CPU freezes when the following conditions are fulfilled.
- # of COPPERs in a VME crate is larger than 13. (For some crate, the number is 12.)
 - Each COPPER board is equipped with 4 HSLBs.
 - HSLB firmware is downloaded.

When monitoring the voltage input to a PrPMC, 3.3V becomes unstable after downloading firmware.

of COPPER = 13, 4HSLBs/COPPER



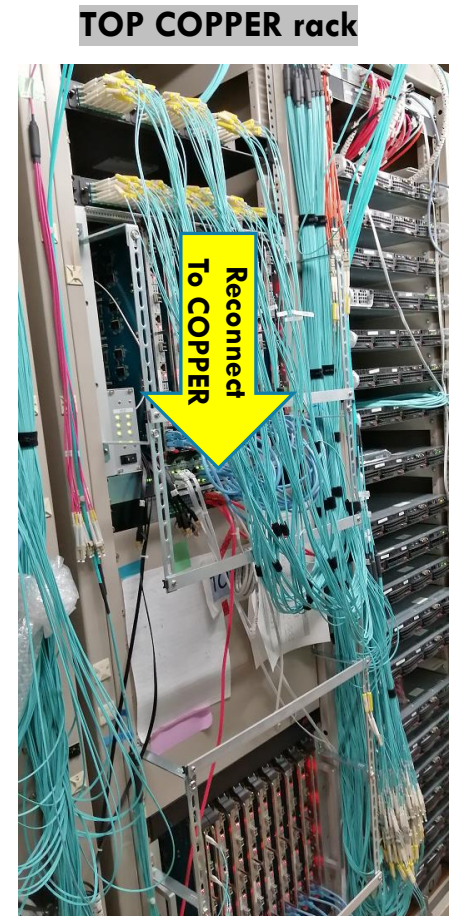
of COPPER = 15, 4HSLBs/COPPER



Even after that, this happens time to time. The problem is that recently the error rate seems to be rising.

COPPER SYSTEM AS BACKUP (1)

- Switching between PCIe40 and COPPER
 - It was frequently done on maintenance days for a readout test of PCIe40 system.
- Procedures
 - Switching fibers on PCIe40 patch panels to COPPER boards
 - Turn off slow-control processes in PCIe40 ROPCs and Turn on SLC in COPPER ROPCs
 - Restart HLT software with COPPER configuration for eb1 rx connection
 - Switch run-control GUI
- Switching during physics run
 - During the 2021c physic run, we rolled back to TOP COPPER system when TOP slow-control error happened.
 - PCIe40 -> COPPER : about 4hours
 - COPPER -> PCIe40 : about 2hours on a maintenance day



COPPER SYSTEM AS BACKUP (2)

- Currently, we keep the COPPER system for every sub-system in E-hut
- COPPER boards : ~ 210
 - HSLB -> spare boards < 10
 - Atom CPU
 - TTRX board

We still have some tens of spare cards except for HSLB.

- COPPER Readout PCs : 43
 - disk troubles : HDD will be replaced in LS1
 - Sep. 27 : svd01
 - Oct. 15 : klm01
- We have not decided how long we will keep the COPPER system as backup.

SUMMARY

- COPPER based readout system has been used for Belle II DAQ since 2018 beam run.
- It has been stably running was not a bottleneck so far.
 - Remaining issue is CPU freezing problem.
- Replacement with PCIe40 based system is ongoing.
 - All readout system except for PXD will be replaced in LS1.
- Keep COPPER system in E-hut as backup
 - maintenance of hardware is needed.
 - It is not decided how long we will keep the system.