



SUMMARY OF DAQ DISCUSSION

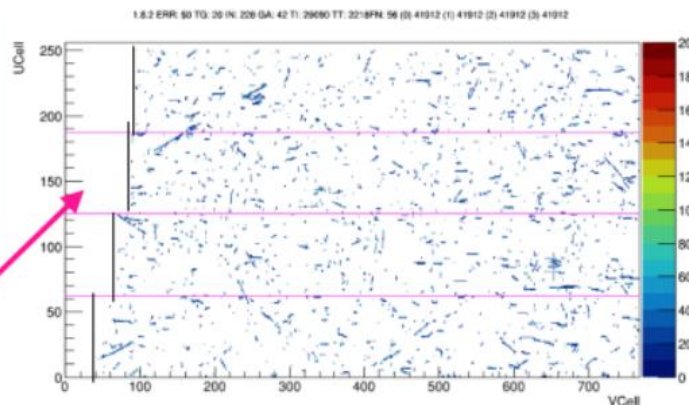
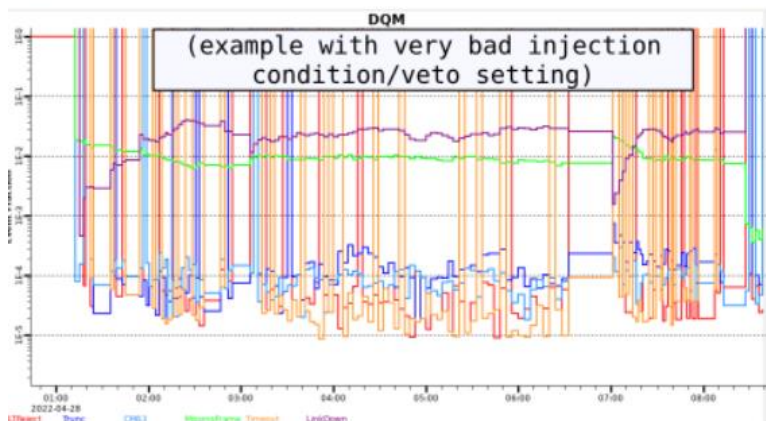
S. Yamad (KEK)

SESSIONS

- Detector sessions
- TTD
- Readout system
- Event-building
- Storage
- ERECO
- HLT
- Storage
- Slow-control
- DCS
- LS2 and future

High Occupany Events

- Close to Injection events can get very “busy”
- Firmware automatically stops event building to avoid link congestion (4%), no DAQ error
 - This affect fraction of PXD data, mostly inner +X modules)
- Small fraction of events affected (and often events where SVD/CDC is not useful, too)



- More tricky: when several of these events are triggered close-by, DHP fifo/link will get full and framing gets out of sync. This may affect several events until it is back in sync.
- This happens often after injection when many triggers come in a short time interval due to background → full veto adjustment helped
- Todo: Firmware to suppress readout-trigger when occupancy gets too high (“internal veto”)
- **Gated Mode will/can not be used**. Several tests in 2019-2021, see large negative impact on data quality (noise, efficiency)

- PXD ROI data-reduction has not been turned on yet.
 - When to turn on it is the matter to be discussed widely in Belle II collaboration.

Summary

■ SVD PCIe40

- 5 PCIe40/ROPC are installed. So far, they are running fine.
- Max data rate per PCIe40/ROPC w/o CRC check is about 1000 MB/s
- Need the long-term stability check.

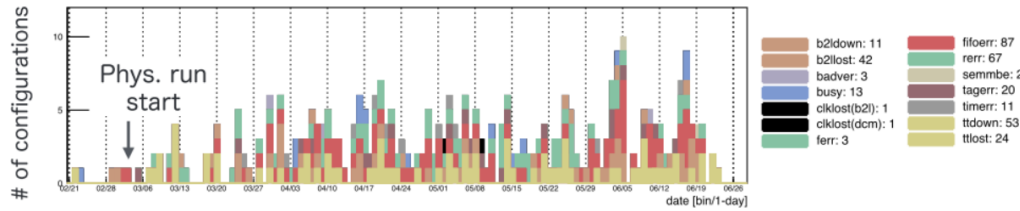
■ DAQ for VXD commissioning in VXD reinstallation

- Readout PXD/SVD data with scintillator triggers
- We like to occupy the global DAQ for 2-3 weeks (TBD) in summer – autumn 2023

■ 3/6-mixed sample mode

- 3-sample data reduce trigger deadtime at a future trigger rate close to 30kHz
- 3/6-mixed sample mode is our option
 - With the tracking algorithm improvement, the BG rejection in 3-sample mode could be improved.
 - Also, if the L1 rate reaches 30kHz with a moderate BG condition (SVD occupancy ~1-2%), we should use the 3-sample mode to reduce the trigger deadtime even without rejecting BG.
- Fine ECLTRG threshold to be adjusted
- Requesting new DQM plots of ECLTRG

3 sample mode with smaller event is still attractive also for online DAQ side.



Idea for DAQ down-time mitigation

- ◆ Keep DAQ running after an error is detected.
 - Re-configure problematic CDC FEs when we stop DAQ for other reasons
 - This is the same as handling unpacker errors
- ◆ Matter of concern: soft errors can break the data structure??
 - We consider whether COPPER can remove the event data from a problematic FEs. (online masking scheme)
 - COPPER processes only the header while adding error/mask flags.

Note :
 If no data from an FEE
 ->
 Just persistent BUSY

We would like to discuss this w/ S.Yamada later.



- ◆ It's implemented but not working... no guard against neutrons, so far
 - SEU-Controller initialization is not finished, and detection and correction process don't start
 - When FPGA is configured by using Xilinx application (iMPACT), SEU Controller works fine.
 - FTSW is likely not correctly mimicking JTAG signals
 → H. Sudo starts debugging soon.

- To mitigate error in SCROD for noisy events, some computation is being considered to be moved to PCIe40 ROPCs.

Planned improvements during LS-1

18

- ▶ Hardware replacements (Inami, Bessner)
- ▶ Migration of TOP Pedestal subtraction and Feature extraction from TOP FEE (currently done in SCROD PS) to TOP ROPCs (Kohani)
- ▶ Saving TOP Pedestals in top db and retrieving these values during LOAD operation for online pedestal subtraction (Purwar)
 - ▶ Acquiring TOP pedestals **in parallel** for all TOP frontends using PCIe40 – May need minor modifications in pcie40_regconfig command (need to be able to write multiple registers for different channels at the same time)
- ▶ Improvements in Automated recovery scripts – provide a TOP recovery GUI to CR shifters (Bessner)
- ▶ Auto masking on known error and auto unmask board stacks after recovery/power-cycle on the next beam stop (Bessner, Purwar)

Harsh Purwar, HEPG, UHM, Honolulu, HI, USA
Nov. 29th, 2022

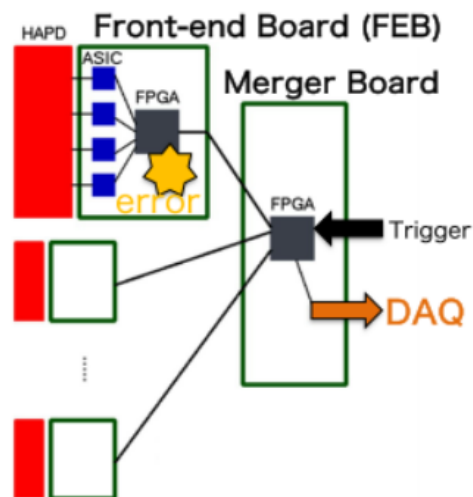
Question to DAQ team

(Yu Nakazawa-san already mentioned)

We'd like to also keep DAQ after detecting an error

- Reconfigure problematic FEEs when DAQ stops for other reason
- If it is possible, we can reduce DAQ crash due to ARICH error

Need to update merger firmware



Your comments are welcome

2022/11/29

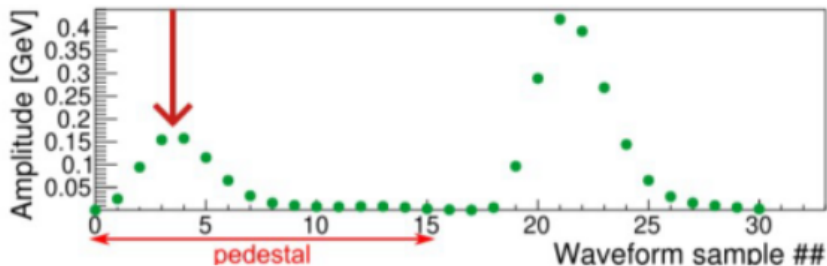
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No effect as long as Merge board keep communication with PCIe40 and FTSW.
 - If Merger does not send data while the recovery procedure, deadtime due to BUSY could happen but DAQ is not crashed.

Handling increased size of waveform data

As was reported in [TB meeting on 2022.11.18](#), injection background causes data loss in ECL due to underestimation of the hit amplitude.

• Higher pedestal → lower amplitude → more hits below the 1 MeV threshold are discarded.



This can be fixed in several ways, best energy resolution is achieved if we **save waveform data** with bad pedestal for offline re-processing at the ECL unpacking stage.

Estimation of data-rate increase will be provided by ECL experts to DAQ group

Firmware Performance

- ☺ 8 ns timestamping of L0 triggers allows for shrinking ROI to 24 ns (in order to capture leading-edge time and peak value)
- ☺ The ROI is contained in 1 TARGETX storage window 50% of the time
- ☺ The Wilkinson ramp takes 8 us per window
- ☺ Shifting takes an additional 13 us (for all 24 samples)
- ☺ Total time per event 21 to 29 us (for 1 to 2 windows respectively)



- ☺ Primary limitation is too many new L1 triggers during digitization
 - ☺ Protections in place so that we can give up on digitization and revert to "simple" mode for a few events in order to catch up, but if occupancy is too high on any given FEE, the digitization queue may fill up before this can happen

Quick recovery GUI or something, so that KLM expert shifter can quickly recover from b2llost from dc38 for example, is preferable.

Trigger and Timing Distribution system

Firmware overhaul project

● Initial motivation

- To implement multiple FTSW modules into one large FPGA for FTSW4 for resource evaluation
- At least, some restructuring was necessary

● Structured data type

- For some unknown reason, I was not using the VHDL's structured data type
- Packing signals into a **"record"** type solves many problems

● Restructuring the component tree

- Time to rethink about modularizing the code according to the functions

● Plan

- Hopefully finish coding before Christmas
- A few more weeks of work to generate all variants from a single set of source files
- Output timing adjustment (ttlost mitigation)
- Hopefully test at E-hut in Jan-Feb
- Convert this talk into a document file
- **Then release it as version 1.00** (latest ft3m is version 0.91)

● Wish

- Code reviewing by a student

So that other people can understand the system in more detail...

FTSW4 development

● Solution to the CAT7 problem

- Up to ~100mV noise on inter-crate CAT7 cables ($\leq 1\text{m}$ CAT7 is still fine)
- No further improvement is expected, b2t over fiber would be a solution

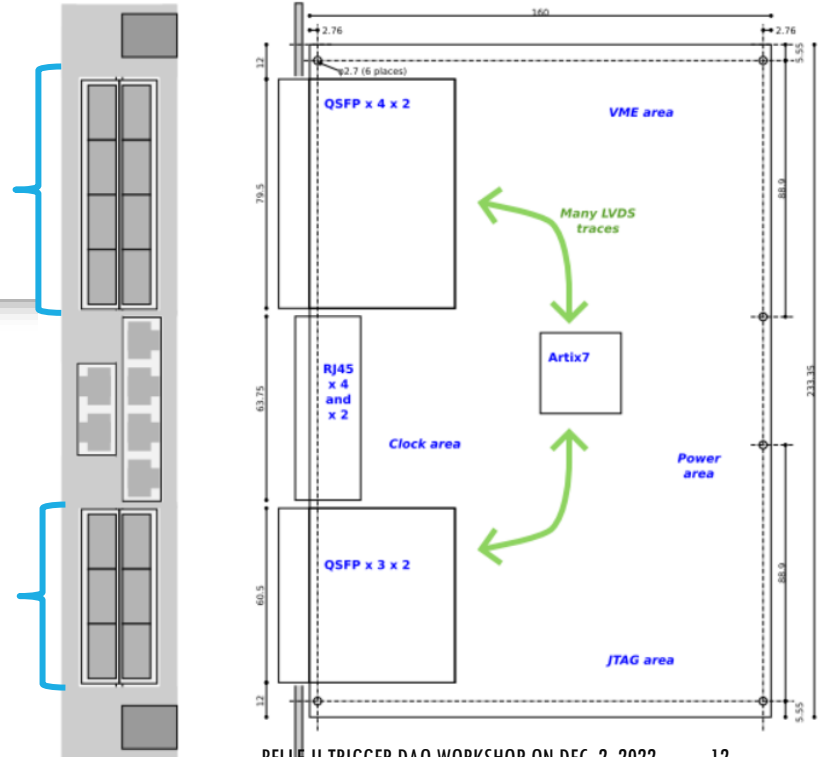
● FTSW4

- Next generation FTSW with fully optical inter-rack connections
- Compatible with FTSW3 for short CAT7 connections
- Cost effective solution with low-end FPGA with maximal I/O

● Outline of this talk

- Motivation
- Part selection progress
- Board layout plan
- Use case for CDC FEE upgrade

Mass production :
 (Next next Fiscal year)
 Budget is needed for this.



non-stop DAQ

Steps towards non-stop DAQ

Quick(auto)
initialization
of faulty FEE

Auto-SALS

Partial-SALS

Auto start
with next subrun
(just reset)

Auto start
with next subrun
(corrupted Data
Error in ROPC)

masking,
,auto-recovery,
Auto unmasking

Wish

(M. Nakao)

● FEE error recovery without SALS

- **Same** run number, **increment** sub run number, event number just **kept incrementing**
- Original DAQ plan included such a wish
- DAQ system has been too complex and unreliable to work on it
- Now, this workshop is a chance to revisit (similar wishes also in subdetector talks)

● What can be actually done

- Recovery from ttlost / b2llost may be realized in a **O(1sec)** time scale
- Recovery from other FEE errors demands reprogramming and would take longer time of **O(1min)**
- Use **PAUSED** state like HV recovery — still some gain against full SALS

● What have to be involved

- **TTD** is the main player
- FEE errors are also detected as corrupt data at **readout PC**
- Therefore, the recovery sequence has to be handled by an upper level — **RUNCONTROL?**
- And **FEE** should be able to start from a non-zero event number

COPPER system

COPPER SYSTEM AS BACKUP (2)

- Currently, we keep the COPPER system for every sub-system in E-hut
- COPPER boards : ~210
 - HSLB -> spare boards < 10
 - Atom CPU
 - TTRX board

We still have some tens of spare cards except for HSLB.

- COPPER Readout PCs : 43
 - disk troubles : HDD will be replaced in LS1
 - Sep. 27 : svd01
 - Oct. 15 : klm01
- We have not decided how long we will keep the COPPER system as backup.

- Maintenance for faulty hardware
- OS for readout PCs : CentOS7
 - Keep COPPER ROPCs off when they are not used ? (save electricity, security)
 - Reduce # of ROPCs and connect them to all COPPER boards via switch ?

● SL7 or CentOS7

- Most of the PCs in daqnet is operated either on SL7 or CentOS7 now
- **EOL 2024 June 30, only ~1.5 years from now**

PCle40 system

REPLACEMENT OF SVD, CDC, ECL AND TRG READOUT SYSTEM IN LSI



➤ Slow-control library and local run GUI for each sub-detector has been developed.
-> Now commissioning is ongoing.

TRIGGER DAQ WORKSHOP : NOV. 30, 2022 3

To SVD, CDC, ECL and TRG experts,

If detector experts has their own scripts to configure/monitor FEEs via COPPER, please rewrite them with new commands.

New SLC Commands

(H. Purwar)

PCIe40 equivalents

▶ The basic register read/write function now has a different syntax:

```
reghs -[a...d] fee32 [addr] [value] → pcie40_regconfig --ch [0...47] --fee32 -r/w [addr] [value]
```

- Additional labels for maskdb:
 - Every time we do "Save & Apply Mask", a new maskdb will be created.
maskdbtrg:pcie40:XX
 - TRG people want to have a "label" for maskdb:
maskdbtrg:**physics**:pcie40:XX
maskdbtrg:**highrate**:pcie40:XX
maskdbtrg:**test**:pcie40:XX
such that they can select different configuration to save or load.

```
[b2trg@rtrg1 ~]$ daqdblist maskdb maskdbtrg:pcie40
```

id	table	name	date
1423	maskdb_2022	maskdbtrg:pcie40:58	23/06 12:22:58
1422	maskdb_2022	maskdbtrg:pcie40:57	23/06 12:06:49
1421	maskdb_2022	maskdbtrg:pcie40:56	23/06 11:51:49



Qidong-san took over TRG PCIe40 upgrade liaison from YunTsung and will work for this with H. Nakazawa-san.

COMMISSIONING STATUS

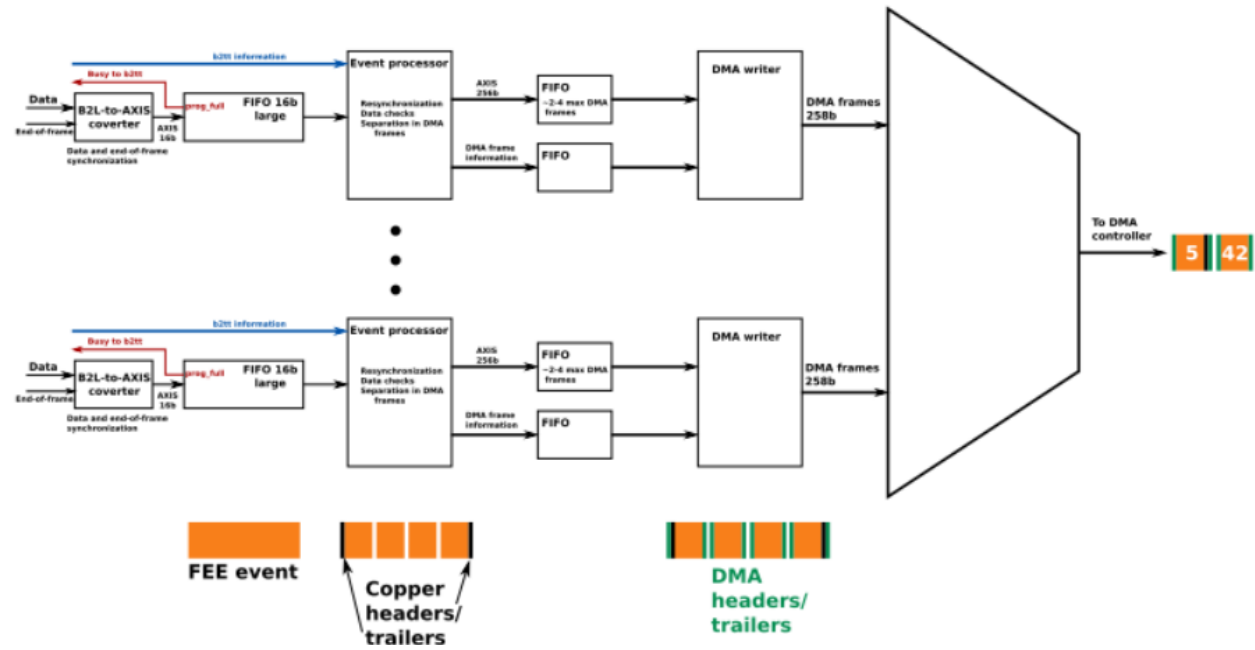
- Readout systems for SVD, CDC, ECL and TRG are replaced in LS1.
 - Basic readout test was done.
 - High-occupancy or large event-size readout test is ongoing or planned.
- Some issues were reported in LS1
 - Persistent BUSY -> Fixed
 - Empty FIFO issue -> Tested after modification
 - Fake error -> will be investigated.

Using server memory instead of FPGA on-chip memory for event-building

tolerable for

- Large event-size
- Large latency from FEE

➤ PCIe40 firmware block diagram for software assisted event-building



- ▶ Performance of the system measured and bottlenecks identified
 - ▶ 2.4 GB/s sustained data rate **with** CRC calculation
 - ▶ 4 GB/s sustained data rate **without** CRC calculation

Note : This is the test result at test bench. Need to be checked in global Belle II DAQ.

Current status on “doublepci”

- There is a stable “doublepci” firmware.

quartus21	master	48 links	v15.4 (sof.LAL, sof.KEK, pof.KEK)	New DMA, user logic and b2tt. Soft CDR for b2tt, fixes for PCIe stability. To be used for development.	v9.5	exp26 run33 (top, arich, klm); deployed during the maintenance day of May 11, 2022 exp26 run250(arich,klm), exp26 run254(top): bellell_KEK_v15.4_36ch.sof
doublepci	master	48 links	v17.0 (sof.LAL, sof.KEK, pof.KEK)	First version with double pci interface. To be used for tests only.	v9.5	

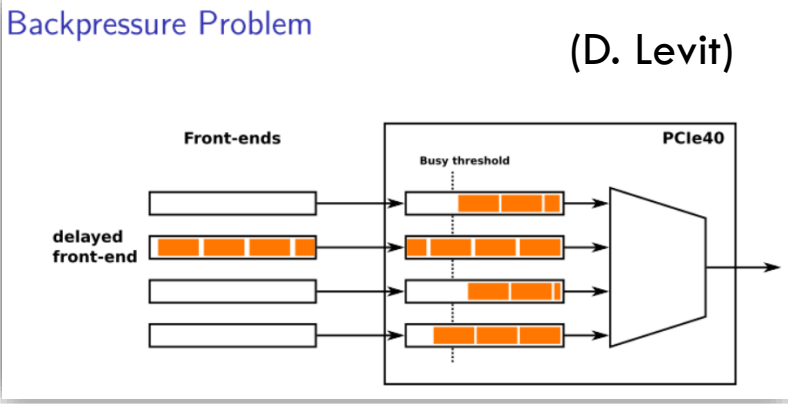
- The firmware has already passed few tests, including slow control test and data readout test, in the IJC lab.
- It is now being tested with the KEK b2ropc.

Plan on Optical b2tt

- Use fibers for PCIe40-FTSW connection instead of LAN cable
- The FTSW upgrade is also necessary.
- I’m joining for modifying and testing the firmware.

Belle2link upgrade

- Backpressure from PCIe40 to FEE
 - FEE can receive BUSY signal from PCIe40 and restrain sending data



- Auto-reset (auto-reconnect) function

- The design of the auto-reset function:
 - Define a link up flag to check the link's hardware status.
 - Issue reset while observing any instability.
 - Repeat it until link is stable.

(YT. Lai)

- Upgrade of Belle2link protocol
 - Could increase max. data rate per one belle2link !

Bypass Idle States and CRC

Uninterrupted Data Flow

(D. Levit)



- ▶ Remove IDLE states and CRC words



- ▶ Transmit full data Uninterrupted
- ▶ Maximum efficiency goes to 100% for long frames

Comprehensive DAQ upgrade paper

Manuscript title?

To be decided...

Few suggestions...

- **Upgrade & performance evaluation of the Belle II DAQ for high-luminosity operation of SuperKEKB**
- Performance evaluation of the upgraded Belle II DAQ
- Commissioning of upgraded Belle II DAQ system: PCIe 3.0-based readout
- ...

Request to all worker bees:

- Please start writing/dumping figures, notes, etc. in your free time.
 - If you put a figure that has already been included in some publication, please do add a reference in figure caption.
- Our target should be to wrap it up, before LS1 ends, at the least have a first draft ready for Queen bees to review.
- Also, please do let me know if you can't access the manuscript on overleaf, I can resend the overleaf invite. The first invite was sent weeks ago!

Event-building

- Various updates were made in LS1 for event-building software
 - Merge eb0+eb1tx
 - Introducing ZeroMQ in readout software
 - More ZeroMQ in new event-building scheme

Moving to PCIe40

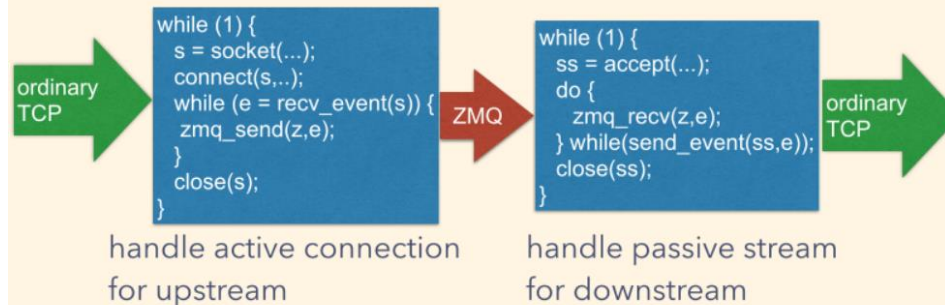
- eb0 is not needed any more.
- eb1tx must be rewritten to read 5 TCPs cyclically.
- rewritten again for throughput faster than 10Gbps
 - removing thread interlock by inproc ZMQ
- rewritten again for new PCIe40 reader by Dmytro-san, which sends data via ZMQ

Partial SALS

- To reduce the DAQ dead time caused by SALS
- keep components READY except ABORTed component
- event builder components dies when the peer process dies.
- The process connected to event builder also die.
- single des_ser death → single eb1tx death → all eb1rx death → all HLT death & all eb1tx death → all des_ser death

Tentative agent to keep connection

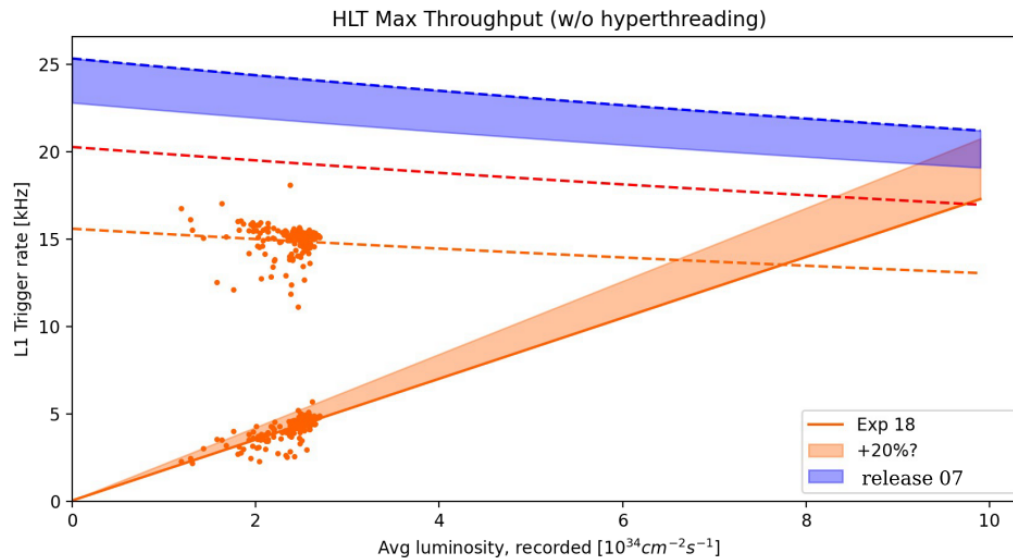
- only applicable to single TCP



May drop event on a reconnection

- Need to avoid death of eb1rx in HLT server, if we want to keep HLT READY when partial SALS.
 - Mechanism to keeping eb1rx alive was considered.
- Hopefully, we can keep the current SLC nodes by making
 - Eb1rx : alive and try to reconnect to eb1tx
 - Inclusion/exclusion of sub-detector needs full SALS
 - Eb1tx : aborted when partial SALS

HLT

with 13 units + release 07

following conditions of exp 18 \rightarrow can operate until 20 kHz
(corresponding to $9 \times 10^{34} / \text{cm}^2 / \text{s}$)

- Optimization during data taking (release-05) allowed us to survive until LS1 (13 kHz)
- with 3 HLT units more + release-08 (event time+ track fitting improvements)
 \Rightarrow should be able to reach 20 kHz (Luminosity $\sim 10^{35} / \text{cm}^2 / \text{s}$)
- need to carefully monitor tracking performance at higher luminosity
- need to make sure software development keeps CPU budget under control
- no clear path beyond 20 kHz... unless significant improvements in pattern recognition

Addition of 3 HLT/STORE units in LS1

- 18 new HLT workers + 2 sets of HLT control/STORE units are already in hand.
- 15 (or more) servers + 1 more set of HLT control and STORE units will be purchased by the end of FY2022.

=> 1.5 units will be built in autumn (Oct.-)
1.5 unit will be added in Jan.-Mar (2023)
-> In total : 13 HLT units; 6400 cores.

(one of them = HLT13 will be used as a test bench as before until it is really needed to process high rate)

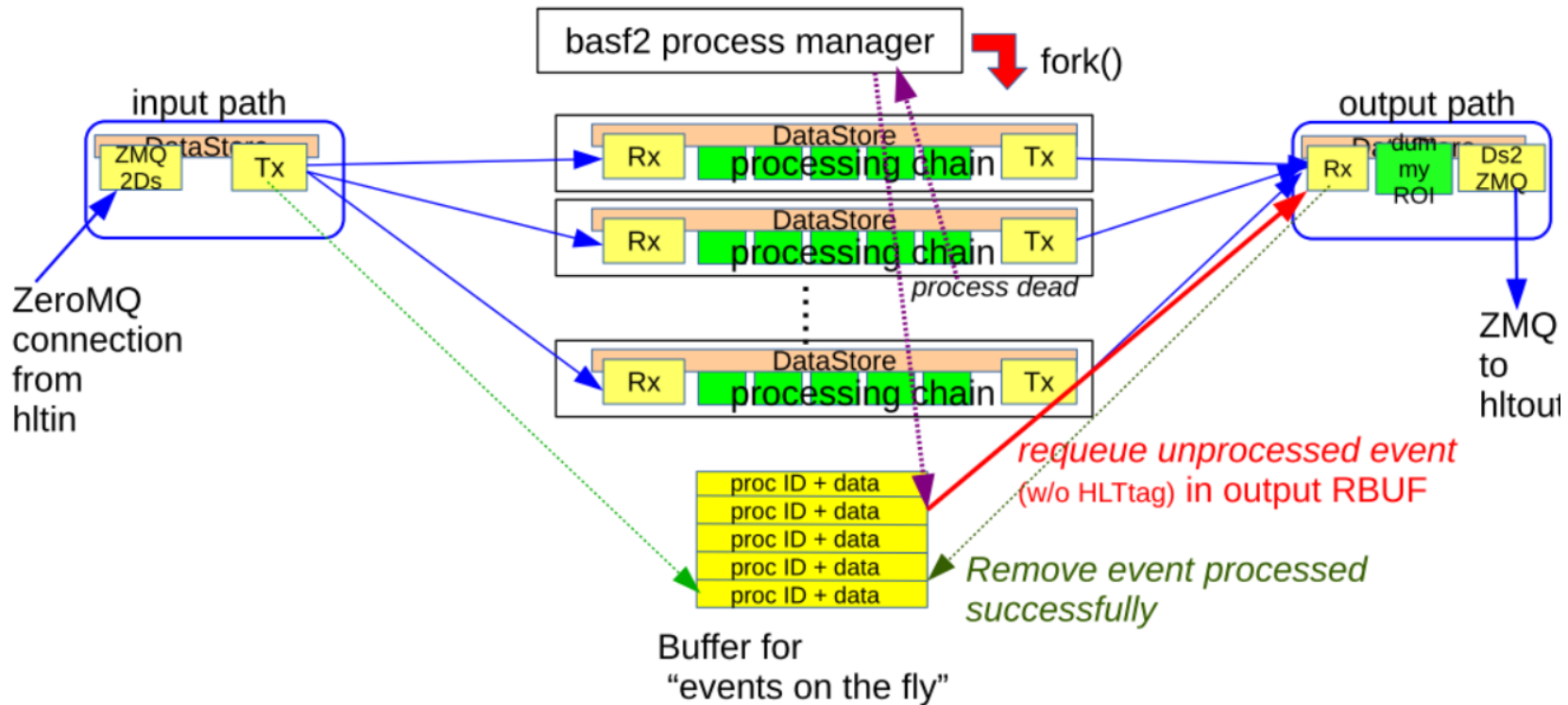
 **Expected performance : up 20 kHz from 2023c run!**

Note: HLT operation during summer was limited (up to 5 units) to save the power consumption.

- Deployment of HLT processing software is managed by Seokhee.
- “Online” version of Belle2 library is released by Giacomo every two weeks together with the update of database (online global tag).
- Whenever a new version is released,
 - * Giacomo test it offline using the recorded raw data.
 - * Seokhee updates cvmfs and database on the maintenance day.

- Issues were
 - * When seg-fault occurs, the worker process is not recovered and the processing power drops and the event is lost.
 - * The test of library with massive raw data is not done because hbasf2 parallel processing cannot run offline.

Improved “basf2” data flow on a worker



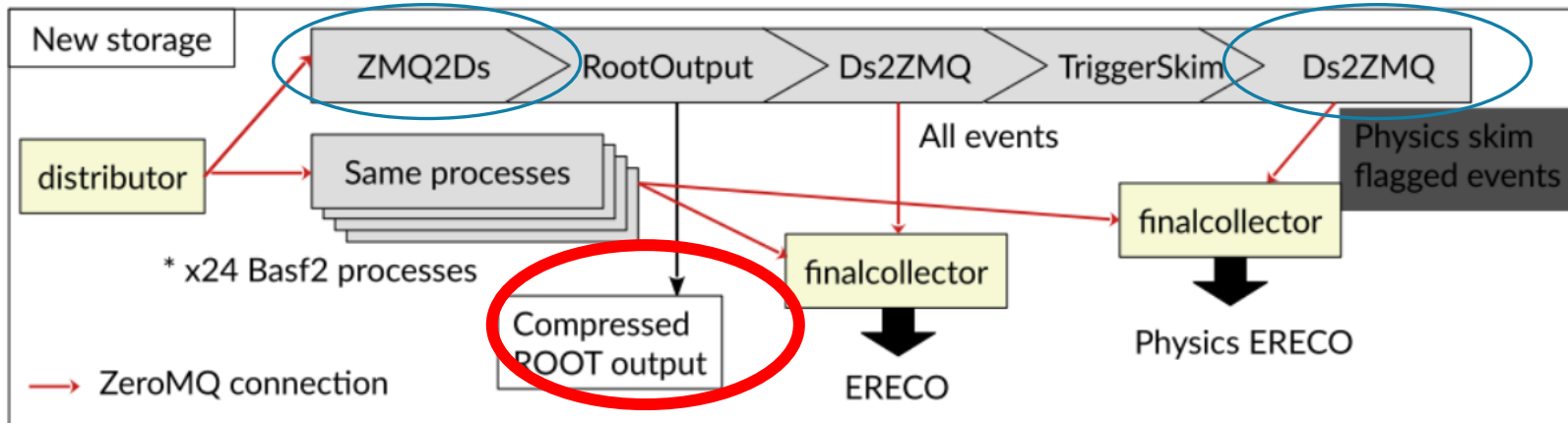
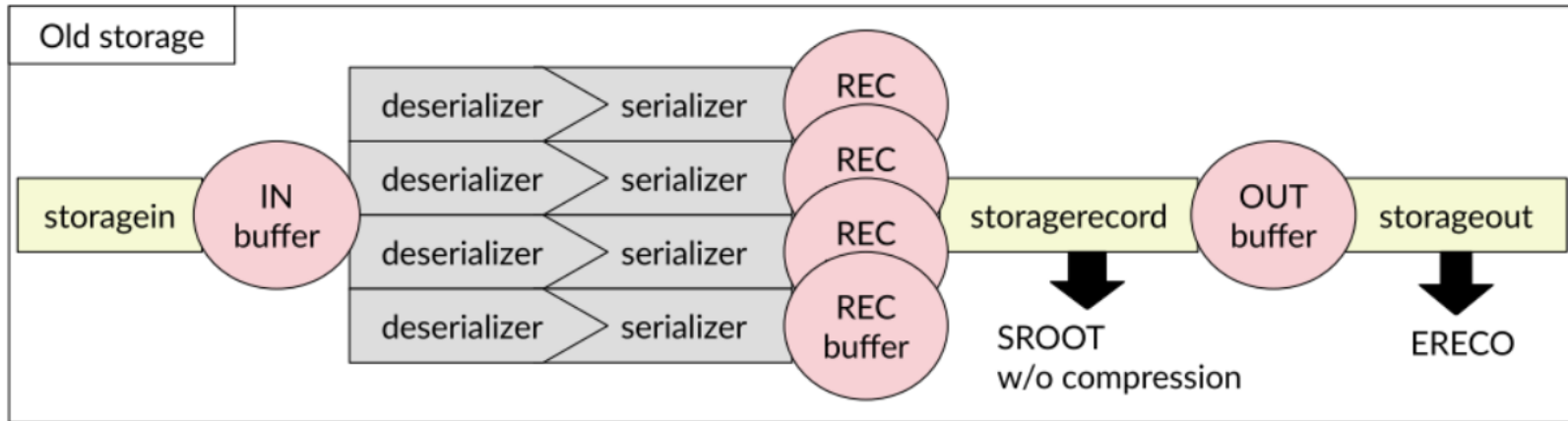
- Plan: complete the development by the end of this year and submit a PR to merge mods in Belle2 library/daq_slc.
=> Test in GCR/HRT from early next year.

Storage

Upgrade of storage (Direct ROOT recording) is ongoing...

Introduction

(SH. Park)



■ System resource usage of the test environment

- ▶ CPU usage per BASF2 process: ~80% (top result)
- ▶ Total (all 3 RAID) disk writing: 150 MB/s → 50 MB/s per RAID

■ 3 kHz physics run estimation using exp26 run1968

- ▶ 22,089,949 evt / 1976s = 11,230 Hz
- ▶ Total output file size after ROOT conversion: 303 GB
- ▶ 3 kHz physics run writes output file with 41 MB/s → 14 MB/s per RAID

■ Our test environment is more tough than the final goal

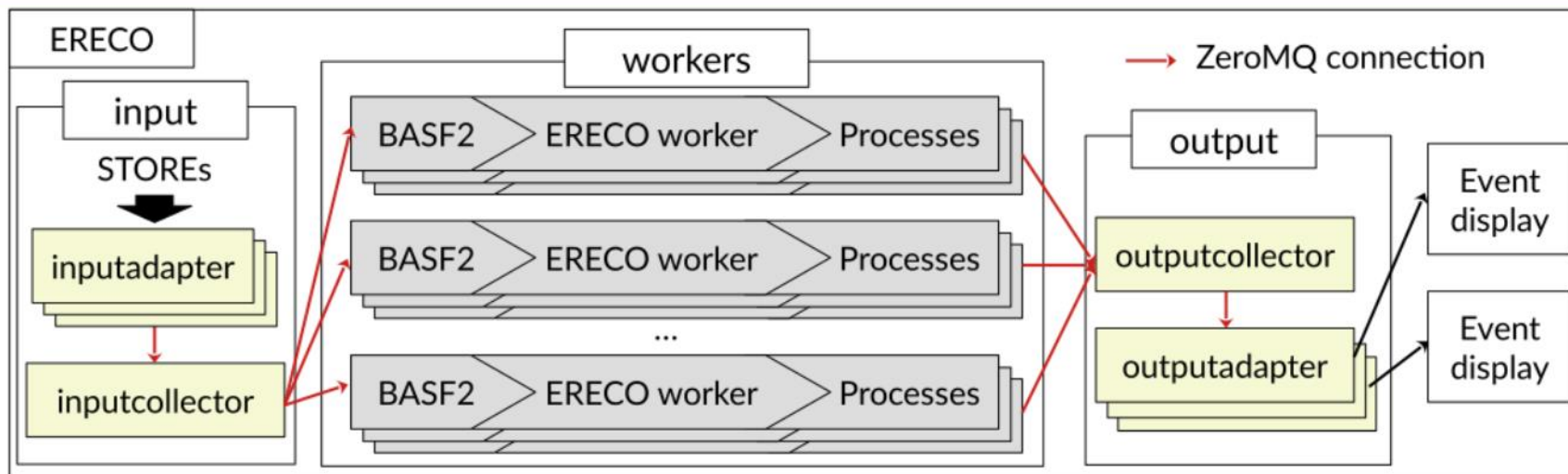
■ Results

- ▶ 17 hours run creates 9 TB root output files into the storage without any issue
- ▶ Simultaneously, b2file-merge and file copying was tested
 - No performance degradation found = No output rate drop and event loss
- ▶ However, sometimes (or frequently), run goes to ERROR right after the events are reaching to the storage
 - SALS makes next run work
 - This was not happened in the test bench, so I don't have any idea for now

Basic implementation for HLT01-05 will be finished this year.

-> Commissioning with detector system will be done when they become available.

ERECO



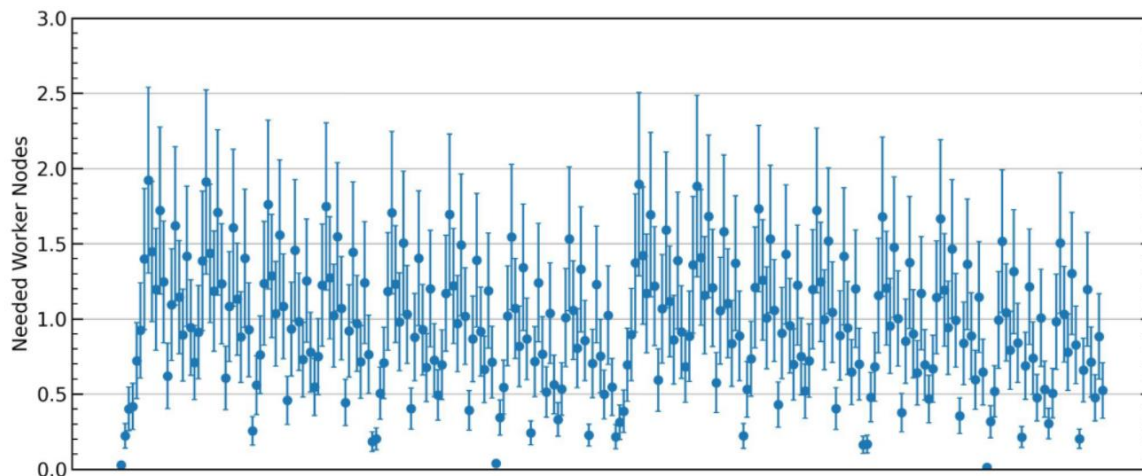
■ Two goals of new ERECO

- ▶ More stable operation with ZeroMQ
- ▶ With an additional ERECO, keep more DQM statistics of physics-flagged events
 - The events are selected by the TriggerSkim module in STORE

- Investigated 8 different trigger lines and any possible combination of them
- Depending on the chosen trigger line we can estimate the worker nodes needed in order to deal with the expected rate
- We ran a few checks to verify that the script is producing the correct results

- We could test additional trigger lines
- We will start using the `accept_dstar1` trigger line and allocate one worker node at a global run
- Preparation of first results to see if findings of this study are also valid in the experiment
- If successful:
 - Add additional trigger lines
 - Start looking at variables we could use for monitoring

Needed Worker Nodes for the Combinations



For any given combination we stay below 3 worker nodes (if standard deviation included)

DQM

Operation

- Analysis gets slower over time → workaround restart every n hours (but better to find & fix the actual reason)
- Several minutes delay between run start and histograms appearing in ERECO (=empty plots for short runs) → **update of ERECO and storage framework**
- **Low statistics in physics channels** → **skims**
- Web server gets slower over time → use proper webserver and updated only changed content
- Histogram bleeding into next run → detection and msg to alarm shifter, final fix by ERECO update
- Proper **test bench** ← open
- Automatic copy of histograms to off-site (DESY, kek) cumbersome, sometime stuck. Several script running (e.g. for MiraBelle) ← improvements
- **Reduce manual interventions**
 - In normal operation
 - Offline site and MiraBelle on experiment number change
- Version control of scripts on dqmsrv
 - Strategy for server failure

Detector side

- **Review** what is shown and if important things are missing
- **Employ our existing tool-set**
 - Use **automatic anomaly detection** where possible to help shifter notice issues ← limits, colorize, alarms
 - Export meaningful observables to MiraBelle, document

Framework

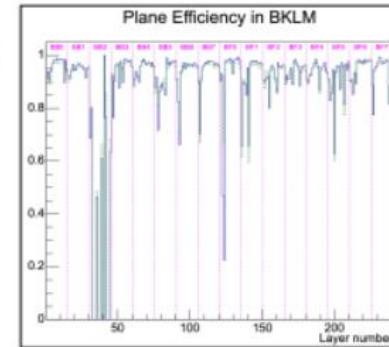
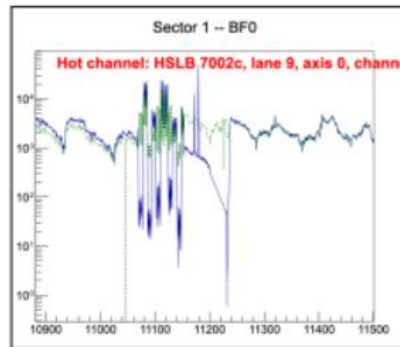
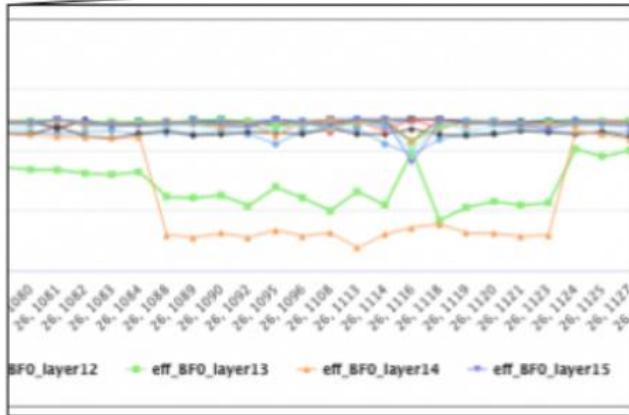
- Run integrated → Time slice delta histograms analysis
- Lower barrier for new developers → consolidate, simplify, cleanup, good examples
- Provide common functionality within the framework to save work on detector developer side
 - Shift man-power to improve on the framework itself!
 - Goal: Hist analysis without writing (too much) code
- Use configuration file for setting, limit and EPICS (high level abstraction)

Shifter & GUI

- Rethink shifter workflow and presentation
- Consolidate web-pages (plots at the top get more attention)
- Automate to avoid subjectiveness, raise attention, and help the shifter decide
- Trend plots: MiraBelle (& CSS?)
- → Discussion needed

KLM DQM

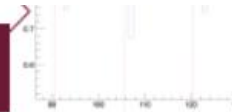
- *Since September*: updates to KLM data quality monitoring – using Mirabelle – to display **history** of key indicators to better see gradual trends and sudden changes



- Implement auto-alerts for KLM DQM to notify expert shifter when a histogram deviates too far from its reference
 - ❖ *Similar to alert system already used by other subsystems*
- Add new training/instructions for expert shifters to use these tools effectively to minimize data-taking disruptions

KLM DQM's to-do-list

- Improving DQM alarm system using ratio plots (M. Veronesi)
- Finer granularity for KLM efficiency (M. Veronesi)
- Implementation of (new!) delta histogram plots for KLM (T. Lam)



Slow-control

Brief summary

After the slow-control group dissolved, no intense development

Remaining/on-going topics

- Development related to the PCIe40 integration
 - Discussed yesterday
- Renovation of the detector control system
 - To be discussed in the latter part of this session
- NSM2-related errors
- Software instabilities
 - Need debugging not only by a single person but in a more collaborative way
- More automatic/convenient recoveries
 - To stack up tolerable errors into a list during a run, then perform a recovery at a next run stop (e.g. due to beam dump)
- Clean-up of log-messages
 - Modifications ready & under review

Do we need to choose Open source for Open science?

- KEK nor Belle II is not a partner of the UNESCO Open Science
- but I naively suppose that there will be a movement toward the Open Science
- If we'd like to declare, in future, that "We respect the recommendation by UNESCO" then we need
 - to migrate from Elasticsearch to OpenSearch
 - to defence that "Elasticsearch is still open enough while it is not approved as open source"
- Generally, we (DAQ-Elasticsearch) just follow the policy of Belle II
- Elasticsearch-OpenSearch migration and related performance studies are possible only during a long-shutdown period

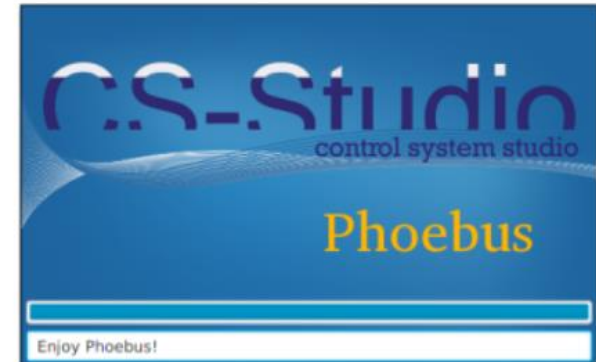
Belle II collaboration matter

Why do we care?

- Upstream CSS is more or less in bugfix-only mode.
- New development mostly takes place in the Phoebus branch.

How to upgrade?

- Two steps:
 - 1) Get the software up and running.
 - 2) Port our content (OPIs).



Migration to Phoebus

OPI to BOB Upgrade Path

- Display Builder can seamlessly open OPI files.
- Most actually do look quite good already at this stage.
 - ⇒ Conversion can be spread out in time. OPIs and BOBs will just mix.
- In the ideal case, open all OPIs once in the editor and save the resulting BOBs.

- Display rules are usually compatible.
- Many scripts need to be manually adapted.



I will upload his talk (and others) recorded by Zoom soon.

Detector control system

1st priority given to HV control

- because it influences SKB injection
- We revisit definitions one by one
- Actual implementation to be done by the end of 2022

State definition

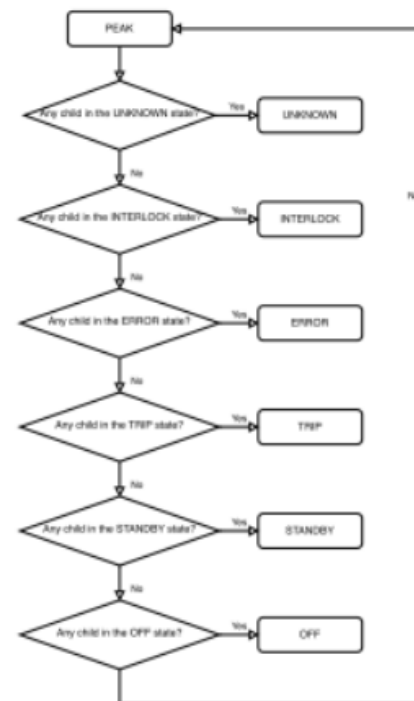
Each sub-detector HV process works as a finite-state machine (FSM), and thus has its state (HV state). For logical objects, the mandatory HV states are PEAK and OFF, reflecting conditions for which data taking is possible or impossible, respectively. The state UNKNOWN is used in case the condition cannot be verified. Other possible states are 1) ERROR, which indicates that normal operation not possible or will become impossible very soon, and 2) TRIP, which is due to over-current or over-voltage of the children modules. The actual state of these logical objects is determined by the states of the associated lower level objects (children) via state rules, an example of the state rule is figure 1.

During beam operations, all sub-detectors ramp HV to nominal values (“PEAK”) only when stable beams has been declared by SuperKEKB, implying no more manipulations/adjustments are done on the beams. Outside stable beams, HV is set to a lower STANDBY value. Stable beams is indicated to Belle II by the HV permission flag, which is sent from the SuperKEKB group via the EPICS network. Current Standby settings are summarised in table 1.

The master node of Belle II HV nodes (HVMASTER) aggregates each sub-detector HV state. The aggregated HV state is treated as the global HV state, which is directly coupled with the SuperKEKB injection blocking algorithm. The coupling between the global HV state and injection blocking is summarised in table 2. The detail of the injection blocking algorithm is described in the MDI section.

State transitions. State transitions can be initiated for every FSM objects by commands in the NSM2 framework. The higher level node propagate the commands to their lower level nodes (children). The state transitions are summarised in figure 2.

State rule

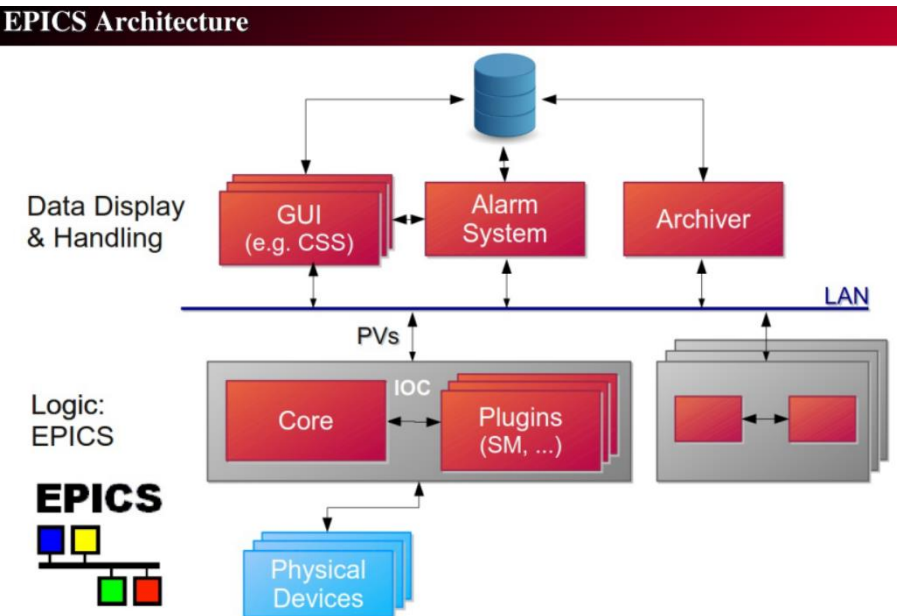


- Detector environment (Recommended by BPAC)
- Interlock documentation

It will not be an LS1 project but some possible options about new/current framework were introduced.

EPICS based DCS

(B. Spruck)



OPC based DCS

(T. Kunigo)

What will be changed?

Current

- No security
 - While protected by the bdaq network against non Belle II users
 - Any users can damage our detectors unintentionally
- Controller processes need to be developed
- Many hard-coded configuration

OPC-UA based

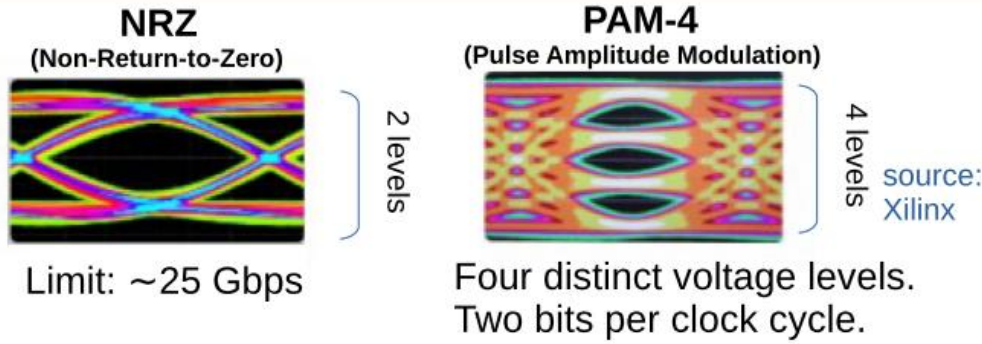
- Security will be introduced
 - LDAP authentication
 - Role-assignment to each user/group
 - OPC-UA servers ready
 - Configuration can be summarised into a file (e.g. XML format)
-
- OLE: Object Linking and Embedding
 - OPC: OLE Process Control (since 1996)
 - OPC-UA: OPC unified architecture (since 2008)

Need to evaluate advantages, disadvantages, interfaces, cost and personpower etc. more

For higher trigger rate

Activities for new high-speed readout technologies in E-sys group

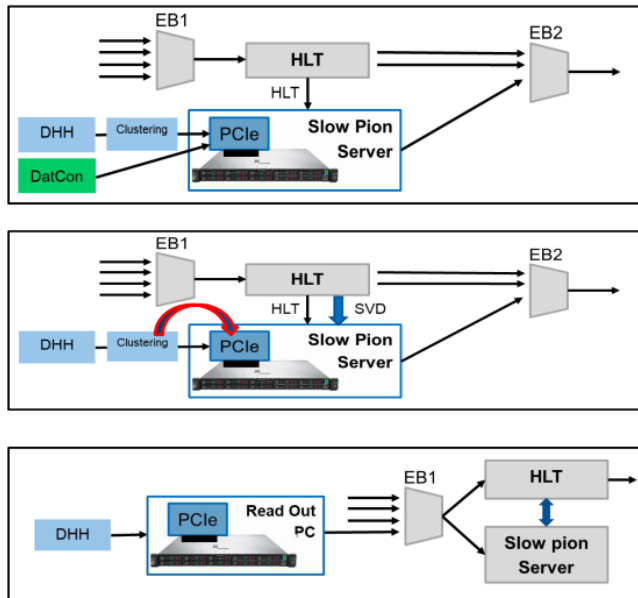
(YT. Lai)



PXD readout upgrade

(I. Koronov)

PXD Readout Upgrade



CDC FEE upgrade

(N. Taniguchi)

- 2022
 - evaluation of prototype board → start discussion about ver.2 which should be almost final design
 - finalize design of ASIC(ASD+FADC)
 - radiation test with gamma and neutron
- 2023
 - mass production of ASIC chip
 - production of ver.2 and performance test
 - finalize design of electronics board
- 2024-2026
 - mass production of electronics board

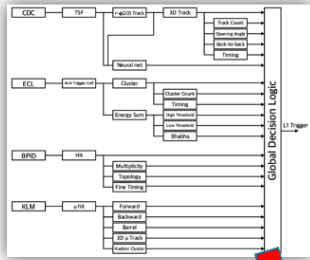
situation of mass production depends on budget

For installation of board, we need to open detector fully at Bwd. side.

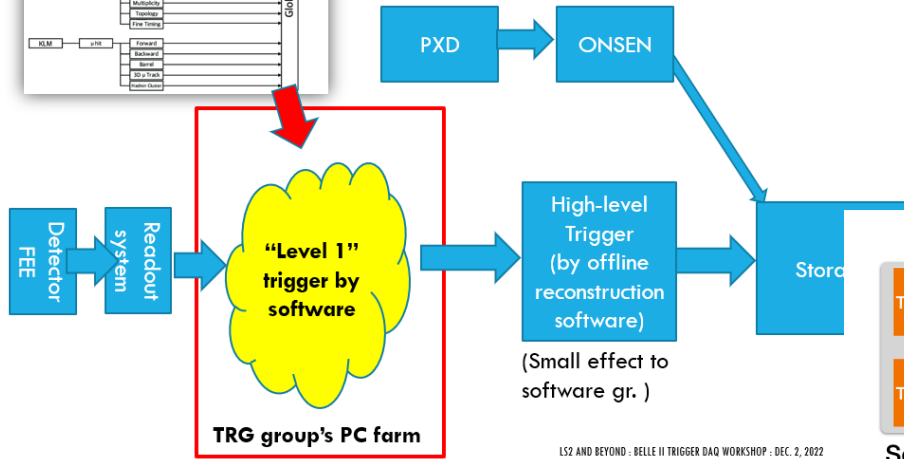
Request to extract QCS, remove cables, dock-boxes and dock-ring for VXD.

Trigger system then moves to PC farm...

Level 1 trigger system

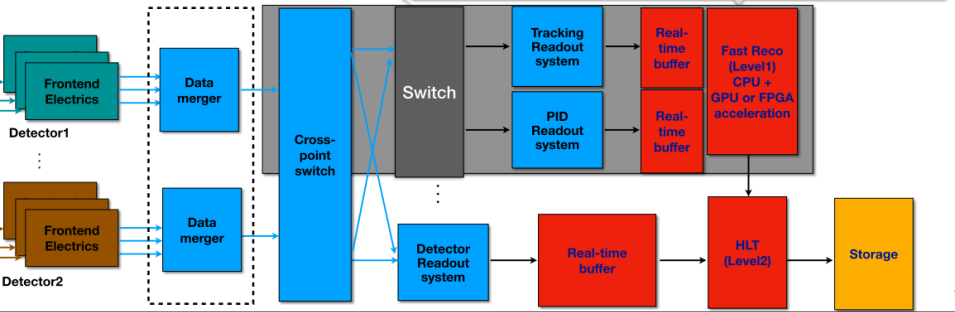
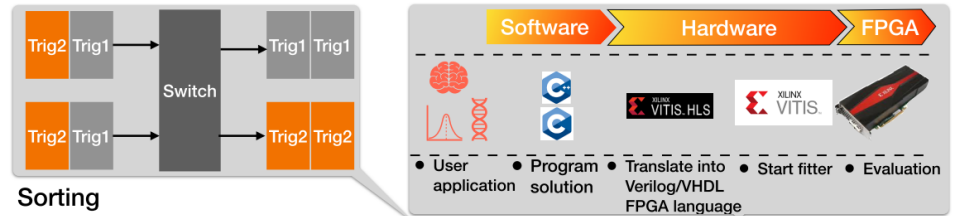


➤ Hardware trigger system itself might stay as a throttling system for a while.



LS2 AND BEYOND : BELLE II TRIGGER DAQ WORKSHOP : DEC. 2, 2022

Partial software trigger



Thank you for useful inputs from sub-detector DAQ experts about high-rate limit !!

Thank you for your
presentation and discussion
in these 4 days !
Let's prepare for the next
physics run and future.