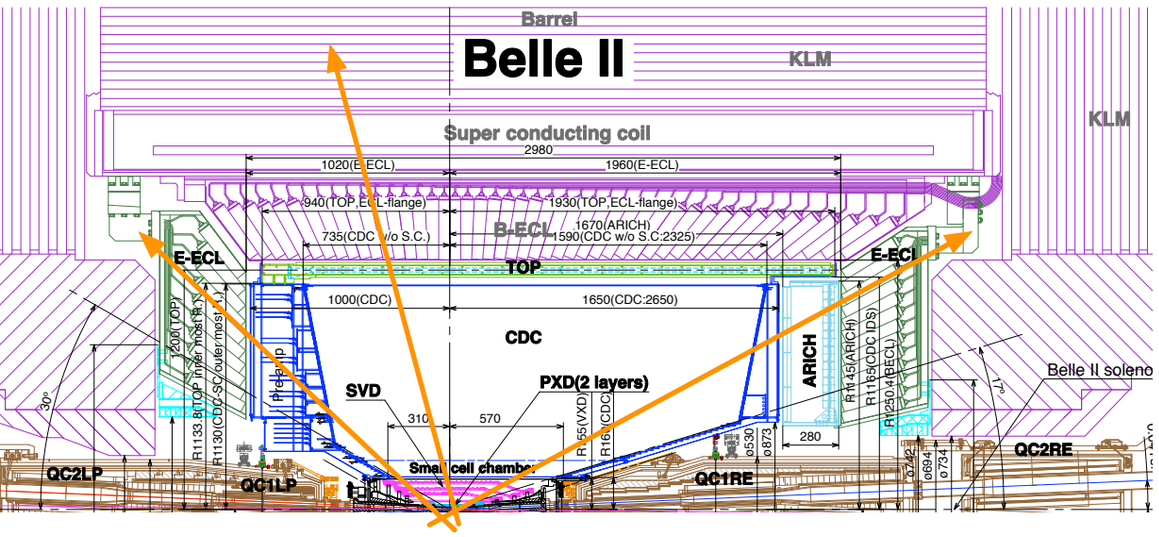
Overview of

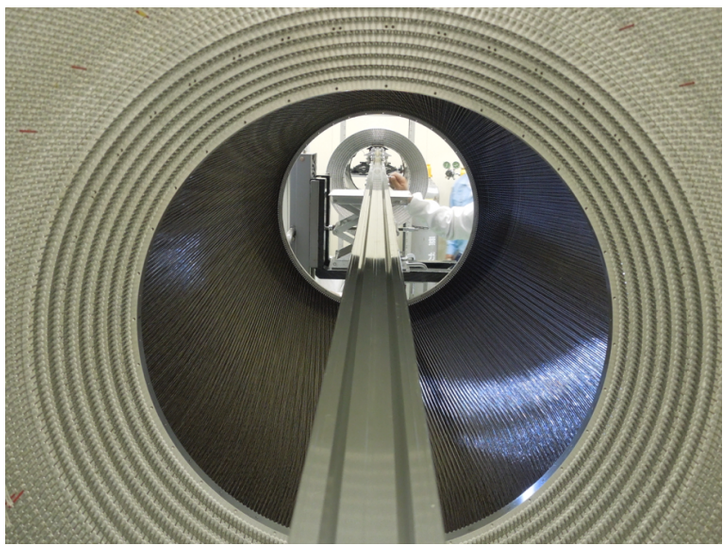
CDC FEE upgrade

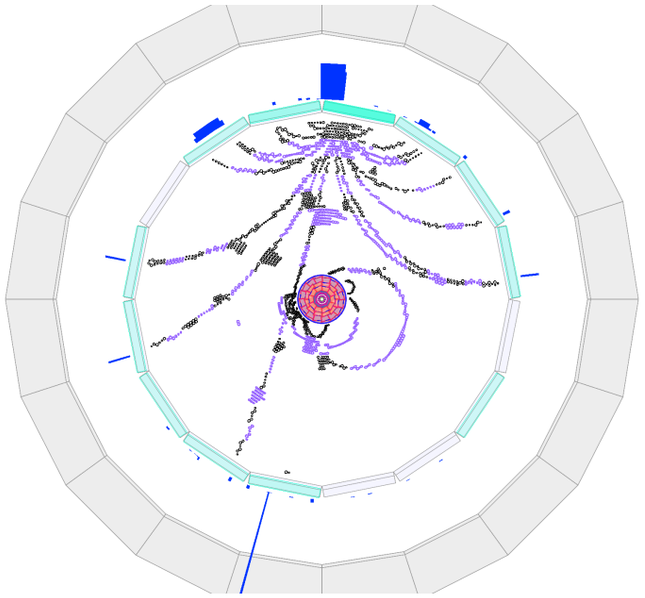
Nanae Taniguchi (KEK)

Trigger-DAQ workshop
2022.12.02

Central Drift Chamber

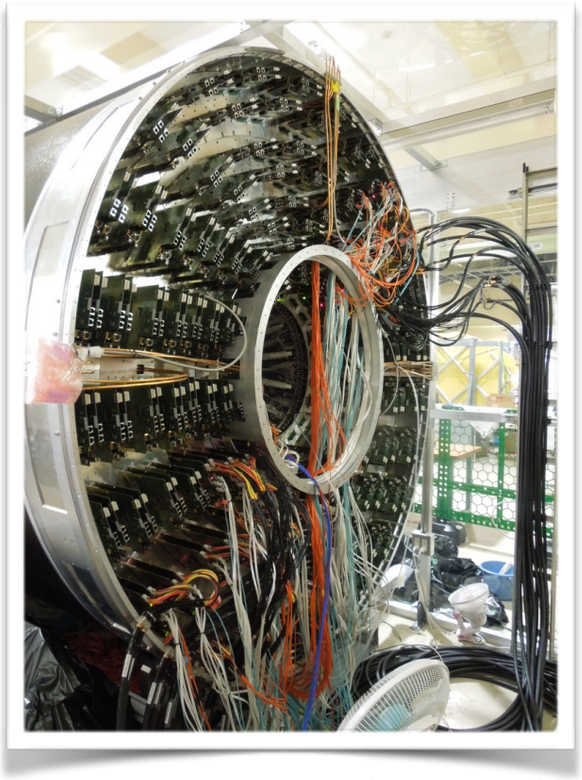


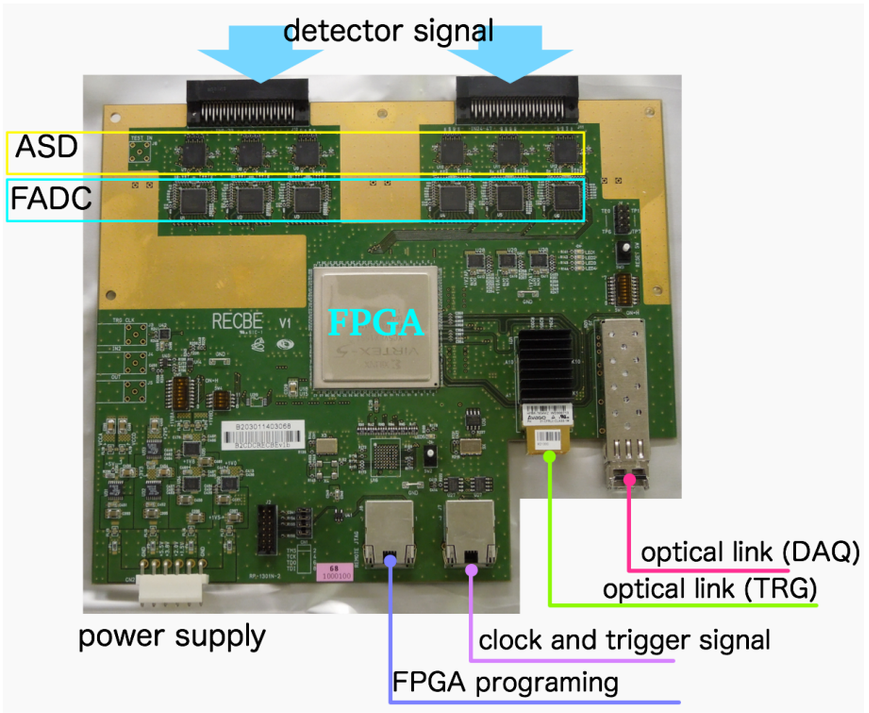


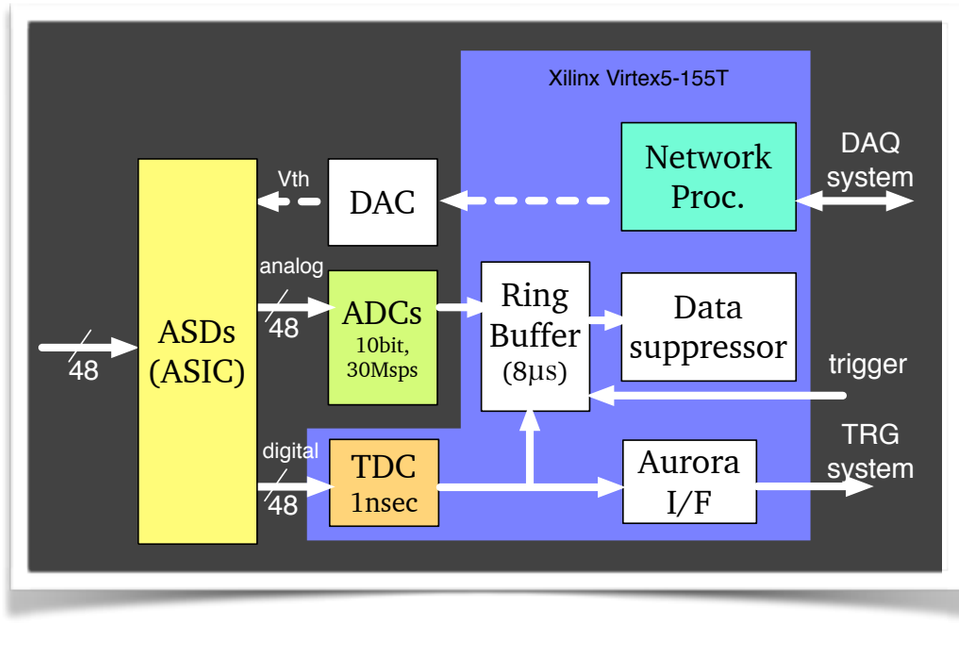


- Main tracking device of Belle II
  - measure position of charged particle and provide track information
  - momentum, particle ID, track trigger
- Drift chamber ; wire(Au and Al) + gas(He:ethane)
  - low material to suppress multiple scattering
  - measure drift time and dEdx.

CDC readout system







- 299 board readout 14336 signal channels
- readout board is located just behind of detector (Belle Bwd)
- We use FPGA based electronics
  - all functions on the board.
- development and mass production has been supported by experts of KEK Esys and NTU
  - 300+30 board were produced.

CDC electronics upgrade

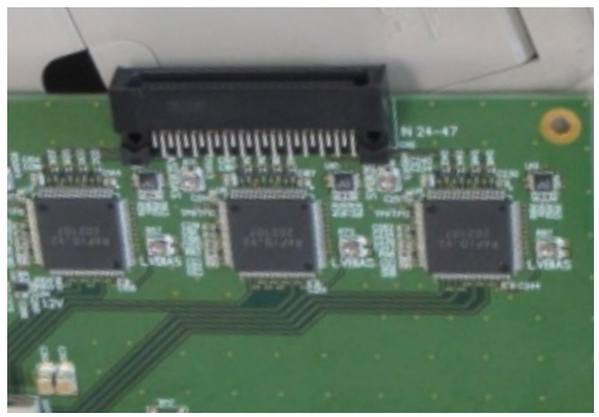
- Motivation
  - radiation tolerance
    - optical module for TRG. life~300Gy < Belle II 10 years
    - soft error of FPGA
  - cross talk suppression
  - power consumption suppression
    - 15W/board x 300 ~ 4.5kW. we need water cooling
    - 4.5kW = Belle-1 x10
  - smaller board size for better cable handling inside CDC cover

- radiation test with gamma and neutron
  - FPGA with prototype board and optical module(QSFP)
  - scheduled in Jan. - Mar.
  - Y. Nakazawa-san organize

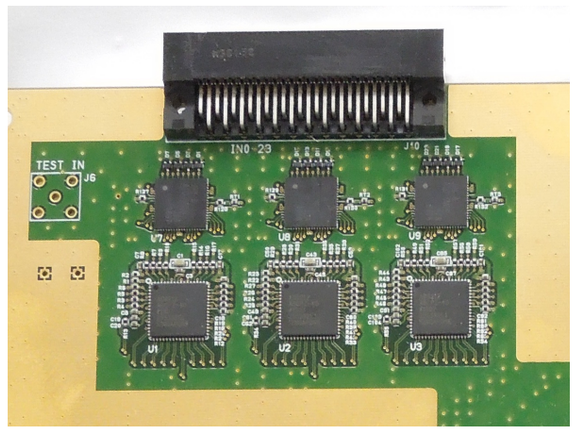
new ASIC

- New ASIC chip is designed by M. Miyahara (KEK Esys)
  - 8ch/chip. same as the present chip
- Amp-Shaper-Discriminator and FADC are integrated in one chip
  - FADC; commercial product → original design. lower power consumption is expected
- performance study has been done by A. Gonnokami(Student of Tokyo Univ.) and Y. Nakazawa
- beam test was done in Nov.
  - we may finalize design of ASIC and propose mass production, if beam test results are ok
- Mass production; 330x 6chip ~ 2k

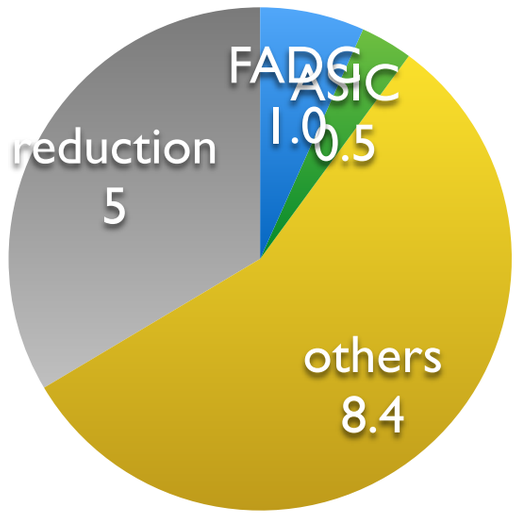
ASD and FADC two-in-one



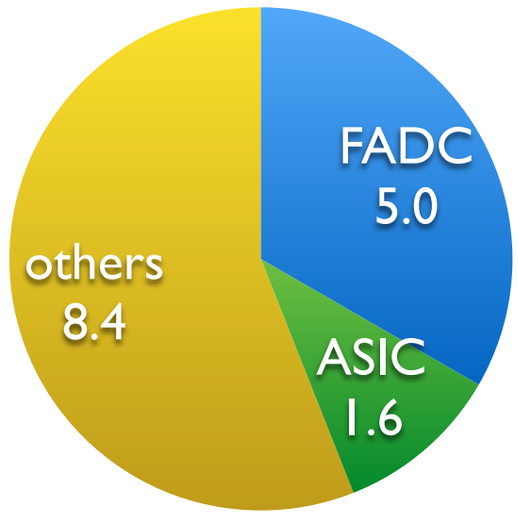
ASD and FADC individual chip



power consumption



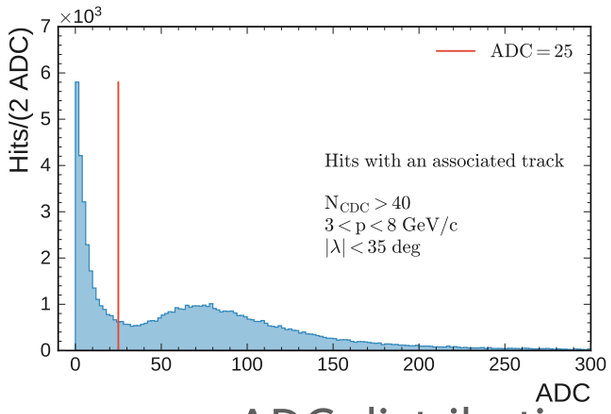
~10W/board (expected)



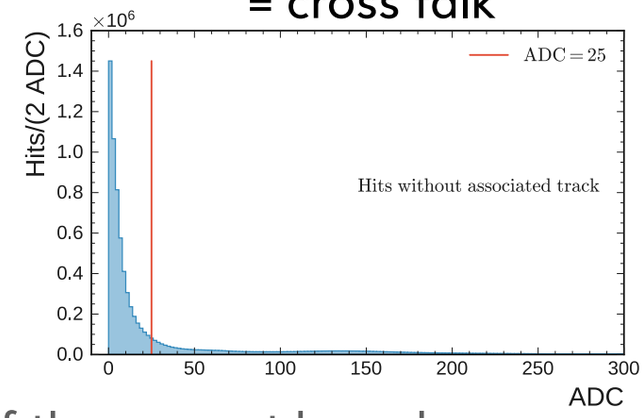
~15W/board

cross talk reduction

with track associated hits



without track associated hits
= cross talk



ADC distributions of the present board
w/ and w/o associated track

EOI

2019
Sasha (DESY)

Efficiency of the filter for hits on/off track

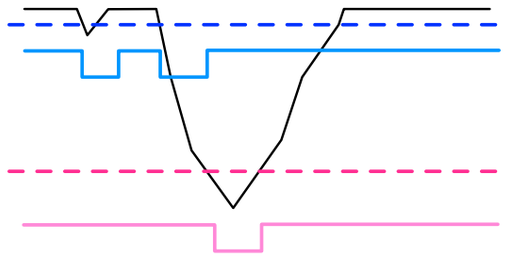
	ADC>18	ADC>18 and ASIC	1200>ADC>18 and ASIC
On Track	95.4%	93.2%	92.5%
Off Track	54.1%	31.1%	25.8%

Check efficiency for hits on / off tracks (for tracking without bg cut). Note that combined ADC&TOT cut has slightly better performance vs single ADC cut

→ ASIC cuts brings significant additional reduction of cross-talk hits with a small signal loss. Further reduction of background can be achieved by upper ADC cut (not considered in the following)

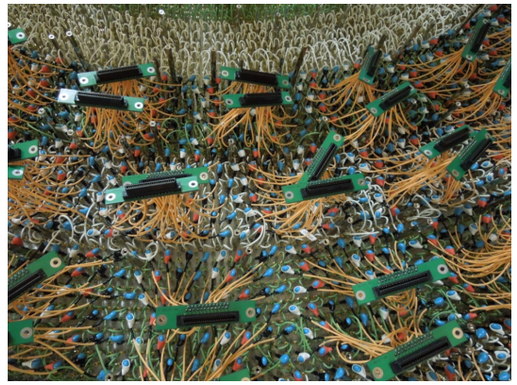
10

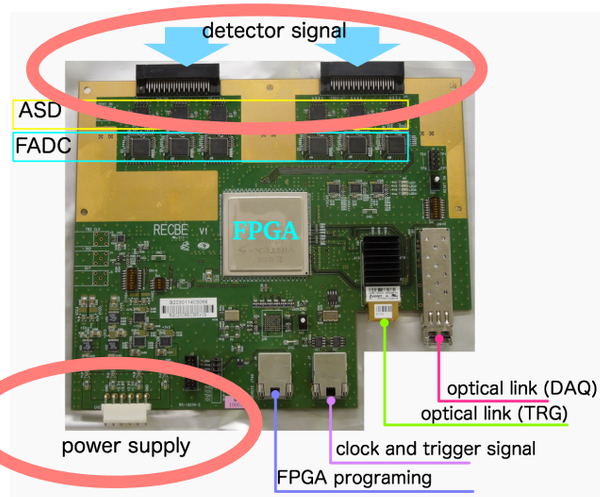
- In the present condition,
  - mostly ADC value of cross talk is small. Applying ADC cut is effective in offline analysis (tracking)
  - higher threshold of FE is effective to suppress fake hit of TSF and L1-trigger rate, while timing resolution and trigger efficiency become worse
  - ASIC-based cross talk filter is also effective
- In the new ASIC,
  - pulse height of cross talk is 1/10 lower
  - double thresholds are implemented. Higher threshold discriminate signal and cross talk, while lower threshold determine wire hit timing

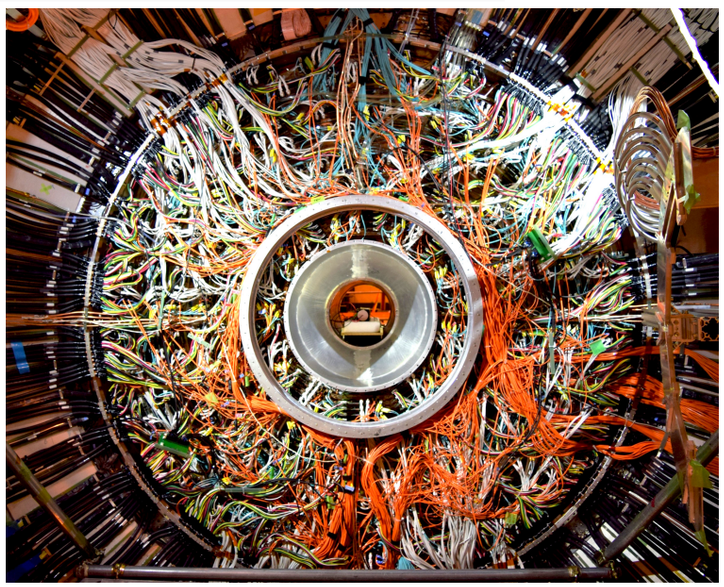


baseline condition

- Constraints
  - type and layout of signal connector must be same as the current design
  - also type of power supply connector must be same
  - board size, height must be same. smaller is better
    - space is quite limited
- optical cables will be replaced
  - 2C x300(DAQ) and 12C x300(TRG) → 12Cx300
- cat.7 cable will be kept for the new board
  - Option. It is replaced by optical cables. It is related to upgrade of FTSW by Nakao-san. Improvement against noise is expected.
    - my concern is space and power consumption
- cooling system should be re-designed







important thing during LS-1

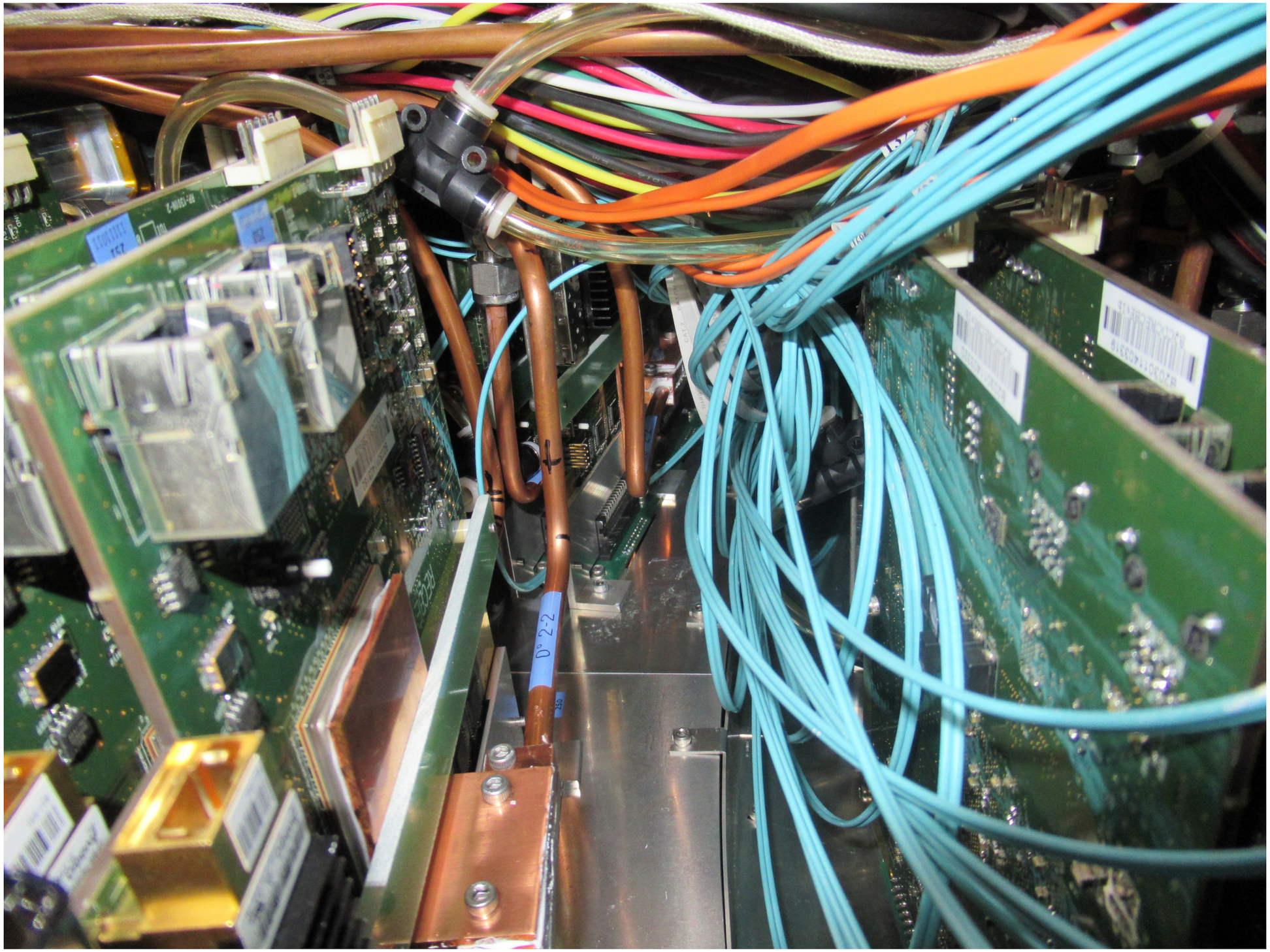
- Experts who are working for upgrade should see the real detector
  - I have asked experts of E-sys as well. We will do in Feb. and later when CDC cover may be fully opened.
    - not only experts but CDC member. I will arrange
- LS-1 is only chance to discuss by looking the actual things before we install new electronics
  - how to install new electronics, how to rebuild water cooling system, how to replace optical cables, how to maintain at limited situation….

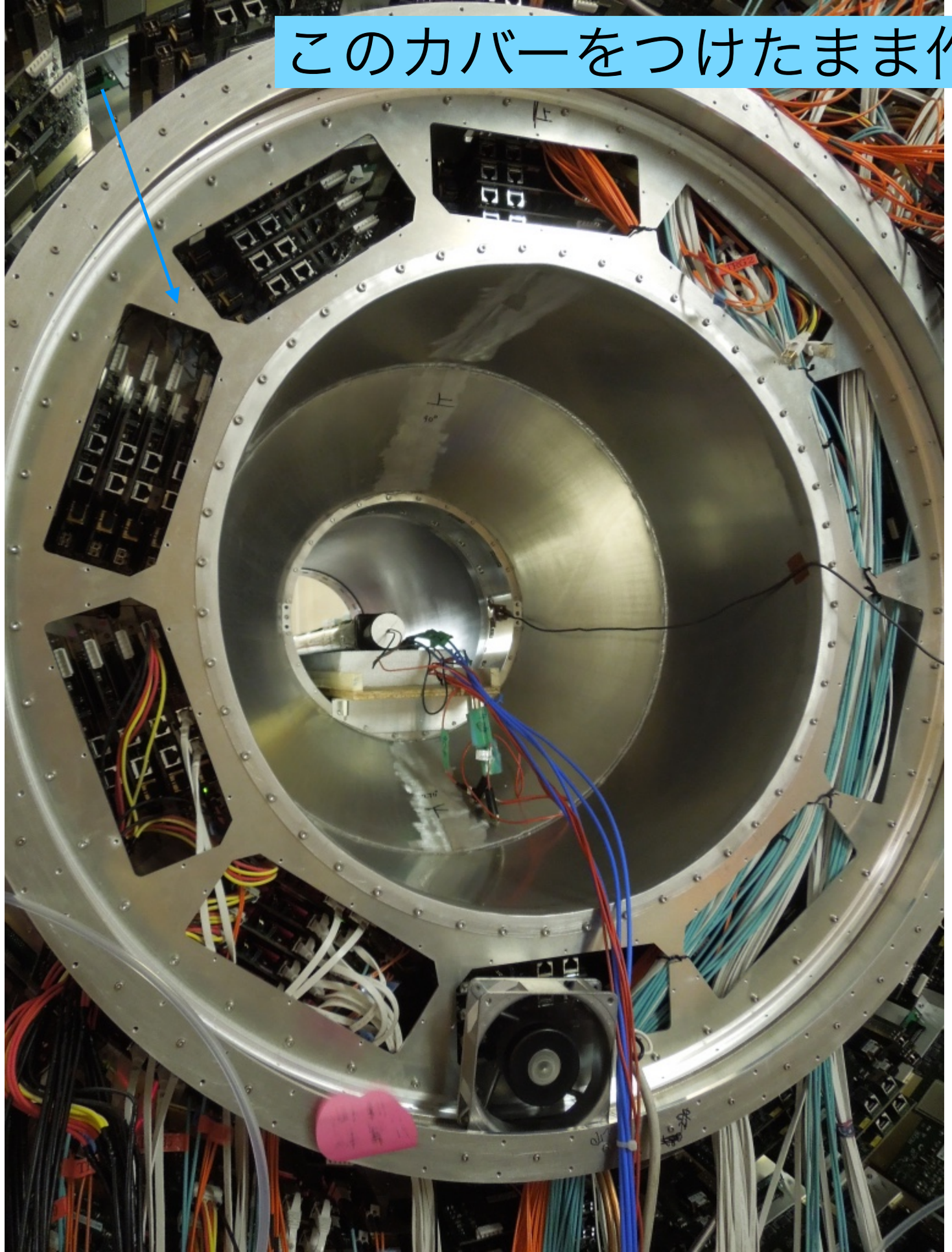
plan

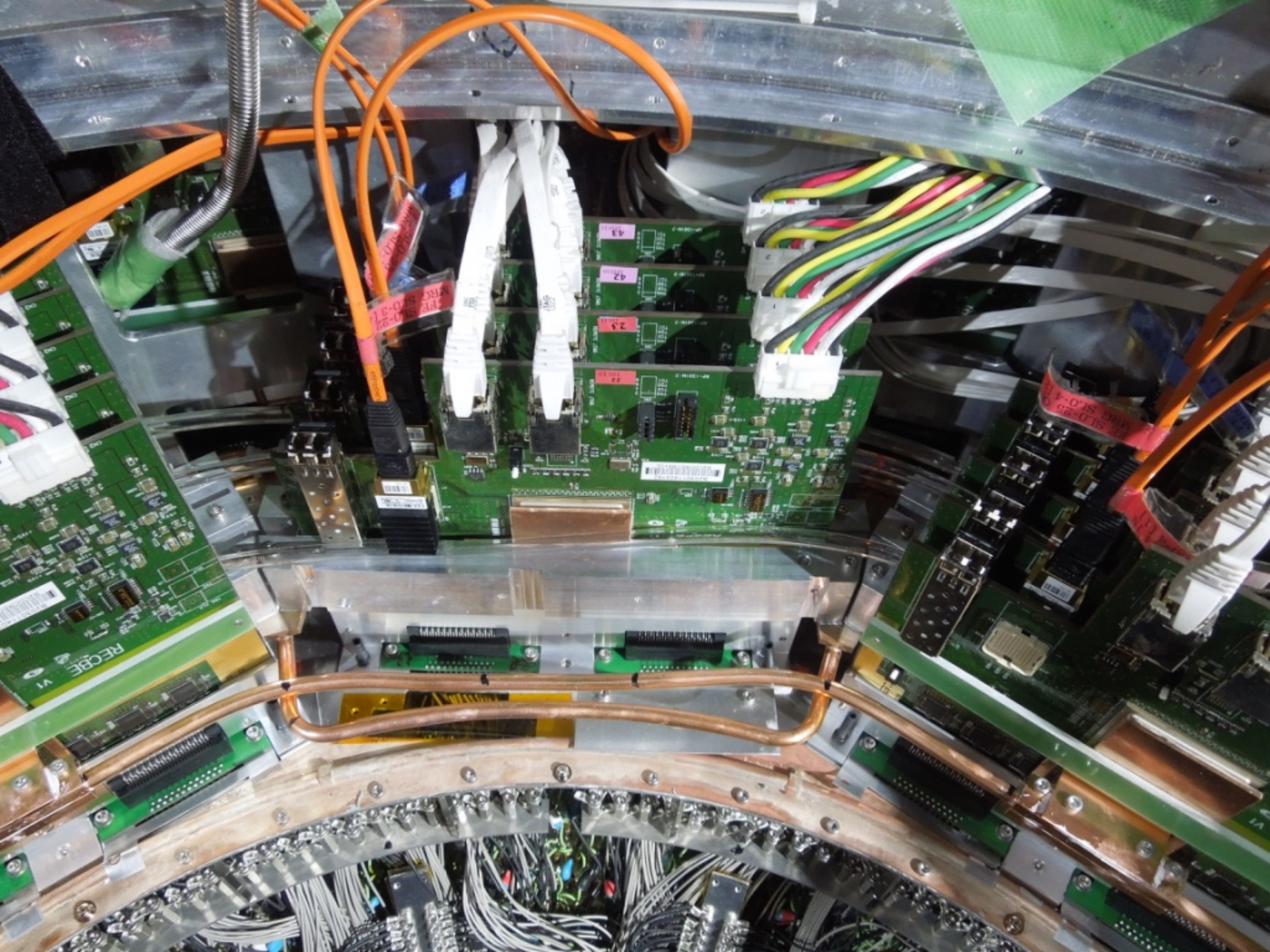
- 2022
  - evaluation of prototype board → start discussion about ver.2 which should be almost final design
  - finalize design of ASIC(ASD+FADC)
  - radiation test with gamma and neutron
- 2023
  - mass production of ASIC chip
  - production of ver.2 and performance test
  - finalize design of electronics board
- 2024-2026
  - mass production of electronics board

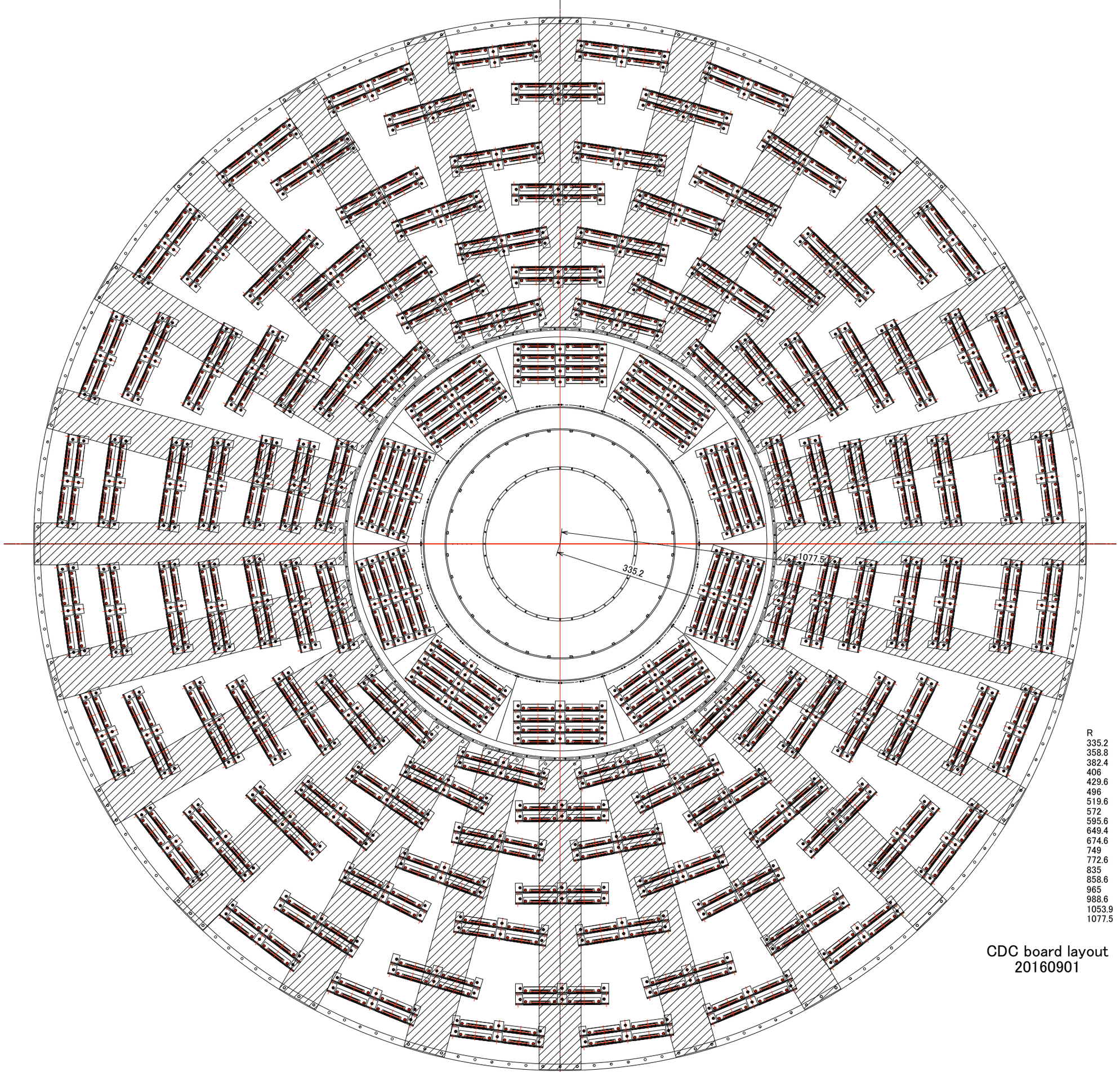
situation of mass production depends on budget

For installation of board,
we need to open detector fully at Bwd. side.
Request to extract QCS, remove cables, dock-boxes and dock-ring for VXD.


D° 2-2


このカバーをつけたまま作業





R
335.2
358.8
382.4
406
429.6
496
519.6
572
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649.4
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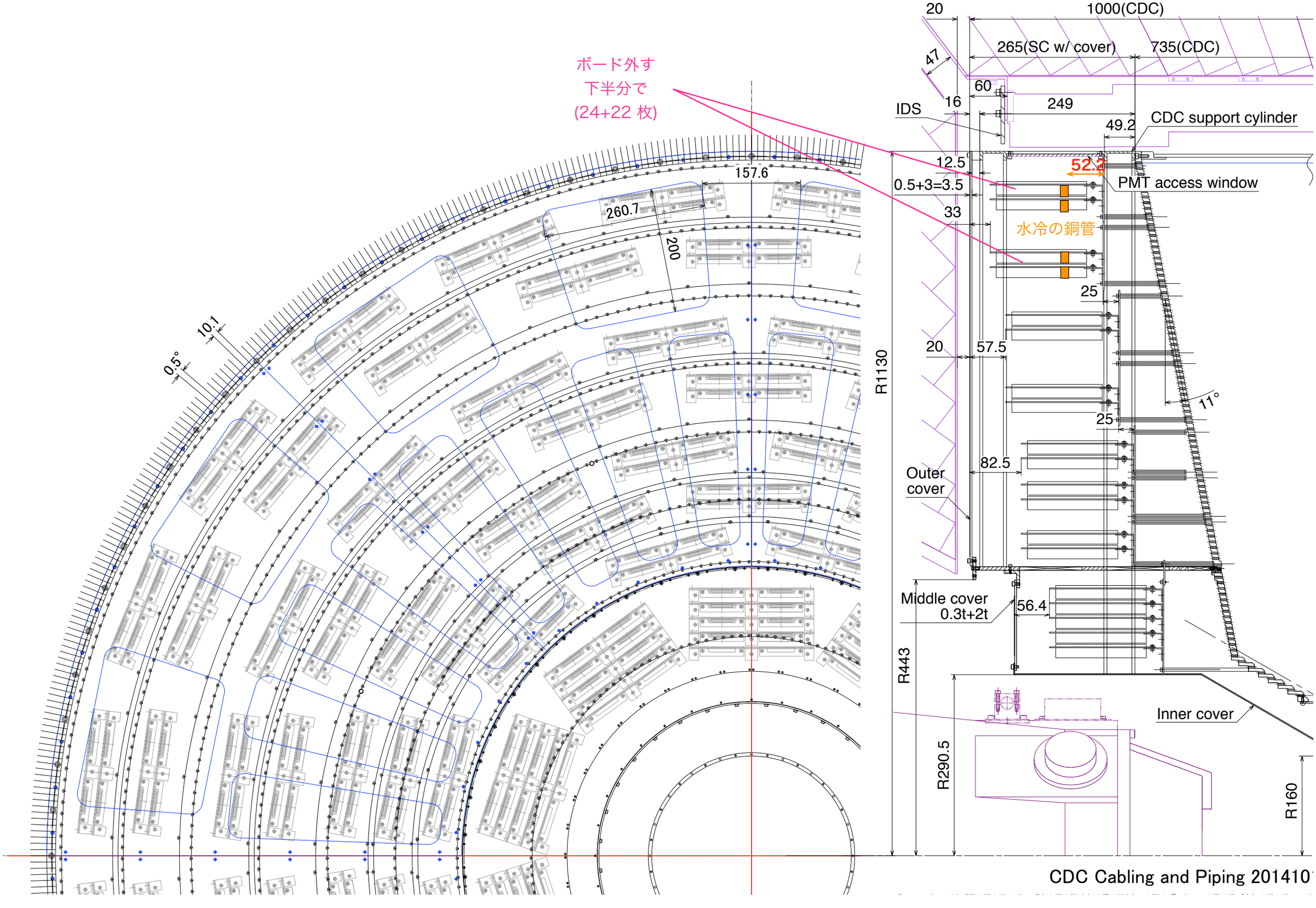
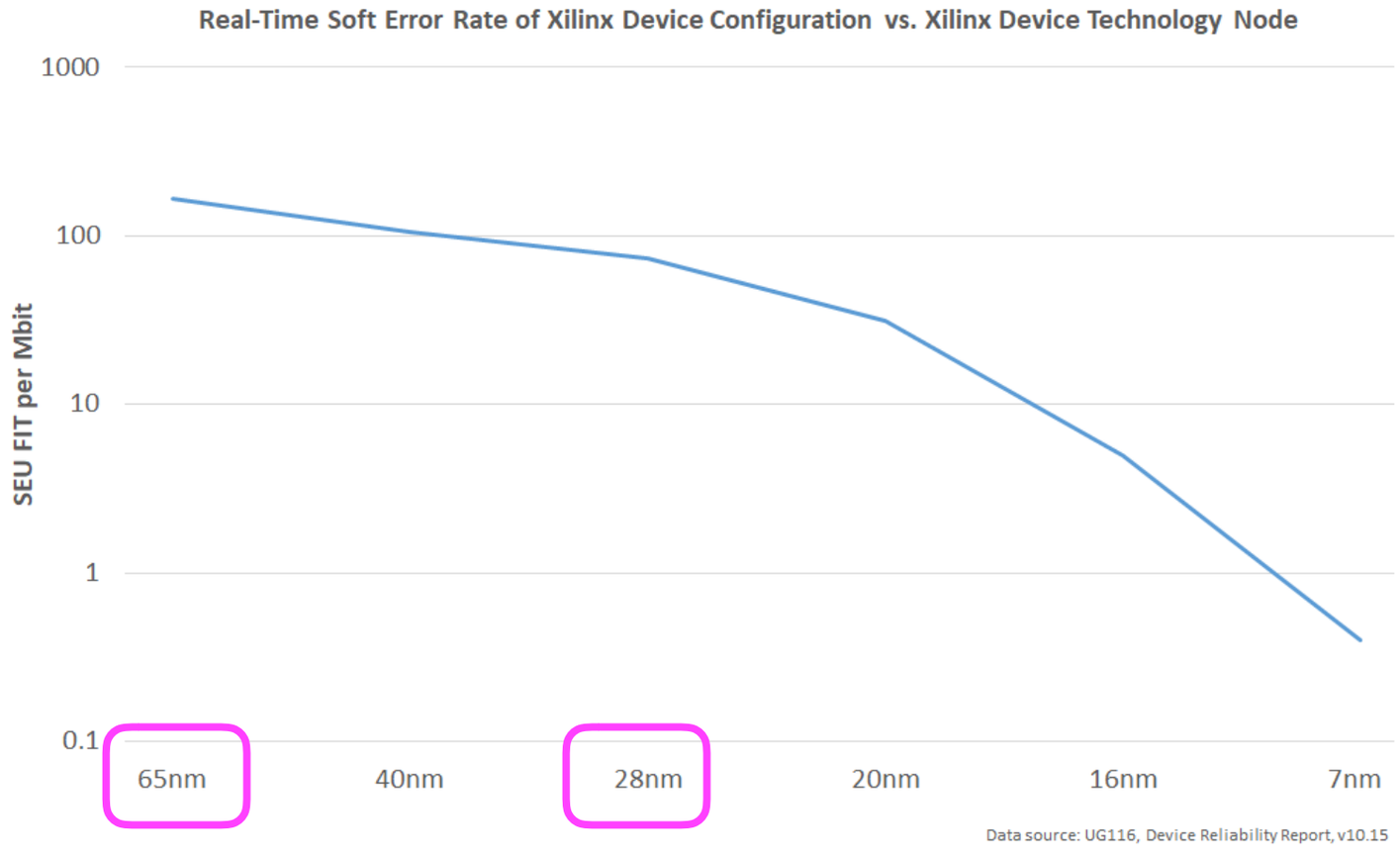
749
772.6
835
858.6
965
988.6
1053.9
1077.5

CDC board layout
20160901


ボード外す
下半分で
(24+22 枚)
157.6
260.7
200
10.1
0.5°
20
1000(CDC)
265(SC w/ cover)
735(CDC)
47
60
16
249
IDS
CDC support cylinder
49.2
12.5
52.2
PMT access window
0.5+3=3.5
33
水冷の銅管
25
20
57.5
R1130
11°
25
82.5
Outer
cover
Middle cover
0.3t+2t
56.4
R443
Inner cover
R290.5
R160
CDC Cabling and Piping 201410

soft error due to radiation

- FPGA ; Virtex-5 → Kintex-7



https://www.xilinx.com/support/quality/reliability.html#seu

	the present board	upgrade	status
power consumption (ASIC of ASD)	separated chips, ASD and FADC	functions of ASD and FADC are in one chip. ~60% reduction is expected in ASD+FADC	design is almost finalized (M. Miyahara, KEK Esys) mass production from 2023
cross talk (ASIC of ASD)	~100mV pulse height induced in neighbor ch with 7pC input	~10mV pulse height induced in neighbor ch with 7pC input + double thresholds	
FPGA soft error	Virtex-5	Kintex-7	purchased and fabricated on the prototype board. irradiation test is planed in 2022.
radiation tolerance of optical transceiver	SFP for DAQ (1kGY) Avago HFBR-7934WZ for TRG (300-400Gy)	QSFP	purchased several QSFPs to be tested with irradiation
bandwidth of optical transceiver	SFP for DAQ Avago HFBR-7934WZ for TRG (3.125Mb/s)	one QSFP in stead of two different optical transceivers	basic test is done with TRG system