PXD Read Out Upgrade

Igor Konorov

Institute for Hadronic Structure and Fundamental Symmetries (E18)

TUM Department of Physics

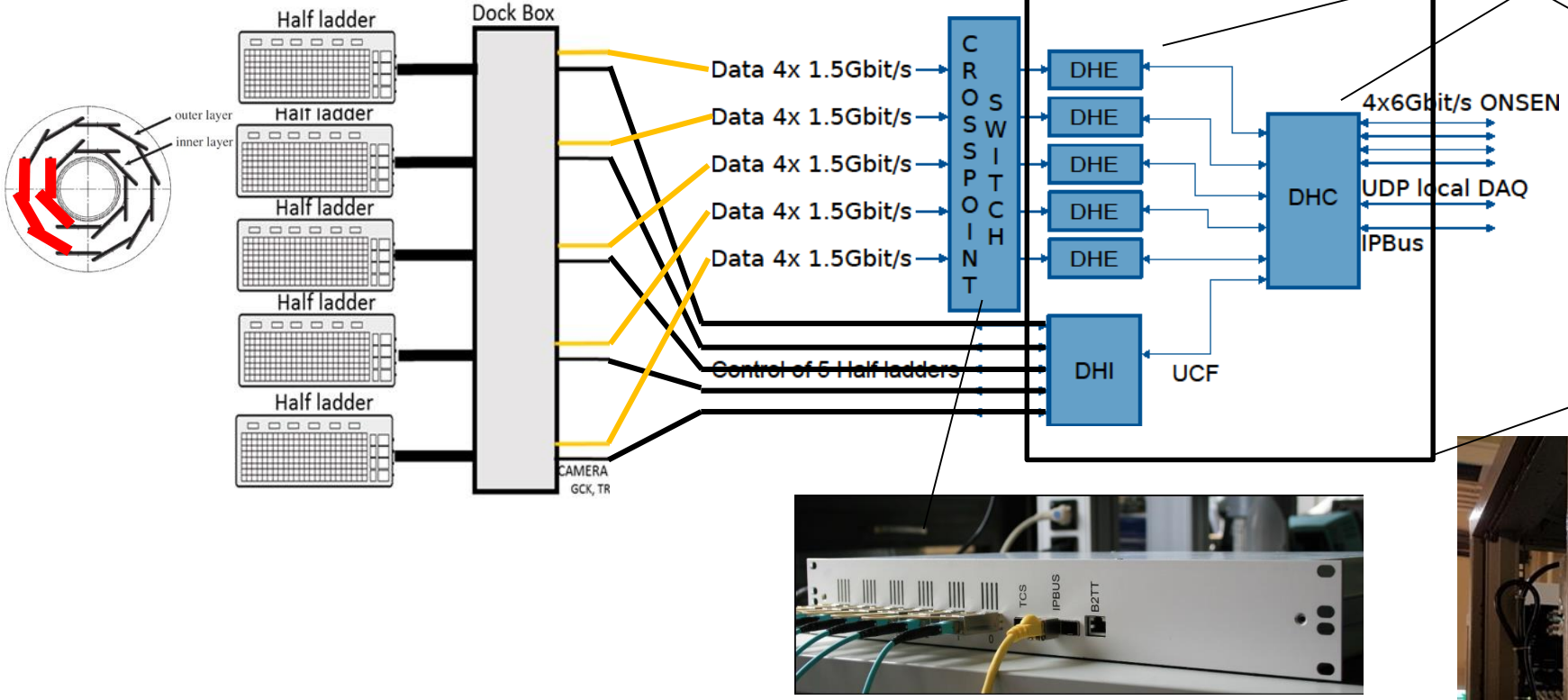
Technical University of Munich

Belle II Trigger/DAQ Workshop 2022

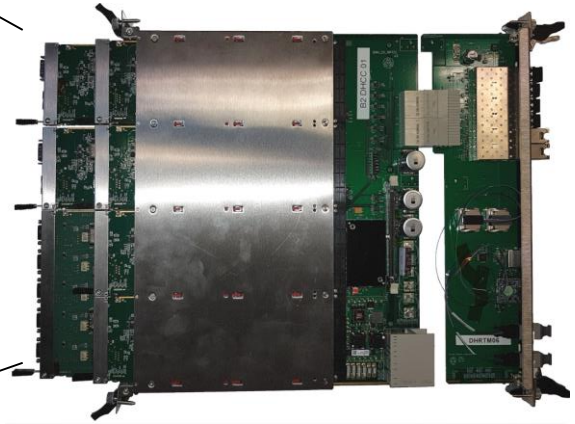
Outline of Talk

- PXD Readout Overview
- DHH Carrie Card Issues and progress with new development
- New Data Throttling Algorithm
- Upgrade of PXD Readout
  - Architecture
  - PC server and PCIe cards
  - Full PXD readout architecture
  - Slow Pion Recovery activity

PXD Readout Overview



DHE/DHC



Cross-point switch : 144x144 @6GB/s

DHI : A7XC100T, Configuration and Trigger

DHE/DHC : V6XC130 FPGA, 4GB memory, Data processing

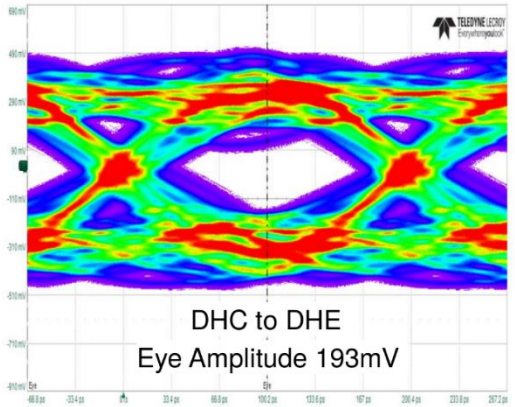
DHH : DHI + 5xDHE + DHC

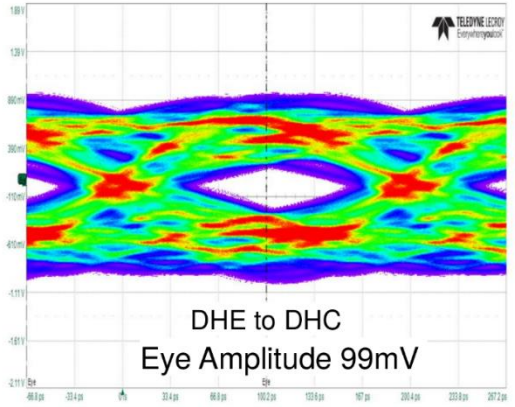
DHHCC Issues

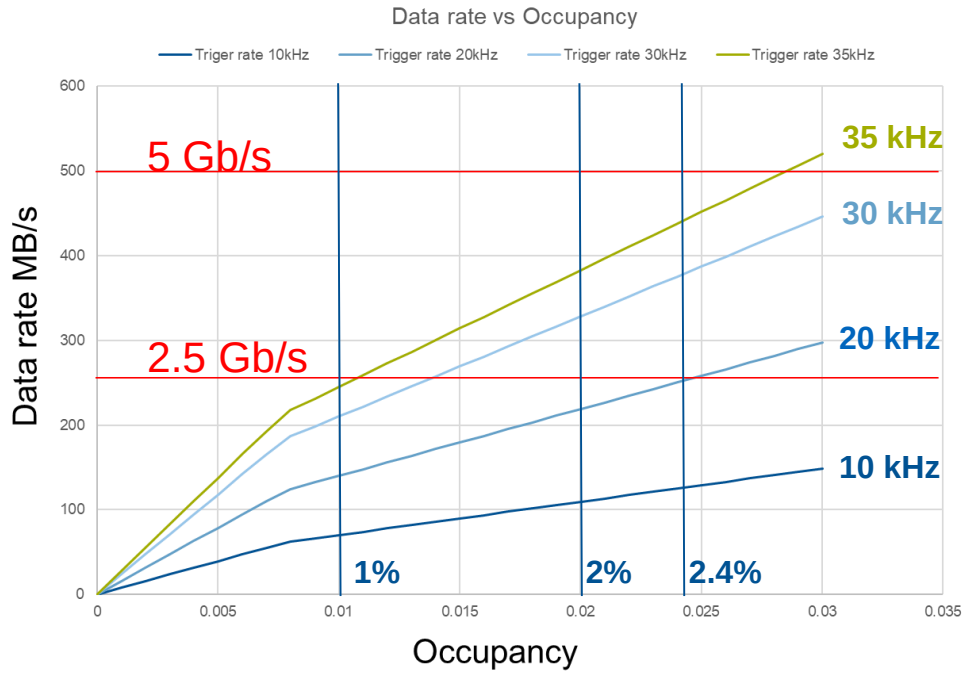
- DHC ⇔ DHE/DHI links run at 2.5 Gbps
  - IBERT tests

  @2.5Gbps all links working fine

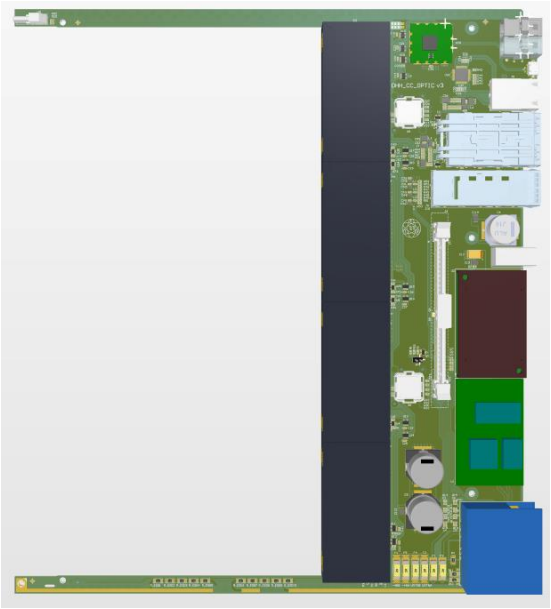
  @5.0 Gbps 1 DHE fine, 4 DHEs high error rate
  - Signal degradation
    - signal losses leads to small open eye
    - layout issue

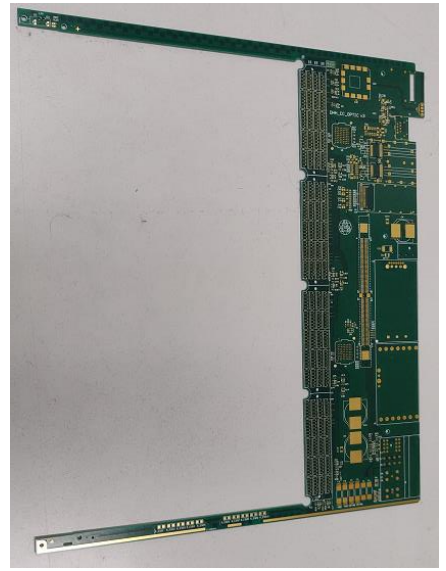






DHHCC Upgrade





Design changes :

- PCB layer stack optimized for matched impedance transmission lines
- Improved layout for high speed links
- All external transceivers mounted on DHHCC no RTM, it will improve quality of ONSEN links

Status

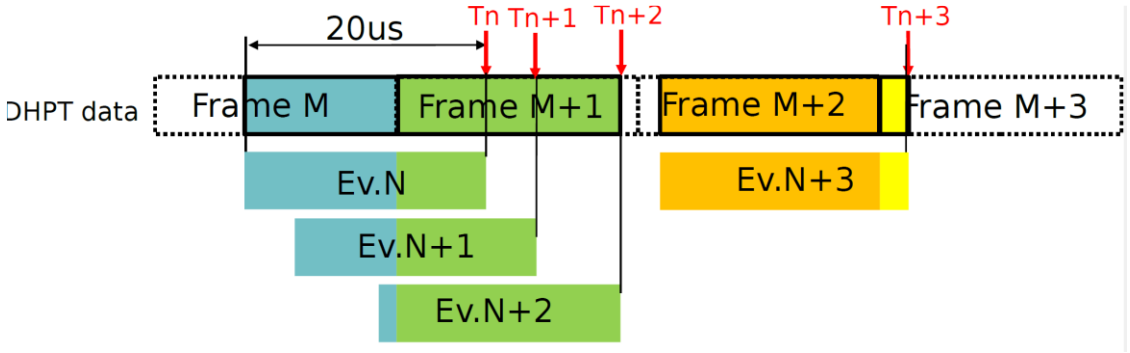
- Prototype PCB produced and being assembled now
- Test is planned in January 2023
- Mass production is expected to complete in March 2023

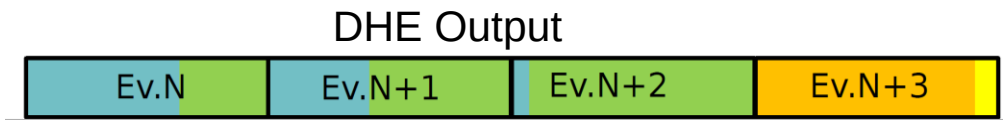
Firmware changes required

- Change protocol from 2 byte to 4 byte protocol to keep UCF clock at 127MHz

PXD Data Throttling I

- Fundamental difference of PXD vs other detectors is an integration time of 20 us or 2 KEKB revolution cycles.
- PXD readout based on running shutter. It takes 20 us for one round and each round organizes hits in single FRAME
- B2TT Triger initiates PXD Trigger which is effectively DATA ENABLE signal





- DHPT links' bandwidth allow to read maximum 2.3% occupancy in continuous mode when DATA ENABLE is always active
- Triggering increases averaged PXD occupancy to higher values on an expense of loosing fraction of data with some probability
- At some conditions it may cause loss of synchronization of data between DHP and DHE

PXD Data Throttling II

1. **Current data throttling implementation**
   - Veto Trigger after every bunch injection
   - DHE limits maximum occupancy of one frame to programmable value. Now it's 4%

   Disadvantage of the implementation
   - Requires fine tuning of Trigger Veto length
   - DHPs buffers are overwhelmed
   - Readout problem probability will become higher at higher luminosity

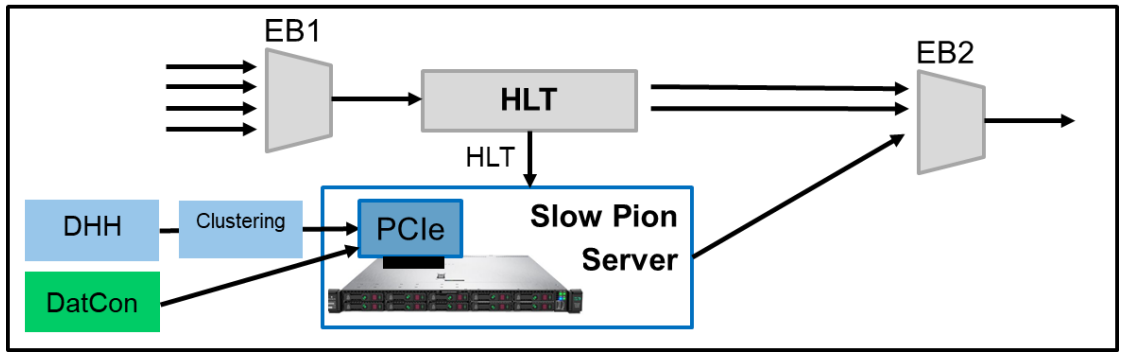
2. **New data throttling algorithm**
   - Idea is to prevent overflow of DHP buffers to handle any occupancy
   - Normal operation
     - DHPs run continuously
     - DHE monitors detector occupancy
     - DHE collects data in time with B2TT trigger
   - Throttling
     - DHE detects high occupancy and issues VETO
     - DHE VETO => DHC => DHI => DHP
     - VETO valid till end of FRAME or till end of next FRAME
     - VETO conditions
       - Exceeding maximum occupancy of one frame
       - Exceeding maximum occupancy of part of frame
       - Exceeding DHP buffer maximum fill level by monitoring data latency

Time Lines

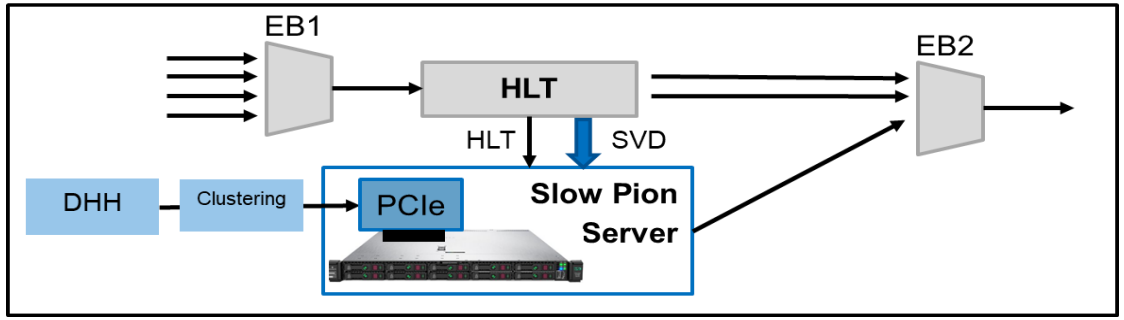
1. New throttling algorithm
   - Test in TUM laboratory - February 2023
   - Test in DESY/KEK - March-April 2023

2. DHH Carrier Card upgrade
   - Prototype test - January 2023
   - Mass production - March 2023
   - Commissioning in Belle2 - June-September 2023

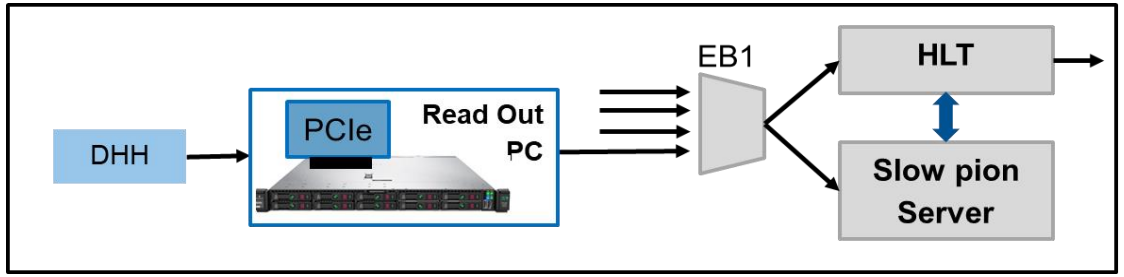
PXD Readout Upgrade



Comments
- changes of DATCON firmware

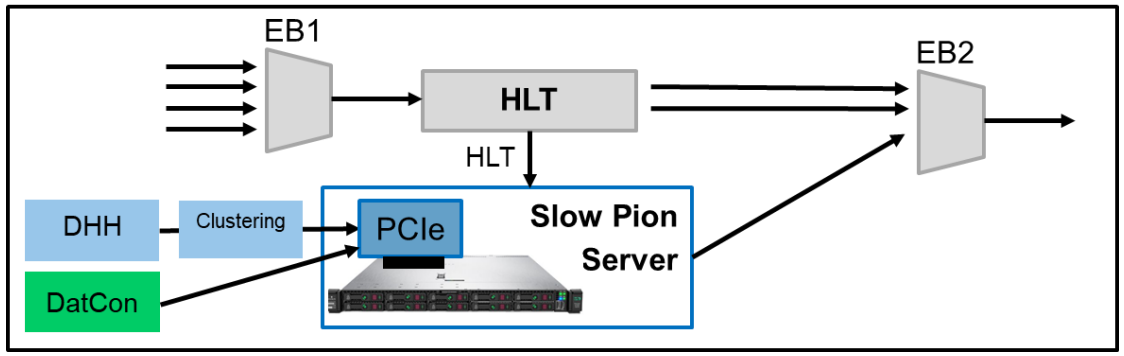


Comments
- Forwarding SVD data to PXD server



Comments
- EB1 performance may not be sufficient for PXD data

PXD Readout Upgrade



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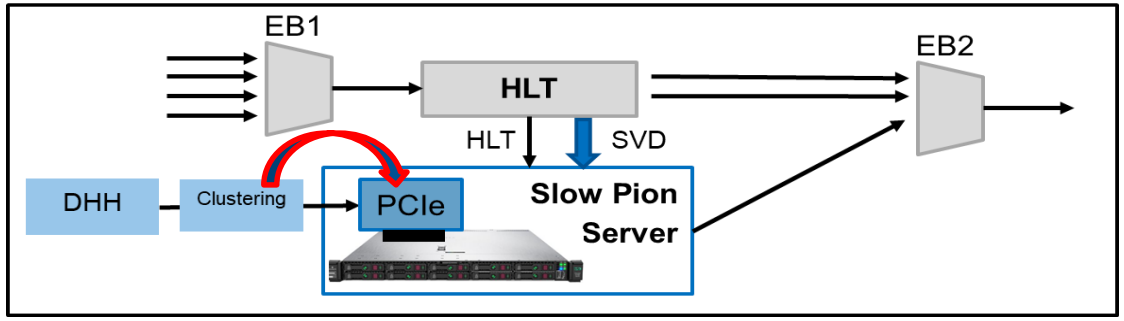
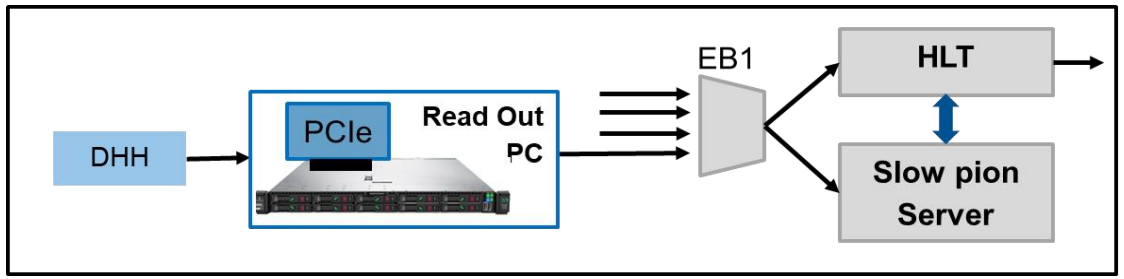


Comments
- Forwarding SVD data to PXD server
- **Preferable solution**
- **Clustering is done in PCIe FPGA**



Comments
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Single Server Configuration

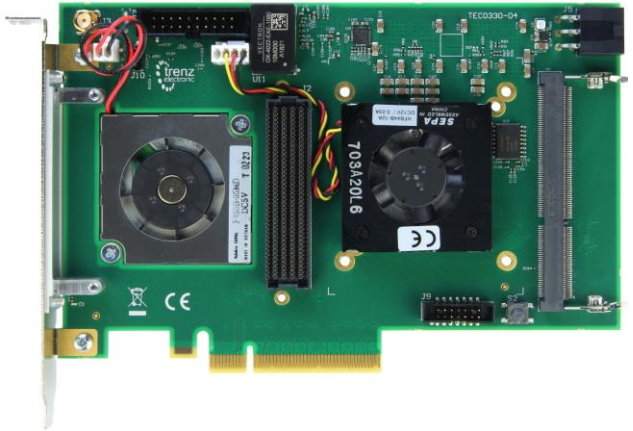
Hardware

PCIE Card from Trenz Electronics GmbH TEC0330

- FPGA Xilinx Virtex-7 XC7VX330T-2FFG1157C
- PCIE 8 lane Gen2, **3 GB/s**
- 8 GByte DDR3 memory
- FMC connector with 12 High speed interfaces

Server Dell PowerEdge R7515

- 1x7302 AMD CPU, 16 cores
- 128 GB DRAM, extendable to 512 GB
- M.2 SSD 1TB



Main PCIe FPGA functionality

- buffer
- Clustering
- Event building

Main server functionality

- DMA data transfer from PCIe to local memory
- Data buffering till HLT
- Data retrieving and ROI selection
- Interface to EB2

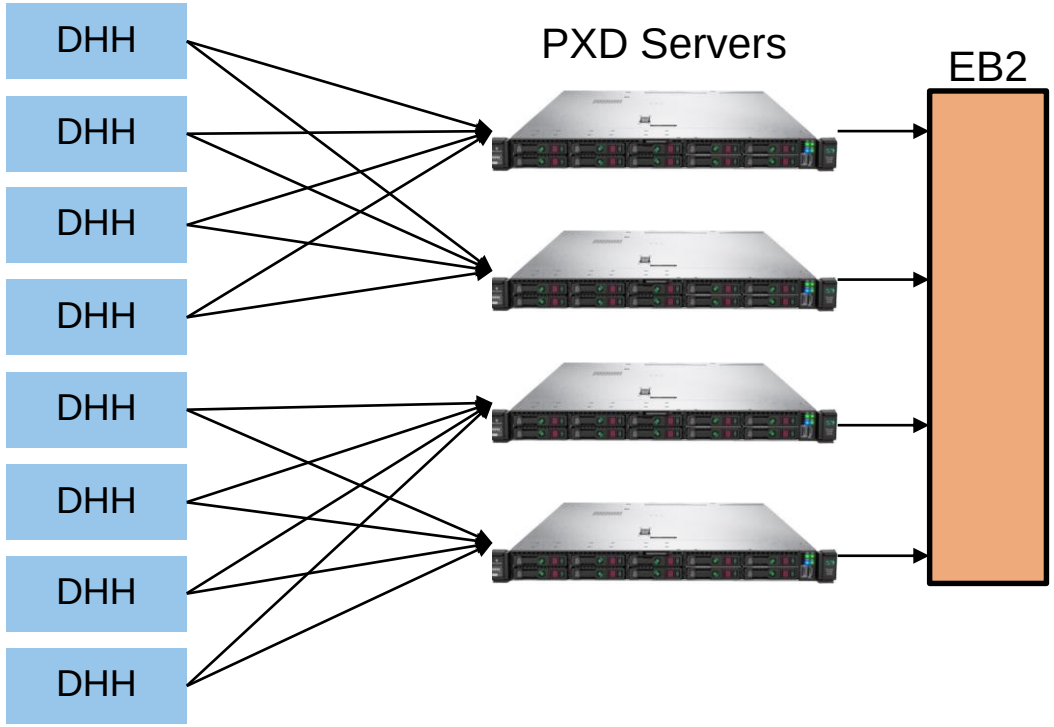
Full PXD Readout Architecture

Expected PXD data rate before LS2 is 3GB/s

Requirements for silicon only track reconstruction is unknown

Foreseen system

- 4x AMD Servers
- 4x PCIe cards
- The System is capable to process up to 8 GB/s



- How to proceed with project development still to be defined
- It shall be split in 2 steps :
  1. Demonstrator with single DHH and single server without slow pion recovery
  2. Full system

Next Steps for PXD Readout Upgrade

Man power status:

- Firmware development is in a good shape and can be finalized with available resources
- No manpower for software development and slow control

I will try to allocate some manpower within TUM group and I propose to discuss the project again at the next B2GM.

The upgrade has an impact on Belle II DAQ data flow thus it's important that propse changes improve DAQ performance and the project is considered important by DAQ group.

In case of positive progress with previous actions the following steps shall be foreseen;

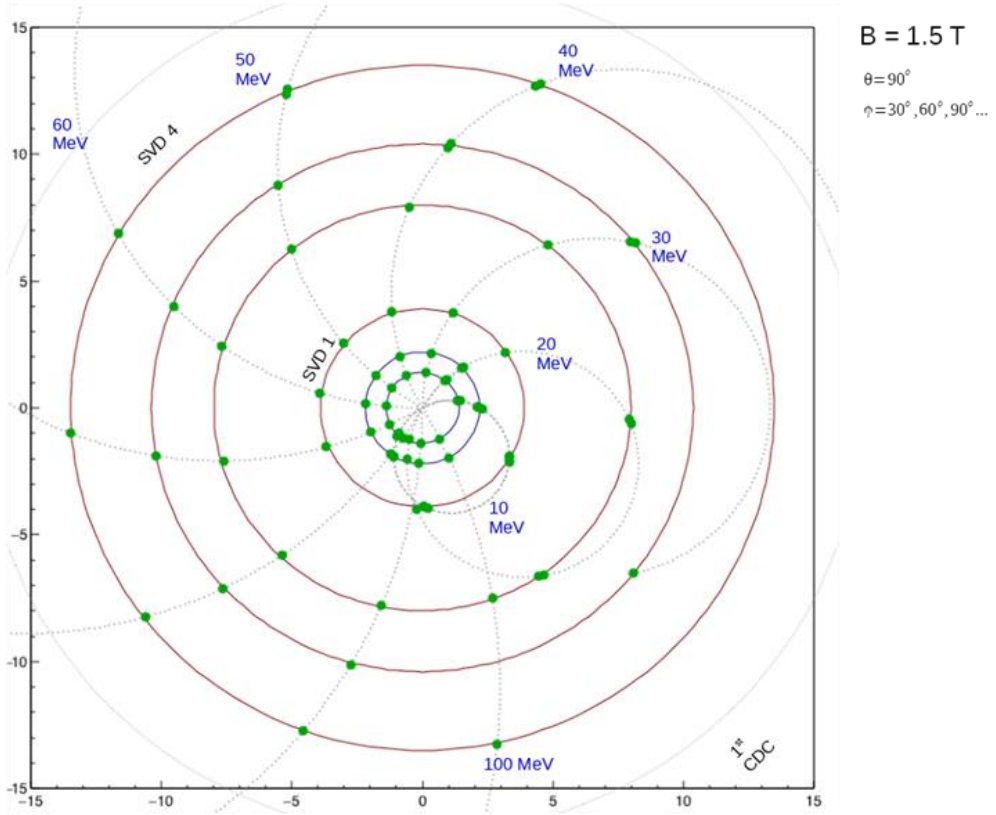
1. Integrate demonstrator with single DHH and single server without slow pion recovery algorithm. This step will be done without interference with existing system
2. Review project and decide whether to proceed further to full upgrade or stop here
3. Full upgrade if decided

Slow Pion Recovery Development

Sergei Gerassimov is working on Silicon Only track reconstruction algorithm

The goal is to reconstruct tracks with momentum < 50MeV

VXD



Sergei studies performance of following algorithms:

1) Kalman fit tree search with PXD based seeds.

2) Pattern matching.

3) Cellular automaton.

4) “Image” recognition with Machine Learning

Summary

- DHHCC upgrade is in progress. It will double DHH bandwidth and allow to read detector with maximum detector occupancy at 30 kHz trigger rate
- Commissioning of new data throttling algorithm is foreseen. The algorithm will make PXD readout stable regardless of occupancy and external VETO timing.
- Upgrade of PXD readout will provide infrastructure for slow pion reconstruction. At the moment the project has manpower problem.
- Work on Silicon Only track reconstruction algorithm is in progress.

THANK YOU

PXD Occupancy and Data Rate

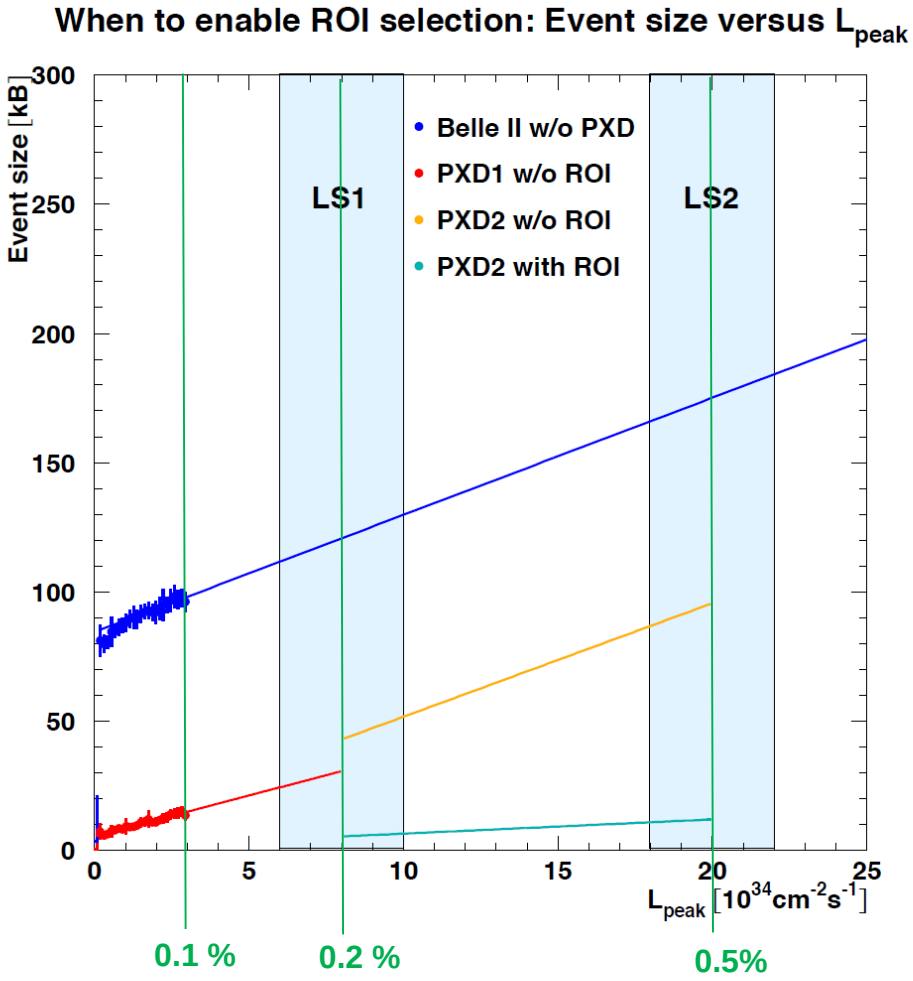
Detector occupancy in 2021 runs

- 0.1 % => 15 kB/ev => 150MB/s @ 10kHz before HLT

Expectations before LS2 @ $2 \cdot 10^{35}$

- 0.5 % => 100 kB/ev => 3 GB/s @ 30kHz before HLT

Expected that fraction of PXD data wo ROI will grow from 10% to 60% to compare to all other detectors before LS2



Occupancy ⇔ Data Rate

Bandwidth => Maximum data rate

- 20 us => 4 x 150 * 20 = 12kB/frame => 6.2kB (0.8%) + 5.8kB (1.5%) => 2.3%

Event size

- 384 Hits/frame encoded by 4 bytes/hit; > 384 Hits/frame encoded by 2 bytes/hit
- Occupancy at 4 bytes encoding: 384*4/(768*250) = 0.8%
- Occupancy => Event Size

	Single DHH		Full DHH	20kHz	30kHz
0.8 % => 384*4*4 = 6.2 kB/half ladder	6.2kB*5	= 31 kB	31kB*8= 250 kB	5.0 GB/s	7.5 GB/s
1.0 % => 6.2 kB + 192k*0.002*2 = 7kB/ev	7kB*5	= 35 kB	35kB*8= 280 kB	5.6 GB/s	8.4 GB/s
2.0 % => 6.2 kB + 192k*0.012*2 = 11kB/ev	11kB*5	= 55 kB	55kB*8= 440 kB	8.8 GB/s	13.2 GB/s
2.3 % => 6.2 kB + 192k*0.015*2 = 12kB/ev	12kB*5	= 60 kB	60kB*8= 480 kB	9.6 GB/s	14.4 GB/s

Realistic event size

2-d layer occupancy < 0.5 * 1-t layer occupancy				
Maximum Event size 2% 1-t layer, 1% 2-d layer	2*11kB+3*7kB = 43 kB	43kB*8= 350 kB	7.0 GB/s	10.5 GB/s
Real Event size 1% 1-t layer, 0.5% 2-d layer	2*7kB+3*3.8kB = 25 kB	25kB*8= 200 kB	4.0 GB/s	6.0 GB/s