TRG upgrade
2022/12/2
T.Koga

Motivation

-TRG upgrade plan in LS2 and beyond

- -VXDTRG
- -CDCTRG
- -ECLTRG
- -Increase latency
- -(UT5)

VXDTRG

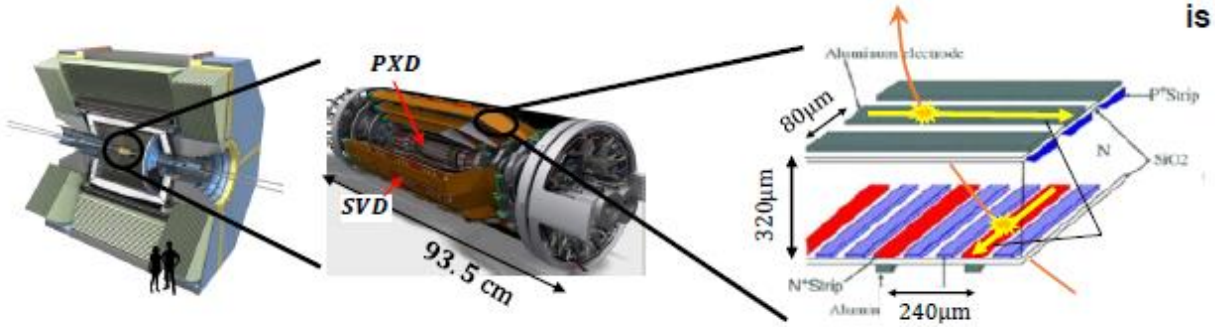
-With VXD upgrade, we can implement VXDTRG

-Purpose: beamBG rejection with |z| measurement

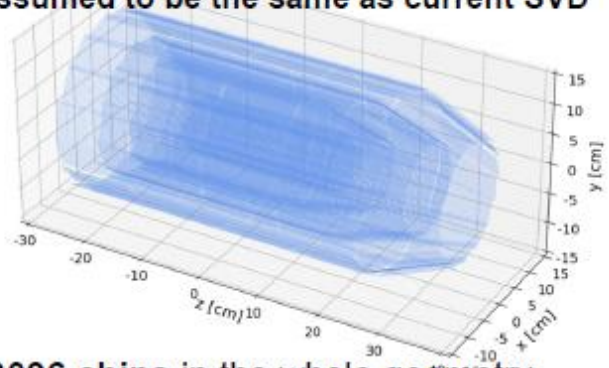
-R&D of VXDTRG logic is on-going with TFP-SVD by Shimasaki-san

SVD

- the double-sided silicon-strip detector located in the innermost part of Belle II detector.
- detects the position through which the particle has passed.



For now, geometry of TFP-SVD is assumed to be the same as current SVD

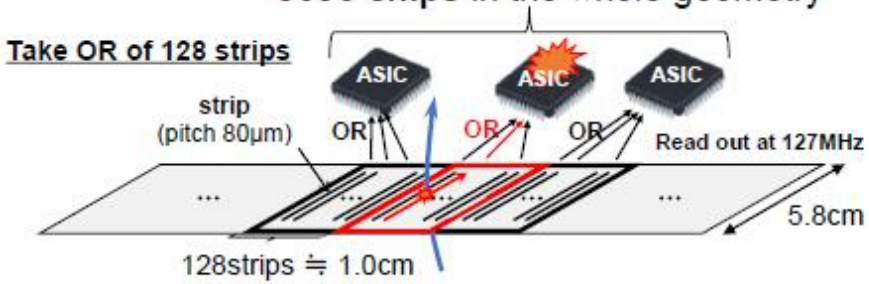


Thin Fine-Pitch SVD (TFP-SVD)

- We are developing new SVD to install after 2026.

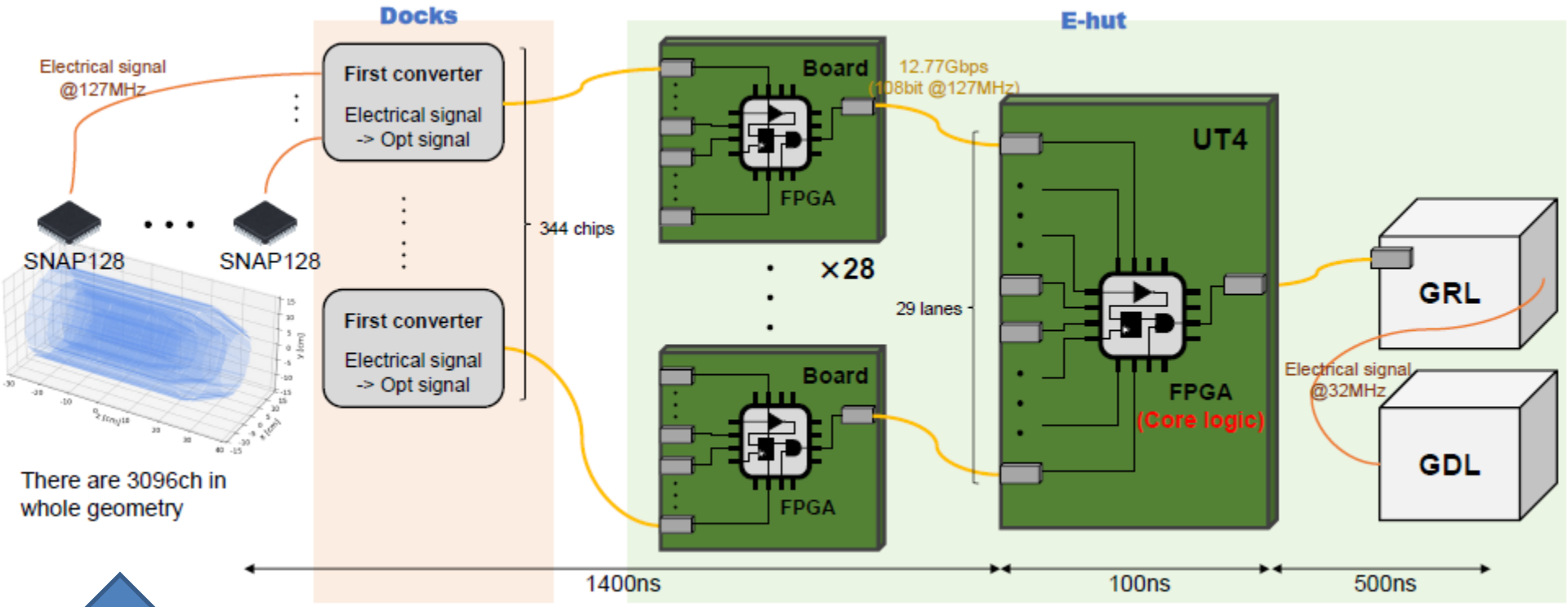
	Current SVD	TFP-SVD
pitch of P side strip	75 μm	75 μm
pitch of N side strip	160 or 240 μm	80 μm
Sampling rate	32 MHz	127 MHz
Generate TRG signal	No	Yes

3096 chips in the whole geometry



We are considering new L1 trigger using TFP-SVD

VXDTRG dataflow



detector

~300 converter board
electrical -> optical

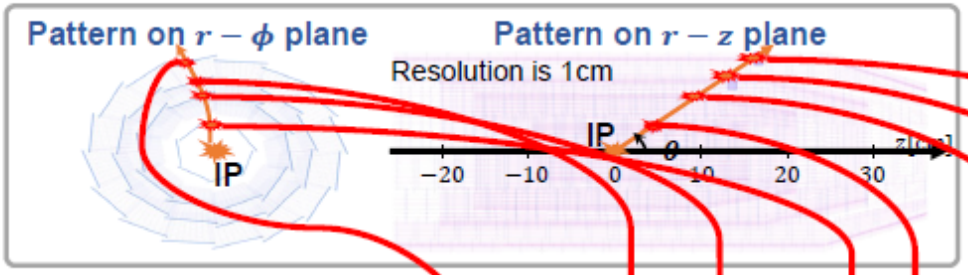
~30 Merger board

one UT4 board
for tracking

VXDTRG track reconstruction logic

Pattern matching by LOOK UP TABLE (LUT)

- Collect track patterns of particles from the IP.



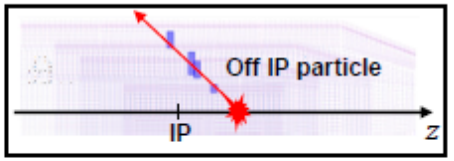
Encoded pattern table
[3096bits × 88,553]

Pattern 0: 100 ··· 001 ··· 010 ··· 001 ··· 100 ··· 010 ··· 100 ··· 001
Pattern 1: 100 ··· 010 ··· 100 ··· 100 ··· 010 ··· 010 ··· 010 ··· 100
Pattern 88552: 010 ··· 001 ··· 100 ··· 010 ··· 010 ··· 001 ··· 010 ··· 100

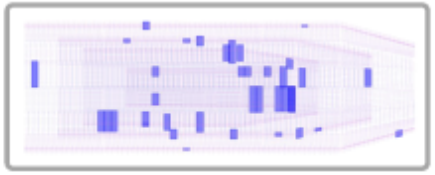
Conditions of particle generation for LUT

Parameter	Condition
Particle type	$\mu^{\pm}$
momentum p [GeV/c]	$0.2 \leq p \leq 3.0$
Production point z [cm]	$z = 0$

distinguish Off-IP track



- # of track pattern:88,553
- Each track is encoded in bit string with 3096-width



Online hits: Compare online hits with the table

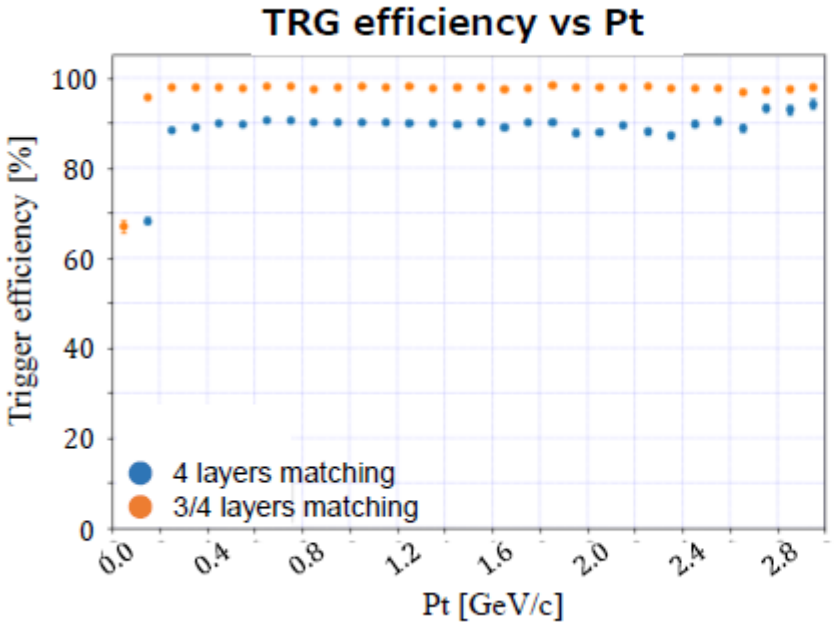
110 ··· 101 ··· 110 ··· 111 ··· 101 ··· 011 ··· 111 ··· 101

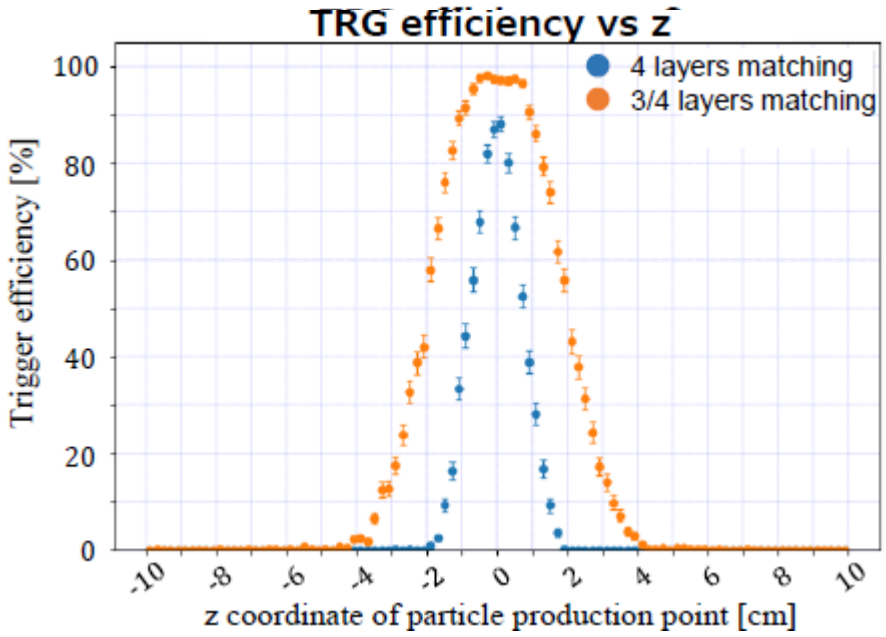
ex) this hits include the track pattern 0 of the table, and TFP-SVD trigger issue a trigger

VXDTRG expected performance

-Tracking performance is studied with a particle gun

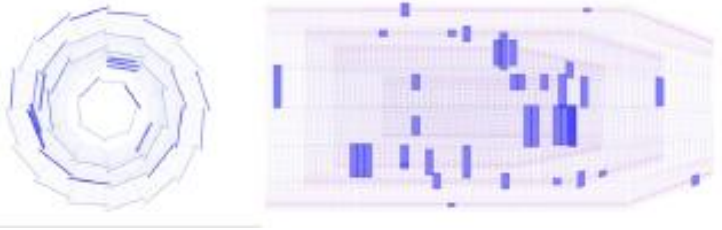
- -High efficiency
- -|z|< 2~4cm cut can be applied



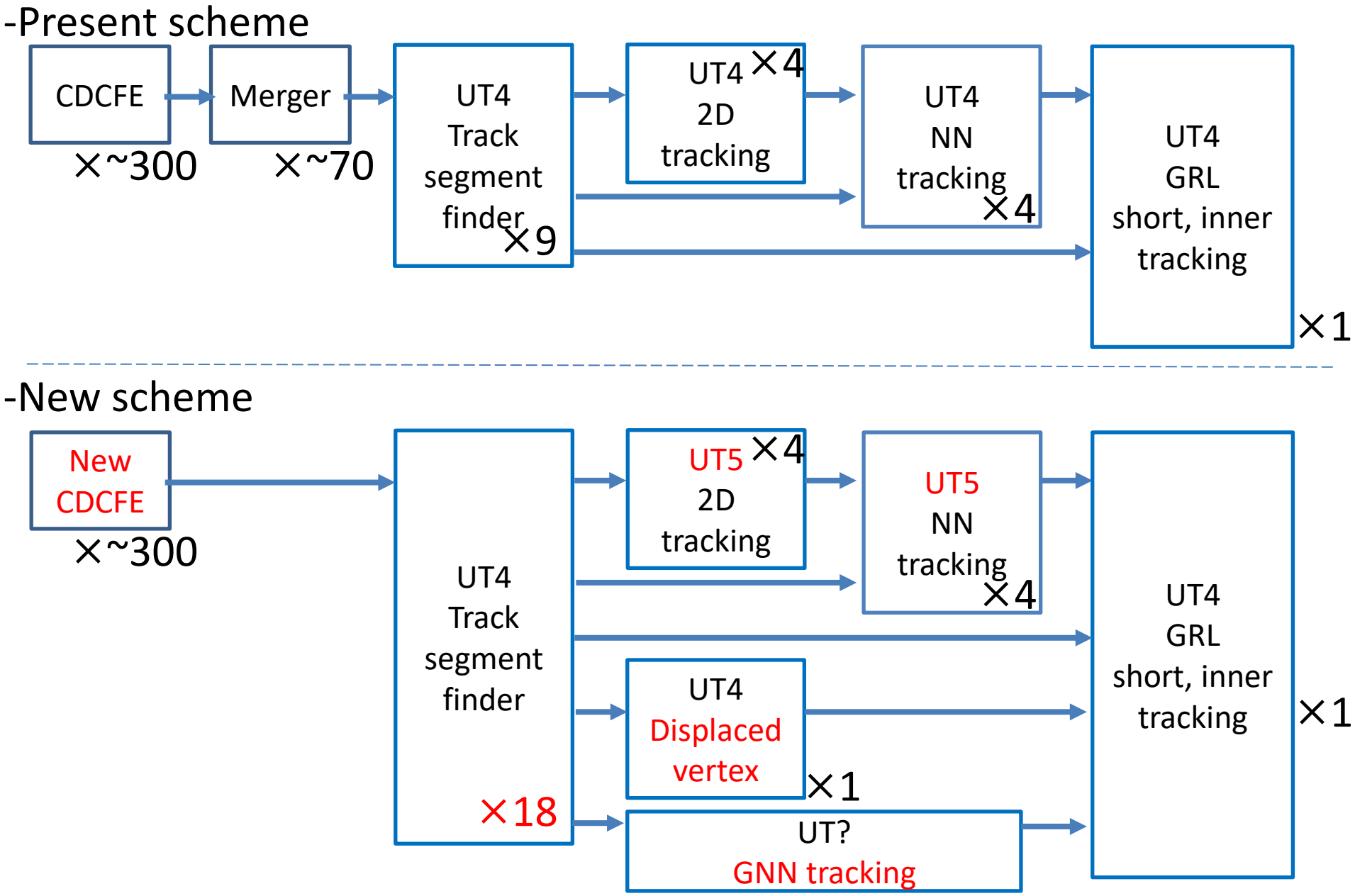


-Fake track probability is studied with beamBG MC

- -~1% fake track per 8ns with 4 layer matching
- -~10% fake track per 8ns with 3 layer matching



CDCTRG


-Present scheme
CDCFE
×~300
Merger
×~70
UT4
Track
segment
finder
×9
UT4
2D
tracking
×4
UT4
NN
tracking
×4
UT4
GRL
short, inner
tracking
×1
-New scheme
New
CDCFE
×~300
UT4
Track
segment
finder
×18
UT5
2D
tracking
×4
UT5
NN
tracking
×4
UT4
Displaced
vertex
×1
UT?
GNN tracking
UT4
GRL
short, inner
tracking
×1

Upgrade of CDCFE and CDCTRG

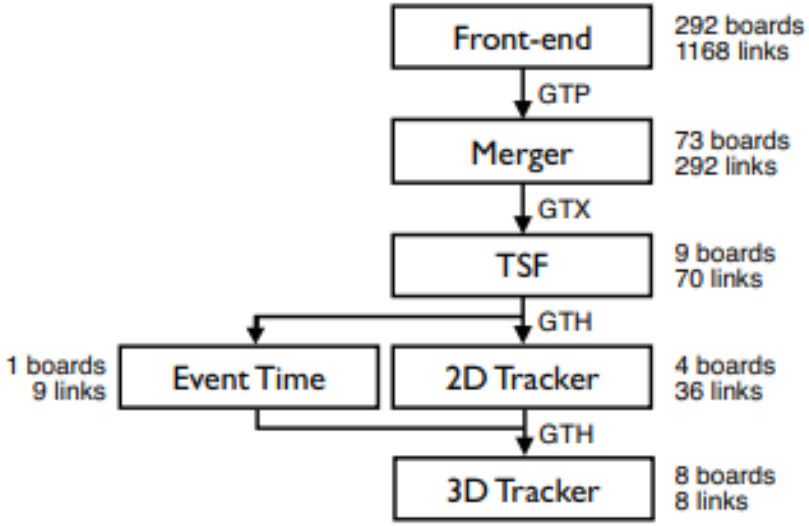
-Optical transceiver speed will be improved with new CDCFE

-To use the high speed, receiver side (MGR) need to be upgraded too

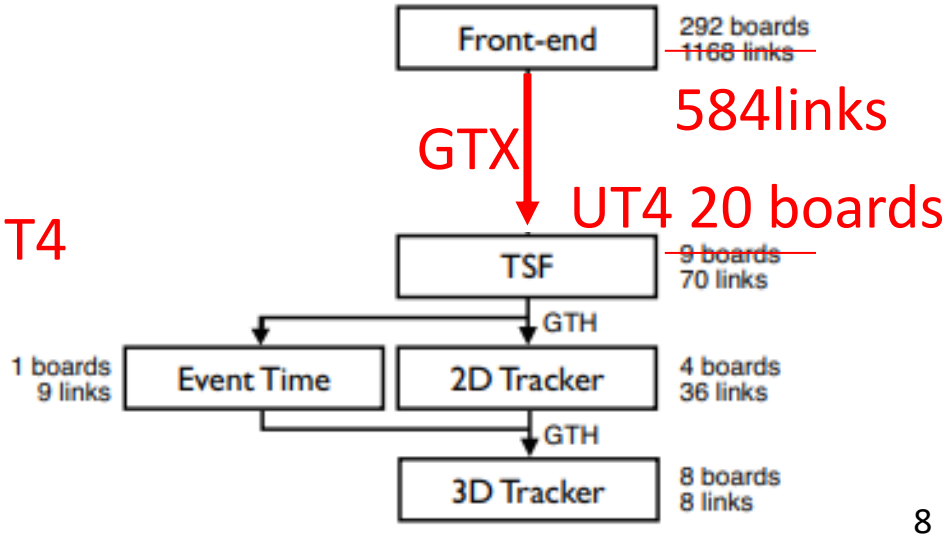
->We plan to bypass the MGR and connect TSF directly

	speed per lane	#lane per CDCFE<->TRG	#bit/32MHz/CDCFE
Present CDCFE	3.2Gbps (2.5Gbps with 8b10b)	4	256
New CDCFE	10.3Gbps (10Gbps with 64b66b)	2	512

Present configuration



New configuration



Merit of high speed

-With the higher speed, we can send TDC and ADC of all wires to CDCTRG

Figure 10: Part of CDC outer SL inside wire cell configuration [6].

Data from a CDCFE to CDCTRG

	data	#bit/32MHz/CDCFE
Present	-hitmap of 5/6 wires -tdc of part(~1/6) of wires (2ns) -fastest tdc among all wires -edge information -clock -total	48 (40)bit 5bit × 16wire=80 5bit × 16wire=80 10bit 9bit 227bit < 256bit
New	-hitmap of all wires -tdc of all wires (2ns) -adc of all wires (4bits) -clock -total	48bit 5bit × 48=240 4bit × 48=192 9bit 489bit < 512bit

Upgrade of trackers

-With the higher speed, we can send TDC and ADC of all wires to CDCTRG

-Great potential for BG reduction and efficiency improvement for future

-TDC: increase fitting points (x5) to improve z resolution

-ADC: crosstalk and noise reduction

-CDCTRG 2D track

●wire used for track fitting with tdc

CDC wire structure

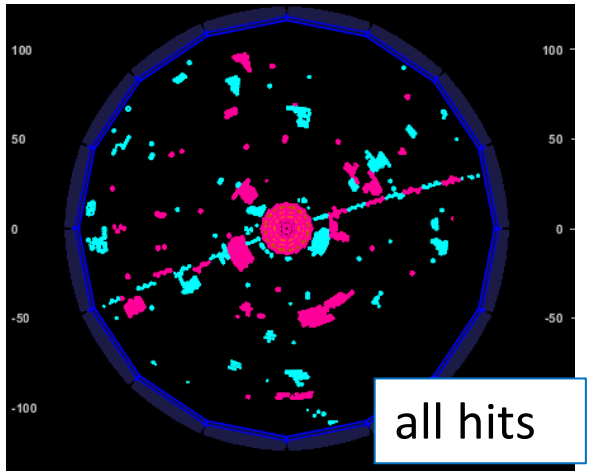
present fitting

new fitting
(LS1 and LS2)

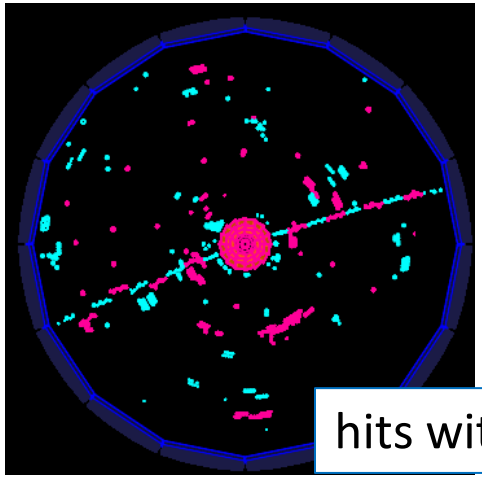
●axial

○stereo

◎
IP



all hits

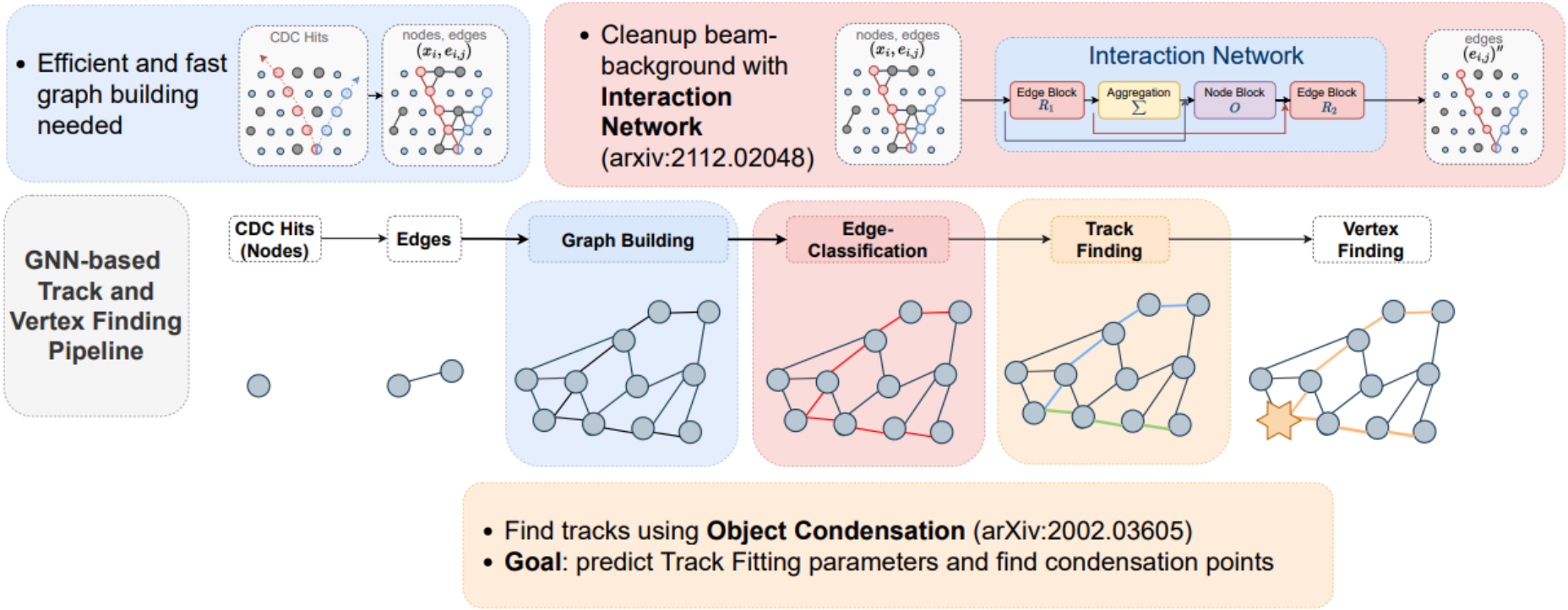


hits with ADC cut

CDCTRG GNN

-Lea and Philip started R&D of tracking and vertex finding with Graphical neural network

-With CDC wire, track finding, fitting and vertex finding are performed.



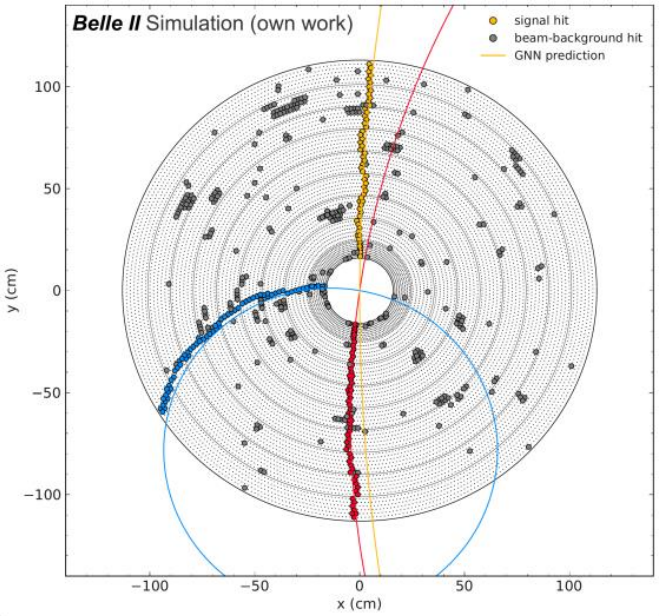
CDCTRG GNN

-Training and performance evaluation are on-going at offline at first, without think of level1 trigger constraint
(all CDC hits, ADC, TDC are used without considering latency and FPGA)

Found Tracks in Event	GNN (offline)[a]	TRGCDC2DFinderTracks	TRGCDCNeuroTracks	RecoTracks
Only signal tracks	91.5%	94.0%	93.8 %	90.6 %
Missing signal tracks	2.1 %	5.6 %	5.6 %	0.02 %
All signal tracks and additional tracks[a]	5.9 %	0.4 %	0.6 %	9.38 %
Missing signal tracks and additional tracks[b]	0.5%	0.01%	0.0 %	0.005 %
Per Track				
Efficiency	97.4%	94.4%	94.4%	99.98%
Precision	95.8 %	99.8%	99.7%	93.3%

-The offline tracking looks succeeded

-Plan to consider how to implement the logic to FPGA



ECLTRG

-Unno-san's talk

-During LS1, we plan to do performance evaluation of ECLTRG with future high luminosity and BG by using MC

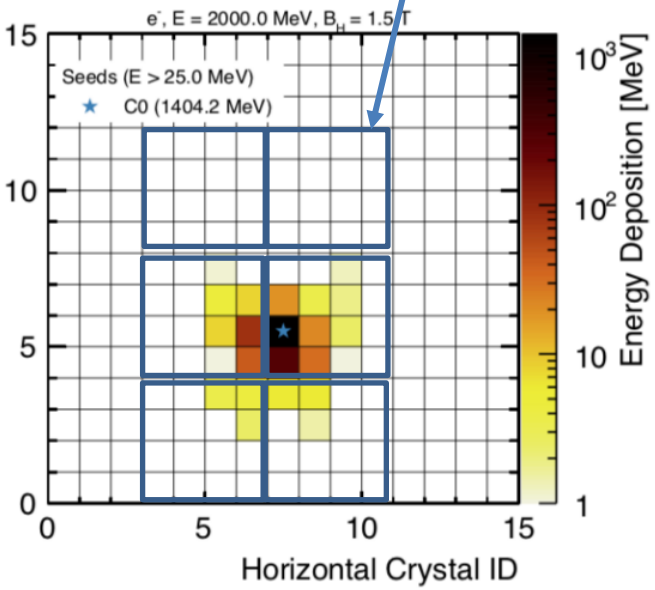
-Investigate possible issues, and determine long term upgrade plan to solve the bottolneck.

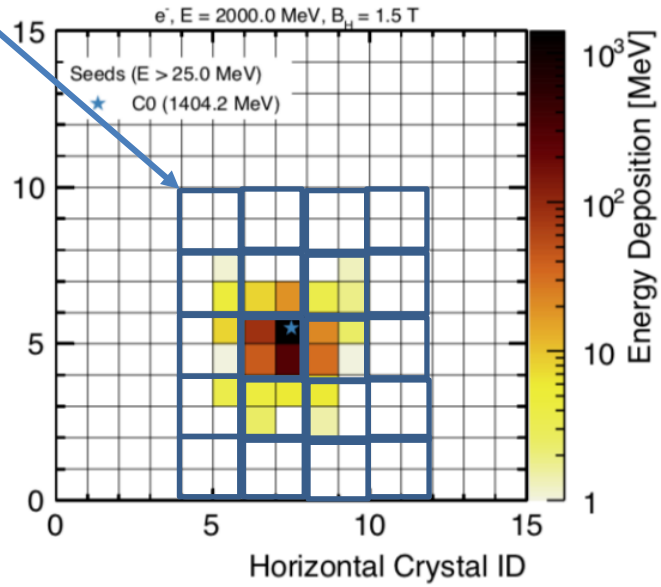
- Background study
  - BGOverlay logic for both MC and random data
  - Performance study for MC and data
  - Consistency study between MC and data
  - Based on the results, make a strategy for high luminosity and bkg conditions (for both after LS1 and LS2)

ECLTRG plan after LS1 and in LS2

- Try to separate two energy deposition in one TC (if necessary) ?
  - If two signal peak positions are >500ns, it would be possible

- New ShaperDSP ?
  - Currently 576 ShaperDSPs in 52 9-VMEs around Belle2 detector
  - Alex is planning to upgrade ShaperDSP
    - Some studies are in progress in BINP (the status not shown anywhere)
  - For ecl trigger, any requests and the meaningful improvement ?
    - "TC" timing can be improved if cell-by-cell timing adjustment in each TC is possible, but bad resolution is mainly from low energy TC
  - Any merit if logic of FAM can be implemented in new ShaperDSP ?
    - TC with from 4x4=16xtail to 2x2 if it improves some performance ?





L1 Latency

-Present L1 latency is limited by SVD

->If VXD is upgraded, we can enlarge latency.

If ~1μs latency increases, we can implement a UT4 for new logic.

-Next bottolneck is KLM RPC, ~5.2μs.

-FPGA resource of SCROD is occupied, and we are not sure if buffer size can increase or not (at present there is no FW expert)

-Need dedicated study, or upgrade of electronics.

Detector	Maximum L1 latency	Contacted Expert
PXD	※Rough estimation ~3times larger than now. At present 50 look back (unit=104ns) is used, it may go up to 191.	Bjoern Spruck
SVD	5.0μs (now) ~10μs in future with the upgrade of detector and FE	Katsuro Nakamura
CDC	~15μs+more, depending on FPGA resource and IP core	Yu Nakazawa
TOP	~9μs tested, just under 1 accelerator revolution = 10 μs should be possible, maybe 12 μs with larger FW changes. More would be very difficult without hardware upgrade, ring buffer has limited size.	Martin Bessner
ARICH	At present 56clk (1clk=15.7ns) depth buffer is used. The depth can increase depending on FPGA resource. We tested 112clk depth, it looks fine. Thus, 10~15 us latency is possible.	Yun-Tsung Lai, Kenta Uno
ECL		Mikhail Remnev, Alexander Kuzmin
KLM	16μs for scintillator 5.2μs for RPCs, need confirmation	Christopher Ketter

Summary

-TRG upgrade plan in LS2 and beyond

-VXDTRG

-add VXD to TRG with upgrade of VXD

-CDCTRG

-send ADC and TDC of all wires from new CDCFE to CDCTRG

-update of tsf, trackers

-GNN based tracking approarch

-ECLTRG

-perform simulation study for future high luminosity and BG during LS1 to consider possible upgrade in LS2

-with new shaper DSP, smaller size of TC can be used to get cluster shape

-Increase latency

-SVD is present bottolneck and KLM is the second. Need investigation for KLM.

backup

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-https://indico.belle2.org/event/1307/sessions/378/attachments/3070/5670/mmilesi_ECLPid_B2SKW_2020.pdf

4. Overview of ECL clustering

Simulation of single particles' energy deposition in a 15x15 ECL crystal array (pre-clustering):

γ	e	π	μ
• Radially symmetric shape • Usually contained in 5x5 cells	• Similar shape of γ • Less symmetric (B field bend, brems γ emitted before the ECL)	• Ionisation loss contained in 1-2 cells. • Asymmetric lateral spread due to hadronic interactions	• Pure MIP behaviour. • $\langle E_{cluster} \rangle$ ~ 200 MeV