New Technology for Data Transmission and Plans for UT5

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Belle II Trigger/DAQ workshop 2022 @ Nara Women's University

2nd Dec., 2022

Outline

- A brief overview for data transmission in HEP experiment
- Versal project in KEK and Japanese HEP community
- FPGA selection for UT5
- Other discussion
- Summary

Data transmission

- Transfer data from device A to device B.
  - Based on the selection of A and B, we have different options on the interface in between.

- If we transport guinea pigs, "guinea pig bridge" is a safe and convenient way:

source: youtube

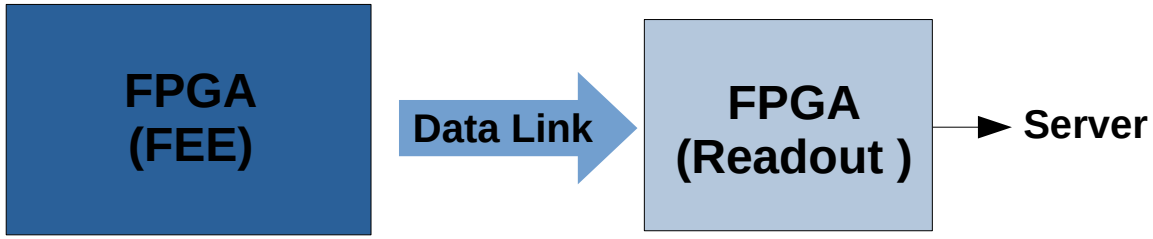
Data transmission in HEP experiment

- Two cases in general.

- **FPGA - FPGA:**
  - Optical link with FPGA MGT and optical modules.
  - Different encoding based on protocol design purposes.

- **FPGA - server:**
  - Data transmission and system slow control.
  - GbE, PCI-express, VME, etc.
  - PCI-express is the most popular one nowadays: PCIe40 in ALICE, LHCb, and Belle II.

- General studies on possible new options are helpful in the future.
  - But practically, a clear target or a chance is needed.

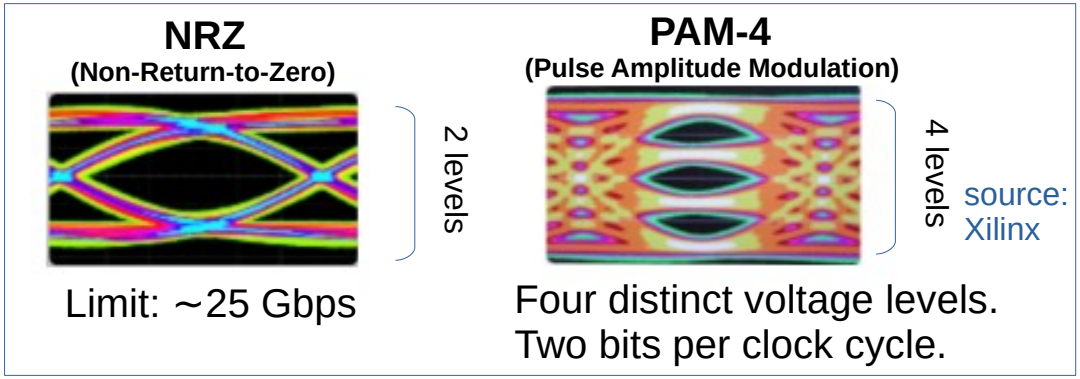


New thechnology for data transmission

- For the optical transmission between FPGA and FPGA.

- **NRZ:** Limit of line rate is 25~30 Gbps.
  - UT4 (UltraScale GTY) shows stable operation at < 16 Gbps.
  - Above it, bit error starts to occur frequently.
  - Similar result observed in ATLAS system due to their hardware device.

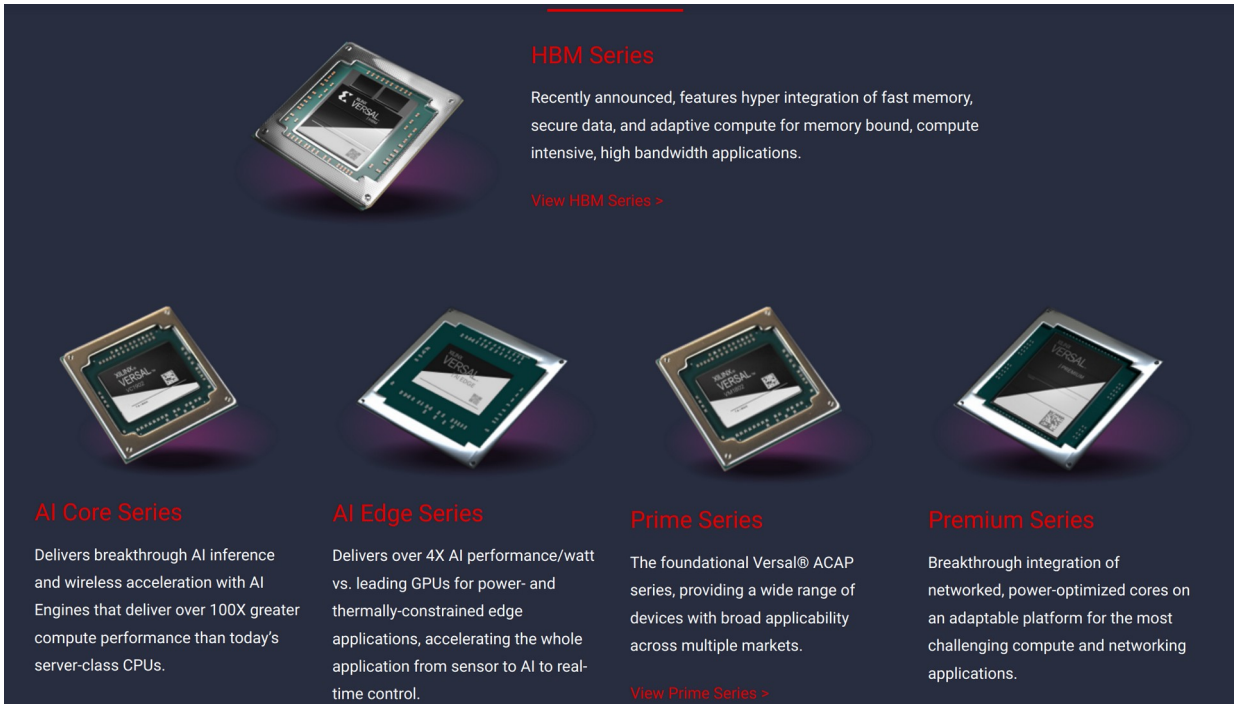
- **PAM-4:**
  - Four distinct voltage levels.
  - Application: higher error rate.
    Need careful firmware treatment:
    Gray code, new encoding,
    CDR, clock compensation.
  - Xilinx UltraScale+: up to 58 Gbps.
    Versal premium: up to 112 Gbps.
  - Need 4*100 Gbps QSFP.
  - Pioneer to study it in HEP community.
  - In addition, PCIe gen6 also utilizes PAM-4.



Versal project

- In KEK and Japanese HEP community, there is a Collider Electronics Forum for common and general studies on new associated technology for future development.\

- One of the plan is the Versal FPGA project.
  - Versal: One of the latest Xilinx FPGA generation.
  - We are able to purchase some evaluation kit for study purpose.

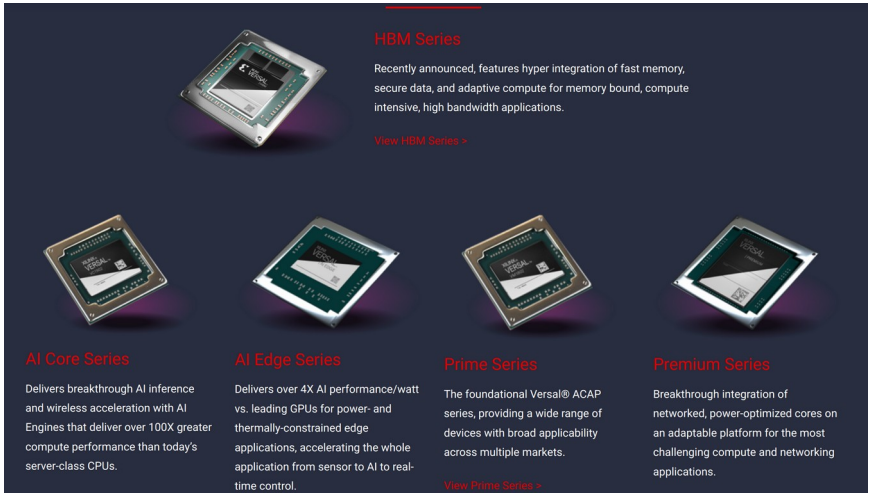


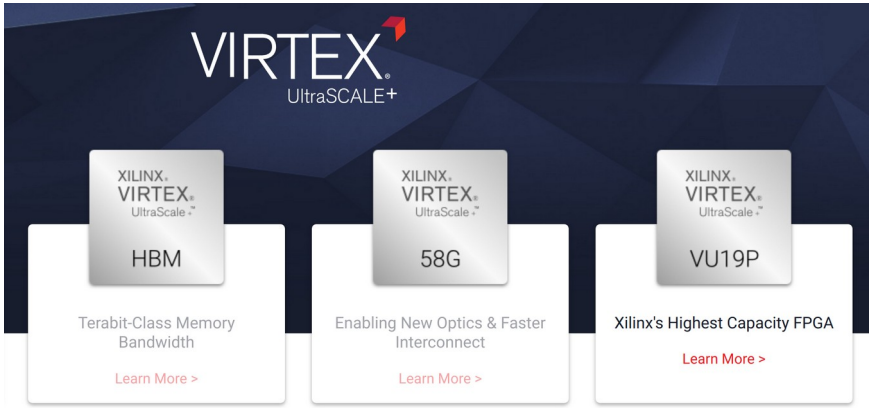
source: Xilinx website

Features of Versal and UltraScale+ series

- If we talk a look at both Xilinx Versal and UltraScale+, the features of different series:
  - AI engine: convenient interface to implement ML core into firmware.
  - High Bandwidth Memory (HBM).
  - FPGA with larger number of cells.
  - High bandwidth for data transmission.

- Each feature is orthogonal to each other.





source: Xilinx website

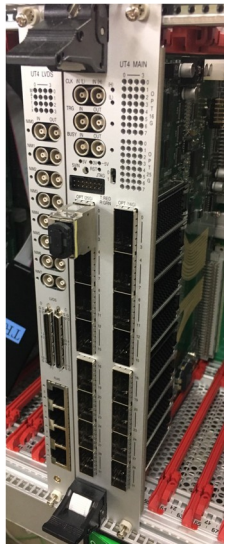
Belle II Universal Trigger boards

- Belle II Universal Trigger boards:
  - UT3: Xilinx Virtex-6, HX380T,565T
    - GTX 6.2 Gbps*40, GTH 11.2 Gbps*24.
  - UT4: Xilinx UltraScale, XCVU080, XCVU160
    - GTX 16 Gbps*40, GTY 25 Gbps*32.

- Interface:
  - QSFP optical link.
  - Lemo and RJ45 for clock input.
  - LVDS.
  - VME 6U: Power, slow control, flash memory access.

- Designed for general purpose to implement various L1 trigger algorithm.
  Have been working from phase 2.
  - Charged tracking (2D, 3D, Neural-3D), Calorimeter clustering, Event timing, muon chamber, global trigger, etc.

UT3



UT4

AVAGO
HFBR-7934WZ
3.125 Gbps/lane

AVAGO
AFBR-79Q4Z
10 Gbps/lane

Taiwan company
CENTERA
Photonics, Inc.
100G-SR4
25 Gbps/lane

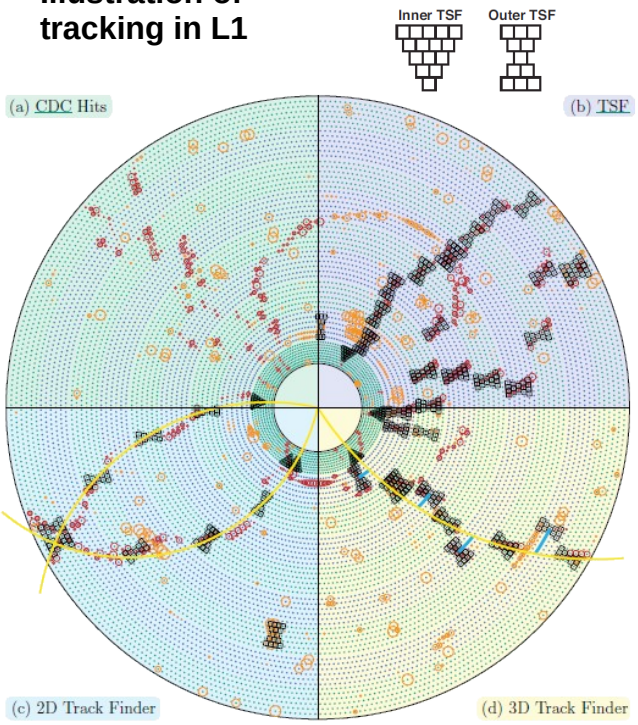
Consideration for the new UT

- Improvement on tracking is one of the plan with higher priority.
  - Not only for tracking.

- Present design:
  - 2D: Hough transformation using 5 axial SL of CDC.
  - 3D: Fitting method together with 4 stereo SL.
  - Neural-3D with pre-trained neuron in block-RAM in FPGA as LUT.

- For new ideas for tracking:
  - More wire info, including ADC, 3D Hough, track with displaced vertex etc.

Illustration of tracking in L1



Consideration for the new UT (cont'd)

- A simple summary in a perspective for TRG algorithm:

- If we want to make our HDL algorithm in the same way for finding/fitting:
  - Better precision, additional info, additional dimensions.
    - Larger FPGA and higher data transmission rate are desired.
    - Also, latency should be in the same level.

- If we want to utilize machine learning:
  - Just like the present Neural-3D in CDCTRG: Pre-trained neuron into FPGA LUT.
    - Large FPGA, larger memory (on-board or extended), or HBM are desired.
  - Implement the ML core using the new AI engine features.
    - FPGA series with those features are desired.

Consideration for the new UT by T. Koga-san

UT5 development idea

slide by T. Koga-san

-Fix issues on UT4
- -GTH laser is not working with 127MHz reference clock
- -VME communication is failed when UT4 is installed to VME crate
  - -failure rate increase with multiple UT4s in the same crate
- -Maximum optical speed is not achieved due to bit error or unstable link
  - -operated with ~half of maximum rate (12Gbps/10Gbps for GTY/GTH)

-New feature
- -Versal or Vertex Ultrascale+ FPGA ?
- -Large resource (~5-10 times larger than UT4)
- -High optical speed (25-60 Gbps?)
- -In the case of Versal, machine learning related feature
- -VME is OK in terms of power consumption? New platform is needed?
- -Can we develop the new board with ATLAS?

FPGA resource

FPGA	# of cells (K)
XC6VHX380T (UT3)	382
XC6VHX565T (UT3)	566
XCVU080 (UT4)	780
XCVU160 (UT4)	1621
Versal AI Edge	44-1139
Versal AI Core	540-1968
Versal Prime	329-2233
Versal Premium	833-7352
Versal HBM	3837-5631
UltraScale+ HBM	962-2852
UltraScale+ 58G	2252-3870
UltraScale+ VU19P	8938

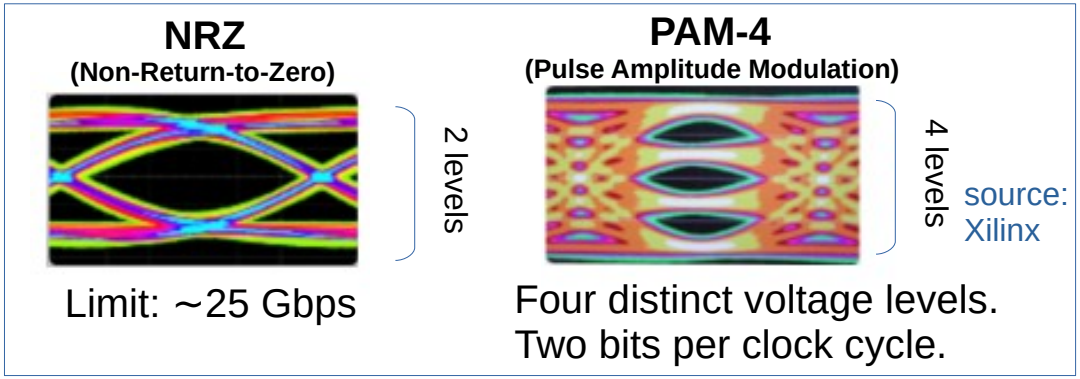
FPGA series with PAM-4

- If we would like to study PAM-4 using Xilinx evaluation kit: GTM transceiver supports PAM-4.
  - VPK120 kit with VP1202 FPGA of Versal Premium series.
    - GTM up to 112 Gbps using PAM-4.
    - GTM up to 58 Gbps for both NRZ or PAM-4.
    - PCIe 5.0 with GTYP.
  - VCU129 kit with VU29P FPGA of UltraScale+ 58G series.

VPK120
$11,994

VCU129
$17,994

- Good chance to perform general study on PAM-4 with the device
  - We can be the pioneer to use it in HEP experiments.
  - Design general-purpose protocol firmware: Lots of firmware work.
  - Helpful for experiments to reduce the time for development.



Other discussion

- PAM-4 could be a good option for new UT for L1 TRG.
  - Needs more considerations: Perhaps not in UT5, but in UT6.

- How about DAQ link (FEE → Readout)?
  - In present experiments: < 10 Gbps.
  - FEE: different considerations, such as # of detector channels, radiation tolerance, etc. So, FPGA is not required to be that large usually.
  - PAM-4 might be too early for DAQ link.
    - Its performance under irradiation environment is also an interesting study.
  - They study on PCIe 5,0 could be helpful for new readout device development.

- Still something to do for UT4: The limit of ~16 Gbps.
  - Further investigation on hardware (QSFP, GTY) and firmware (GTY IPcore), using oscilloscope, etc.
  - Custom encoder design.

- Other than GTM (with PAM-4):
  - https://www.xilinx.com/products/technology/high-speed-serial.html
  - Different options can be considered for UT.
    - Versal™ ACAP GTY (32.75Gb/s): Optimized for latency and power reduction.

Summary

- PAM-4: New technology for data transmission.
- The development of new UT for L1 TRG purpose:
  - Utilization of PAM-4: With Versal FPGA project.
  - For new UT, the selection on FPGA still requires various considerations.
- Other discussion:
  - What we can do with Versal FPGA, not only for new UT.
  - Still something to do with UT4.