FTSW4 development status

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Introduction

- **FTSW4**
  - Next generation FTSW with fully optical inter-rack connections
  - Compatible with FTSW3 for short CAT7 connections
  - Cost effective solution with low-end FPGA with maximal I/O
- **Outline of this talk**
  - Motivation
  - Part selection progress
  - Board layout plan
  - Use case for CDC FEE upgrade

Motivation

- **Solution to the CAT7 problem**
  - Up to ~100mV noise on inter-crate CAT7 cables (≤1m CAT7 is still fine)
  - No further improvement is expected, b2tt over fiber would be a solution
- **Upgrade opportunity for the new CDC FEE**
  - Large number of FEEs (299), unchanged
  - JTAG should be faster (now: 41M bits/FEE → new: 91M bits/FEE)
  - **Opportunity** to deliver b2tt to CDC FEEs over fibers, **if we have a high-density optical FTSW**
  - **Opportunity** to implement a backup route of clock, b2tt, belle2link on multi-port transceivers
- **By-products**
  - High-density optical FTSW can be directly connected to optical fiber version of PCIe40
  - Intermediate FTSW for KLM and ARICH may be removed
  - (need a new route to reprogram on-detector TOP FTSW3)

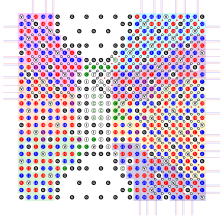
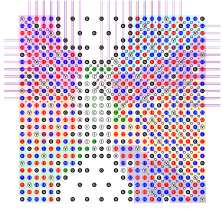
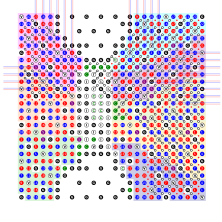
Part selection (FPGA and VME)

Except for FPGA, devices are chosen from those available in market stock

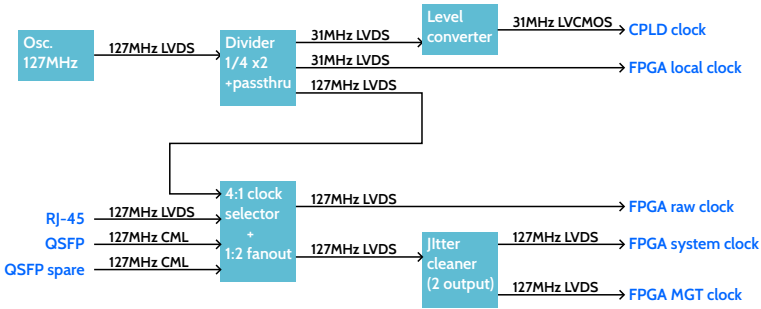
- **FPGA**
  - No Xilinx FPGA in the stock, need a VERY long delivery time
  - Large number of general I/O pin is needed
  - Considered: Spartan-7, Artix-7, Artix-Ultrascale+
  - Artix-7 has the largest number of I/O pins (400 pins), although it is still marginal
  - Choice: Artix-7 XC7A200T-1FBG676
  - 2 chips from unofficial market place in hand
  - 2 from official distributor to be delivered in May 2023
  - No secondary FPGA (simpler than FTSW3!)
- **Configuration flash memory**
  - Micron MT25QU128 (or other product)
- **CPLD and VME I/O**
  - XC95288XL-7TQG144C as a 5V tolerant CPLD for VME interface
  - 10-bit DIPSW to set the address
  - With just 5 more LVCMOS/TTL chips to form the VME interface

FPGA pin counting

- **Artix-7 I/O pins**
  - 400 I/O pins are divided into 8 banks × 50 pins (up to 24 LVDS pairs)
  - LVDS I/O requires 2.5V VCCIO, other I/O requires 3.3V VCCIO
- **LVDS pin counting**
  - Current design uses 118 LVDS pairs
  - In principle, they fit in 5 banks with 2.5V VCCIO, leaving 150 I/O pins with 3.3V VCCIO
  - Fully utilizing the pins is quite a challenge
    (below is one of my earlier trial, 98 LVDS pairs from 5 banks in 3 layers, not optimized)

Part selection (clocking)



- Oscillator: KDK KEM35AT-L 127.216MHz
- Divider+passthru: SY89873L
- Level converter: DS90LT012ATMF
- Selector (4:1) + fanout (1:2): SY89547LMG
- Jitter cleaner: CDCE62002

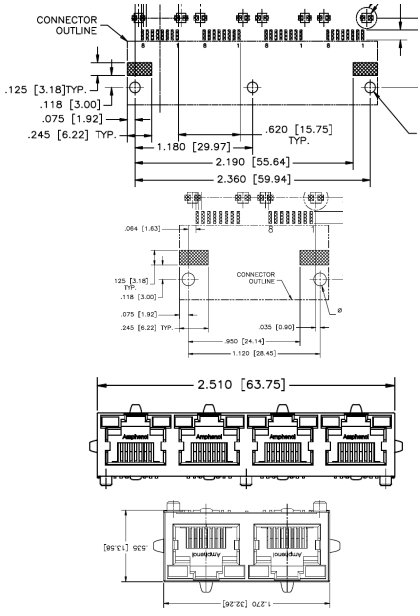
3.3V device only

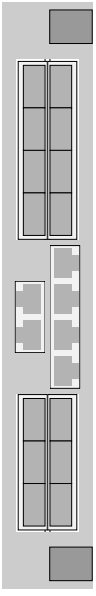
Part selection (power)

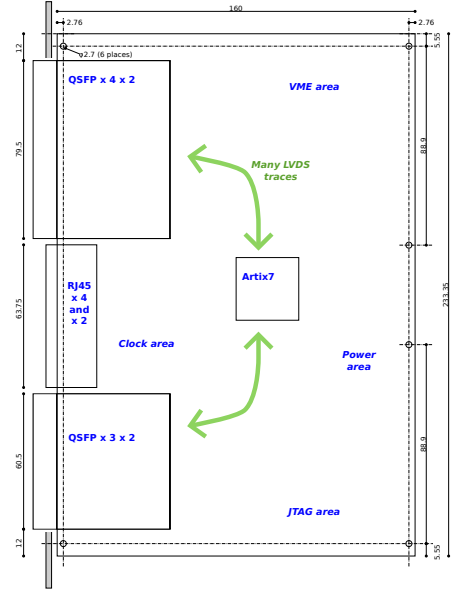
- **3.3V from 5V of VME**
  - Originally considering a DC-DC converter with multi-voltage output
  - Changing the design: use 3.3V only device other than FPGA
  - Confine the other voltages only near the FPGA
  - Large-current 3.3V DC-DC suggested by Dima: LMZ10505
- **External 3.3V**
  - Option to use J0 connector of KEK-VME, and from a on-board terminal (same as FTSW3)
- **2.5V, 1.8V, 1.2V, 1.0V**
  - Only for Artix-7, use reliable LDO regulators (same as or similar to FTSW3)
  - 2.5V (VCCIO for LVDS): LT1963
  - 1.8V (VCCAUX): LT1963 or LT1761
  - 1.2V (MGTAVTT): LT1963
  - 1.0V (VCCINT, MGTAVCC): TPS74401

Part selection (connector)

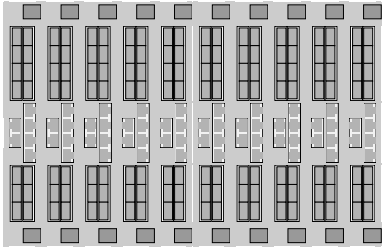
- **No optional daughter card (no FMC)**
- **QSFP**
  - Current trend is into high-end O(100Gbps) transmission
  - QSFP is probably the only available low-end multi-port transceiver
  - 2 QSFP cages can be mounted by a belly-to-belly configuration (to maximize the front panel area usage)
  - PC board has to be a bit thicker ($\geq$ 2.2mm, like FTOP, while standard is 1.6mm)
- **RJ-45**
  - Several RJ-45 ports are needed
  - Priority in maximizing the number of optical ports
  - No RJ-45 connector designed for belly-to-belly (only double-story RJ-45 connectors like FTSW3)
  - A solution found: 4-port RJ-45 and 2-port RJ-45 in belly-to-belly
- **Maximizing the number of ports**
  - 14 QSFP cages + 6 RJ-45 connectors
  - About the limit of the number of pins of Artix-7


CONNECTOR OUTLINE
.125 [3.18]TYP.
.118 [3.00]
.075 [1.92]
.245 [6.22] TYP.
.620 [15.75] TYP.
1.180 [29.97]
2.190 [55.64]
2.360 [59.94]
2.510 [63.75]




160
2.76
2.76
12
5.55
2.7 (6 places)
QSFP x 4 x 2
VME area
79.5
88.9
Many LVDS traces
Artix7
RJ45 x 4 and x 2
63.75
233.35
Clock area
Power area
QSFP x 3 x 2
60.5
88.9
JTAG area
12
5.55

FTSW4 crates for CDC



FTSW4 counting

- Minimum 19 FTSW4 modules to cover 300 CDC FEEs
  (7×3=21 FTSW4 modules is more logical configuration)
- 1 more FTSW4 in the main TTD crate to deliver signals
- 1 more FTSW3 to deliver JTAG signals to FTSW4
- 1 VME CPU for JTAG
- Fully packed 2 VME 6U crates,
  or more logical 3 VME 6U crate configuration

FTSW4 location

- FTSW4 can be located in E-hut (no length limitation of CAT7)
- FTSW4 on the detector will save the fiber cost, but less accessible
- One rack space for FTSW4 crates, and one rack space for patch panels
- MPO fiber (clock, b2tt, JTAG, b2link) directly from E-hut to FEE? (cabling would a lot simpler)

Quantity and Cost

- **Number of boards**
  - 20–22 FTSW4 for CDC
  - 1+1 FTSW4 for KLM+ARICH in E-hut to reduce 9 intermediate FTSW3
    (no real gain for the current FEEs of other subdetectors)
  - Produce 30 boards if no other FEE upgrade which adopts optical b2tt/jtag
- **Cost estimate**
  - FPGA ∼ 500 USD per module
  - Connectors ∼ 300 USD / module
  - Oscillator → need to purchase a reel for CDC (8000 USD total)
  - Power chips ∼ 100 USD / module
  - Clock chips ∼ 50 USD / module
  - Passive parts and extra parts for JTAG to be estimated
  - QSFP modules ∼ 1,000 USD / module
  - Front panel ∼ 50 USD / module
  - PC board and assembly ∼ 500 USD per board
  - Total: ∼ 2,500 USD per board, 75,000 USD total (?)
  - (MPO fibers and CDC patch panel are not included)

Plan

- **FPGA pin counting needs a bit more work**
  - Priority since it may affects the part selection
  - Need to allocate time to concentrate
- **Start buying parts**
  - Clock related parts may disappear from market stock
  - Not much budget of this FYl left
- **JTAG needs more work**
  - JTAG-over-b2tt should be avoided for new CDC FEE
  - JTAG-over-optjtag to be driven by FTSW4, but need more thinking
- **More work on details**
  - Ethernet option (both optical and RJ-45)
  - Passive components, especially on noise mitigation
- **Schematics**
  - Maybe towards the end of the FY or beginning of next FY