ARICH requirement for high rate/triggerless DAQ

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Limitation of trigger rate

ARICH FEB

- Sends data to merger using 4 lines with 63.6 MHz clock.
  - Event size: 4 bit/ch * 144ch + 80 (header) = 656 bit.

  → 164 clocks to send one event.

HAPD : 144 ch

FEB condition

- Issue maximum 10 triggers within 26.4 us.
  - ARICH fully relies on this condition

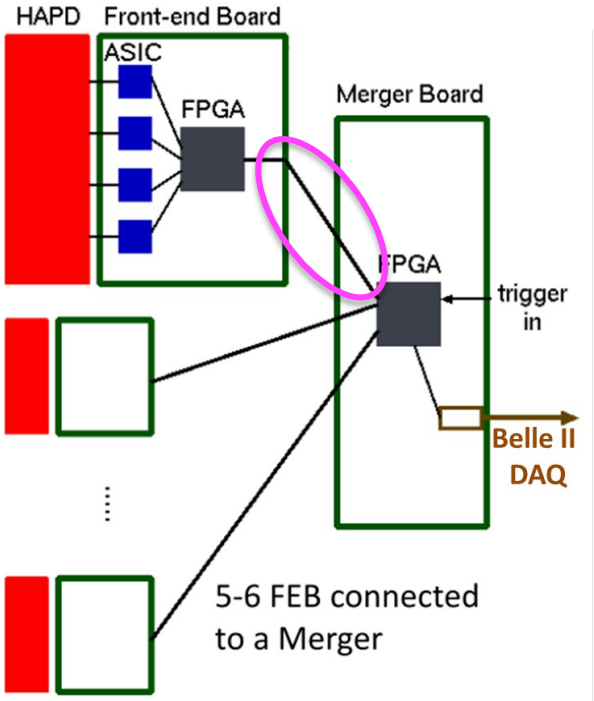
  → Overflow never happens

→ $f = 1.0/(26.4/10) \sim 380$ kHz is the limit

※ **Difficult to remove this condition**

- A lot of modification (firmware) is needed

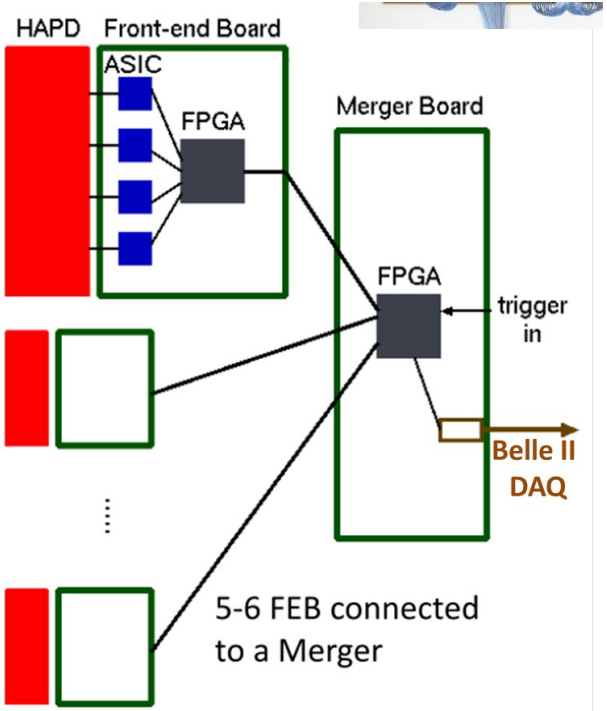
→ **Triggerless readout is not possible**



Event size

Header

※ARICH: 420 FEB, 72 Merger Board



- 12 bytes merger header per merger
- 22 bytes FEB header per FEB
- Belle2Link header: 36 bytes per Belle2Link.

Data per FEB

- Raw mode: 4 * 144 bit = 72 bytes FEB data
- Suppressed mode: 2C bytes (C: #channels with hit)

Event Size:

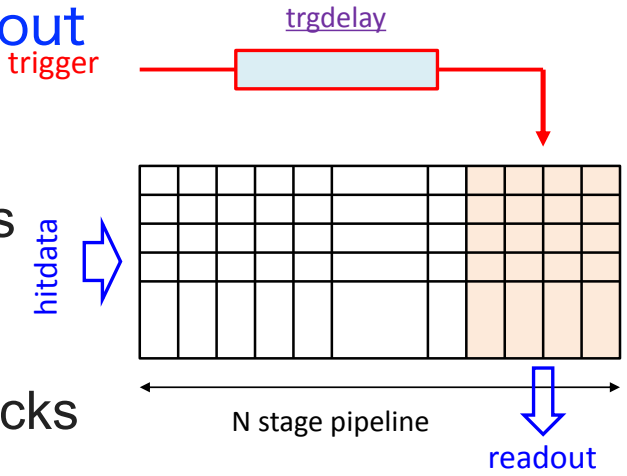
- Raw mode: 12 * 72 + 36 * 72 + (22 + 72) * 420 ~ 43 kB
- Suppressed mode: 12 * 72 + 36 * 72 + (22 + C) * 420 ~ (13+0.4C) kB
  - C: average #hits per HAPD. Typically, C < 1 → <15 kB

Large part of the data is header

This is necessary to check the consistency of the FEB data
→ No plan to change the format.

Limit/Improvement of FEE

Internal logic of the FPGA for the hitdata readout



- System clock is 63.6 MHz (1 clock = 15.7 ns)
- Data inside pipeline is shifted every hdcycle clocks
- Pipeline has N stage, where N = 56
- Trigger signal is delayed by trigdelay * hdcycle clocks
- Last 4 stages of the pipeline are read out

→ Hit data is kept for ~(N - 2 - trgdelay) * hdcycle * 15.7 ns

Current FEE (N = 56, hdcycle = 8, trigdelay = 16) → Keep data for ~ 5.0 us

Consideration

- Increase the depth, N (Already confirmed firmware with N=116 works)
  - 10 us latency is possible
- Option to reduce time window to be more tolerant to beam bkg

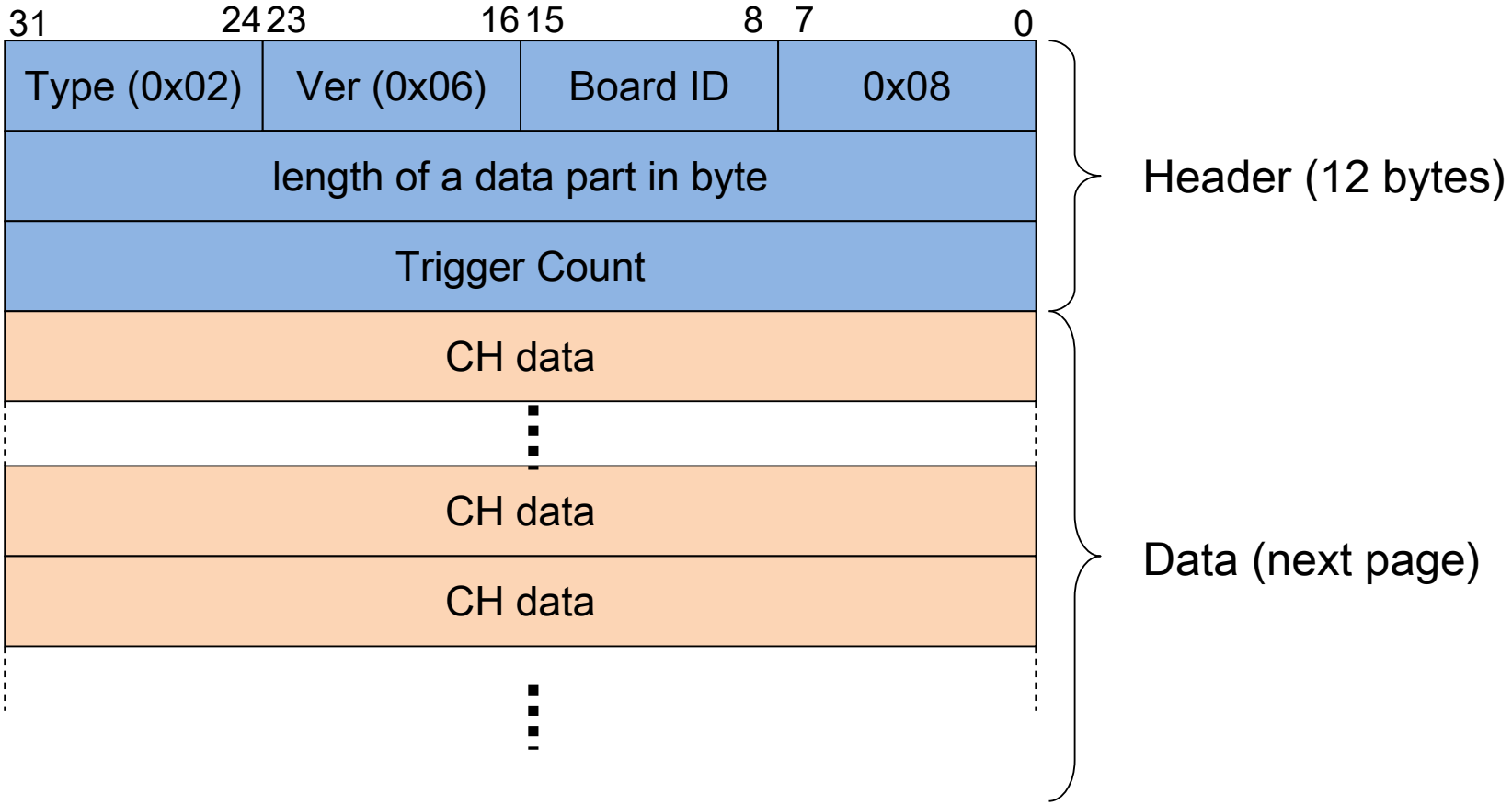
  → If we adopt 10 us, it's difficult to adopt this option

Backup

Nishida-san's slide

ARICH Data Format

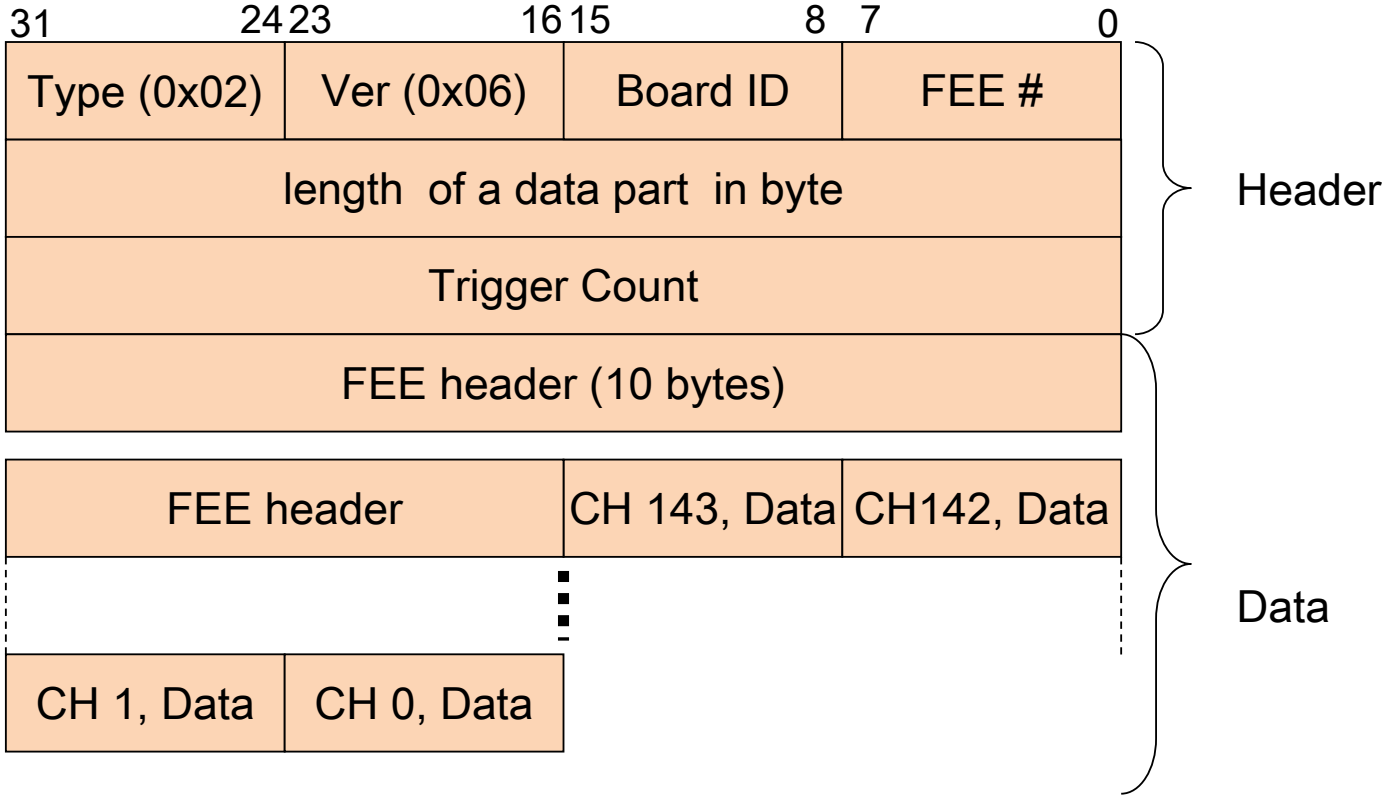
Data format from one Merger Board (= one Belle2Link).



Nishida-san's slide

ARICH Data Format

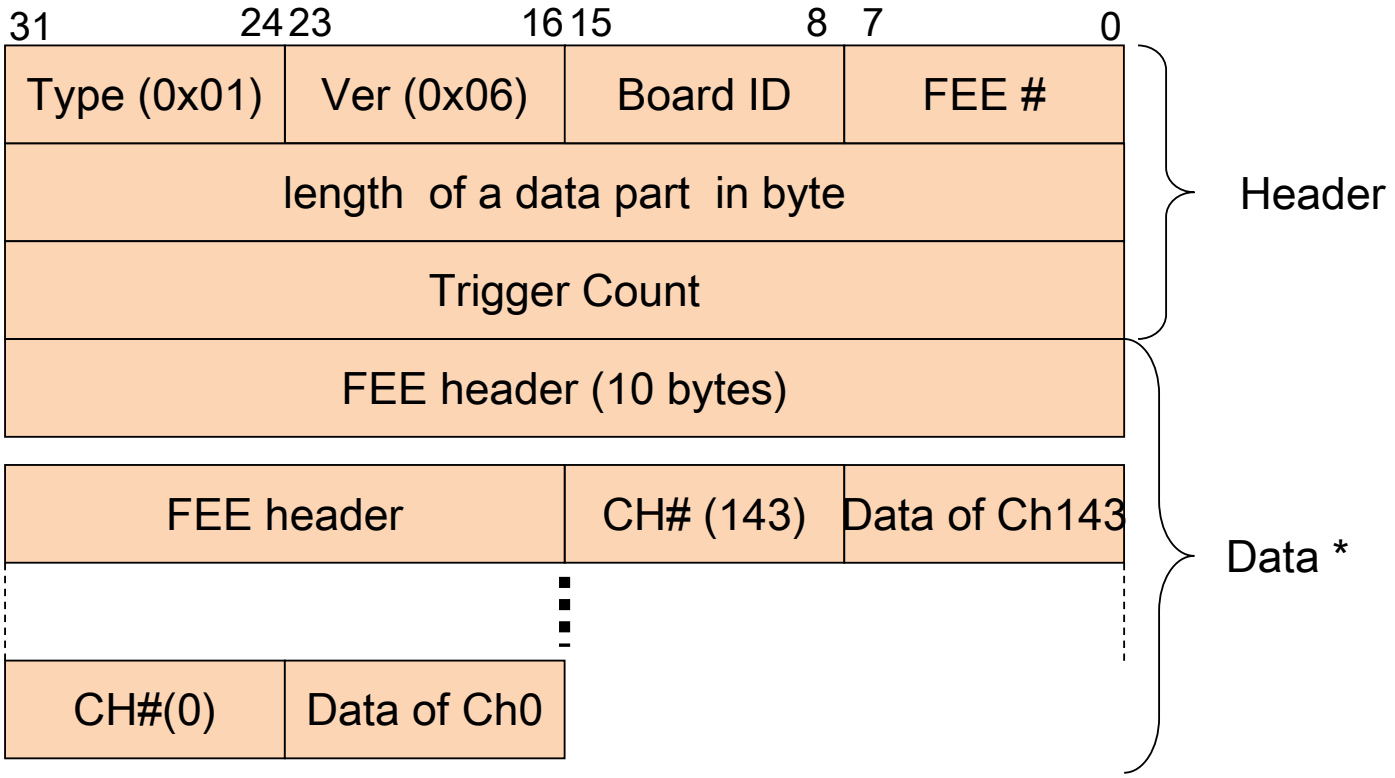
CH Data in Raw Mode



Nishida-san's slide

ARICH Data Format

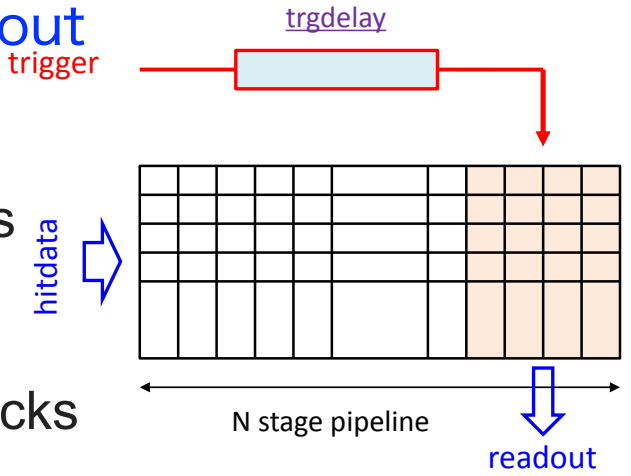
CH Data in Suppressed Mode



* If a ch has no hit data (Zero), its data is not transmitted.

Limit/Improvement of FEE

Internal logic of the FPGA for the hitdata readout



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Current FEE (N = 56, hdcycle = 8, trigdelay = 16) → Keep data for ~ 5.0 us

Plan

- Increase the depth, N (Already confirmed firmware with N=116 works)
- Shorter time window (hdcycle) depending on beam background

→ 10 us latency is possible by updating firmware