Mics. for Merger and data flow

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Outline

- Merger firmware update
- Data link
- Summary

Merger firmware's recent udpate

- v2.49 → v2.50

- Features:
  - Masking on single FE input channel.
  - Improve the timing condition of firmware.

- In the cosmic run last weekend, new firmware was downloaded to SL0,1,2, and the 2D tracking rate looks the same.
  Stability of optical links also looks fine.
  - Ready to update the flash for all Mergers.
  - Start to do it in Dec.?
  - Koga-san borrowed some Intel JTag cable.
    Will also try to use it.

CDCFEE → Merger → TSF data link

- The present design:
  - CDCFEE → Merger: 2.54 Gbps, 127 MHz useurclk, 1-4 FIFO.
  - Merger → TSF: 5.08 Gbps, 254 MHz, 1-8 FIFO.

- We tried higher speed but gave up ~10 years ago.
  - Data corruption in Merger → TSF: Lack of knowledge for timing violation.
  - UT3 GTH does not allow such line rate.

- The new design:
  - CDCFEE → Merger: 3.175 Gbps, 158.75 MHz useurclk, 1-5 FIFO.
  - Merger → TSF: 6.35 Gbps, 317.5 MHz, 1-10 FIFO.
  - 256 bits → 320 bits: Hope that it is helpful for the new ADC-based CDCTRG.

- Higher speed Merger → TSF link could be a headache
  - Fast userclk: Need careful treatment on timing condition.
  - Double data path width (16 bits → 32 bits) could be an option for development.

- A short-term project: Try to finish it within few months.
  - Update can be done together with the ADC-based version of firmware.
  - Need to set up a test bench (FEE+Merger) in B2. Will talk to relevant people.

UT4 data link: Try higher speed

- We are using the data link up to 16.764 Gbps in CDCTRG now.
- Limit of GTY is ~25 Gbps, but we could not reach higher than 16 Gbps.
- Also a short-term project which is worth trying.
  - Other option of encoding?
  - Try self-defined encoder module?
  - Check the eye-diagram of hardware-level signals? No optical oscilloscope.
  - Check the eye-diagram by iBERT with different setups/encoding.

Line rate (Gbps)	data path width (bit)	userclk (MHz)	FIFO (dataclk)	FIFO (sysclk)	data/lane with dataclk (bit)	data/lane with sysclk (bit)	
5.588	64 (66)	84.67	3-8	3-2	170	42	
11.176	64 (66)	169.33	3-16	3-4	340	85	
8.382	64 (66)	127	1-4	1-1	256	64	
12.573	64 (66)	190.5	1-6	2-3	384	96	**We are using it**
16.764	64 (66)	254	1-8	1-2	512	128	**BER exists**
25.146	64 (66)	381	1-12	1-3	768	192	**Frequent BER**
18.8595	64 (66)		1-9		576		**Not supported**
20.955	64 (66)		1-10		640		
23.0505	64 (66)		1-11		704		

UT4 data link

- FIFO-bypassing design for 8.38 Gbps is tried?
- I think some TRG firmwares will move to use 12.57 Gbps setup.
  - Please let me know if you need help in your implementation.

CDCTRG: 32 MHz dataclk

Latency (sysclk)	Total
UT3 5.58 Gbps	54 (420 ns)
UT4 5.58 Gbps	66 (515 ns)
UT4 8.38 Gbps	46 (359 ns)
UT4 8.38 Gbps no TXFIFO	39 (304 ns)
UT4 8.38 Gbps no TX, RXFIFO	28 (218 ns)
UT4 12.57 Gbps	40 (312 ns) ←
UT4 16.76 Gbps	32 (250 ns)

TOP-GRL-GDL: 127 MHz sysclk

Latency (sysclk)	Total
UT3 5.58 Gbps	~450 ns
UT4 5.58 Gbps	64 (500 ns)
UT4 8.38 Gbps	44 (343 ns)
UT4 8.38 Gbps no TXFIFO	39 (304 ns)
UT4 8.38 Gbps no TX, RXFIFO	28 (218 ns)
UT4 12.57 Gbps	34 (265 ns) ←
UT4 16.76 Gbps	31 (242 ns)

Summary

- Present Merger firmware's update: To be done in Dec.

- Data link mics.:
  - CDCFEE → Merger → TSF with 1.25X line rate
    - Together with the new ADC-based firmware
    - Schedule of Merger firmware update: Need to be careful
  - UT4: break through the limit

- Other plan: for CDCFEE upgrade
  - Plan to work for TRG data link: 4.2 Gbps or 8.4 Gbps with 64B/66B.
  - Contacting with relevant people in E-sys for other development works

Backup

Firmware download to flash

- During testing the new firmware, I was using JTAG to download .sof (.bit of Intel FPGA).
  - At least 3 Mergers (0-2, 1-3, 7-1) cannot be detected by JTAG at all.
    - We cannot do anything using JTAG on them.
  - I tried to re-insert those boards on VME crate, two of them became working (1-3, 7-1), but 0-2 is still not accessible now.

- To update Merger firmware .pof (.mcs) to flash:
  - We can do it via Merger crates' VME first, but it is possible to fail (< 10%?) Failed → Empty flash → Empty FPGA.
  - Then, we need to use JTAG to download .pof to those failed ones.
  - Using command line via VME to update all Mergers:
    5 crates in parallel → ~1 hr.
  - There will be 5~10 failed ones → ~1 more hr.

- But if failure happens in 0-2, we cannot do anything using JTAG.
  - Replace with spare board?
  - Try other JTAG cable? Need to find them in B2.
  - Move 0-2 to a standalone crate to test.