Status of spare CDC mergers

Jing-Ge Shiu/NTU, 2022,1201

Spare merger at NTU (before last week)

Five v3.02 (commissioning version) merger boards.
All were reported with some problems (since 2016).

036: JTag access to flash
042: JTag access to flash
056: JTag access to FPGA
073: Problem in the 2-directional pins between U1/U2 sometimes not properly working.
→ supposedly this won't affect the current commissioning (true?).
074: JTag access and VME interface

- The FPGA internal tamper bit (volatile key) were set on board 056 (U1) and 074 (U1 and U2), which causes the devices cannot be recognized by JTag (1st discussed in 2016 Feb. B2GM). This anti-theft design forbids the JTag access to FPGA and is not recoverable for Arrial II. The only solution recommended is to replace the FPGA (at least for Arrial II).

- Problem in soldering was found at a few places on those boards.

possible issue of the merger JTag problem

2016 Feb. B2GM

- Symptom
  - ➔fail to load the .sof file via JTag with the error message:
    - ➢"Can't configure device. Expected JTAG ID code …. , but found JTAG ID code 0x00000000."
    - ➢ So far, 4/80 production board, 1 pre-production board have this problem.
  - ➔the TDO reads 0x80 (should be 0x00)
    - ➢ the 'volatile key' is set → that is, the .sof file has to match with a preset key to be loaded into the FPGA.
    - ➢ this feature is for an anti-tampering security of this FPGA. However, the FPGA is not programmed with a non-volatile security key.
    - ➢ supposedly, this volatile key configure can be cleared.
  - ➔unfortunately, sometimes, the VME interface is also not stable for firmware loading.

如果, 按 Altera 的 description, 應該是 volatile key 被設 '1', but 我去 UNLOCK 都無效

Table 9: Security Mode Verification for 28-nm FPGAs

Security Mode	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
No key	0	0	0	0	0	X	X	X	X
Volatile key	1	0	0	0	0	X	X	X	X
Volatile key with tamper protection (9)	1	0	0	0	1	X	X	X	X
Non-volatile key	0	1	0	1	0	X	X	X	X
Non-volatile key with tamper protection bit (9)	0	1	1	1	0	X	X	X	X

所以看來只有兩條路:

1. 如 http://www.alteraforum.com/forum/showthread.php?t=34365 所言, 更換 FPGA 因為 tamper key 是 不可逆的

to us some tests to do to verify that the anti tampering bit I

rds. We replaced the 2 FPGA and we went on working...

2. Keep FPGA, 使用 VME update bitstream. 不使用 JTAG update .sof file.

On the left-hand side is the message from the merger company. Basically it says the same thing. They tried to unlock it but not successful.
(I am not sure if they have done it with the correct procedure.)

The FPGA on merer should be 40-nm FPGA, but the security mode verification has the same definition.

3 Arrial II from KEK (thanks to Iwasaki san)

The 3 FPGA with tamper bit problem on board 056 and 074 were replaced.

Both board are working well after the fix. However, board 074 was found JTag access problem again and being diagnosed as the same problem.

074 → 2 FPGA replaced → tested OK → broken again
056 → 1 FPGA replaced → tested OK

→ So replacing FPGA is a fix, but it is not a solution.

The JTag and VME accessibility are tested several times, as well as the TX/RX test.
The final result summary:

Merger ID	074	056	036	042	073
JTag to FPGA	NG	OK	NG	OK	OK
JTag to CPLD/FLASH	NG	OK	OK	OK	OK
VME access	N/A	OK	OK	OK	OK
transceiver TX/RX	N/A	NG	N/A	OK	OK

- ✔ Soliton download cable is replaced with USB-Blast II download cable
- ✔ TX/RX is tested with external cross-loopback of each FPGA unit.

- board 074: JTag access broken due to tamper bit set
- board 056: TX/RX test of U2 FPGA has no response,
  JTag can not find the configuration block for SignalTap monitoring.
- board 036: JTag access to U2 malfunction even though the FPGA is recognized by JTag.

→ board 042 and 073 have been delivered to KEK (on 1128),
Together with 128 of LM2C-L3S-TC-N-L 4x25G transceivers.

Concerning possible Arrial II FPGA

EP2AGX95EF29**I**3N → industry version, not available now.
I3, I5: operation temperature -40 ~ 100 °C
EP2AGX95EF29**C**6G → commercial version, still available in the market.
C4, C5, C6: operation temperature 0 ~ 85 °C

The footprint (EP2AGX5EF29) is same. One may choose one with the closest speed rank to use, but the operation temperature range could still be a concern.

Test Jtag cable: USB-Blast II download cable

CPLD/FLASH file: 20140513_mergerv3_1.19

(This is loaded before one can pursue the VME access tests.)

transceiver TX/RX test file: custom8B10B_altera_gen_together_5

(external cross loop back, two transceivers of the same FPGA connected to each other with optical fiber, with internal clock source)

VME interface: vme_v1.19_Mgr3 20140513 revised version.

Test mcs file: New_merger_v3.mcs

Test item:

reading board ID (set by DIP SW403)

write to register and read it back

unlock and erase flash, and write a mcs file to it

LM2C-L3S-TC-N-L 4x25G transceivers tested at 25Gbps BERT on UT4, using external loop-back (self or cross one) connection.

Testing Duration > 1 Hour

Data send/received > 9e13 bits, no bit error observed

(longer test, up to 11 days, has been applied to limited samples and no bit error observed either.)

SmartLink project