EventT0 after LS1 2022/9/21 T.Koga

EventT0

- -As a possible development during LS1, CDCTRG is discussing to degradate eventT0 resolution, to use ADC information instead
 - -fastest timing bit from CDCFE will be replaced with ADC
 - -will be recovered with new CDCFE after LS2
- -Requirement of eventT0 is ~10ns for SVD 3-sampling
- -In this case, TOPTRG must be ready for operation after LS1

 - -Is this acceptable for TOPTRG?
 -Could you make a schedule during LS1 at B2GM?

EventT0 resolution (σ)

	ECLTRG	CDCTRG	TOPTRG
before LS1	5~15ns	5~10ns	
after LS1	5~15ns	~25ns	~10ns
after LS2	5~15ns	5~10ns	~10ns