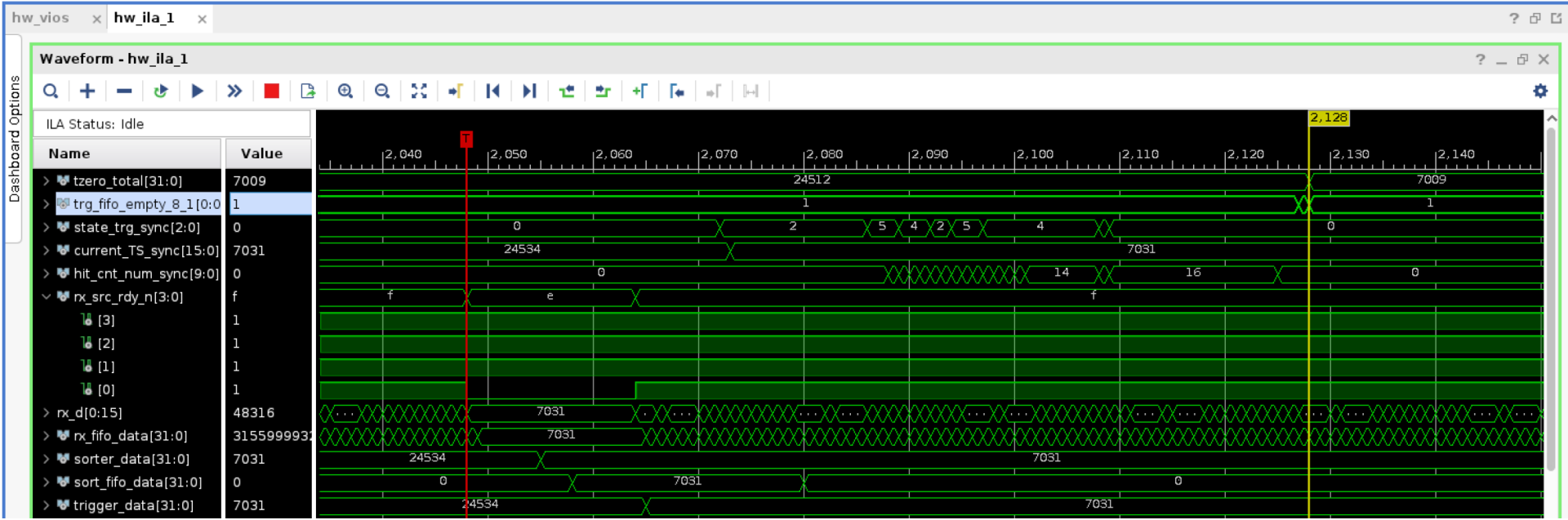
TOPTRG Status

Goal:
Port TOPTRG FW from UT3 to UT4

Status:
1.Erfei developed the Aurora 8b10b for GTY and successfully test with internal loopback on both VCU108 and UT4
2.Set up the TOP FEE infrastructure at Pitt to generate actual timestamps with pulser
3.Confirm the new TOPTRG FW (one bar) on VCU108 works correctly
4.Proceed to test the full TOPTRG FW (8 bar) on UT4 at KEK

TOPTRG FW (one bar) on VCU108 evaluation board



Clocking:

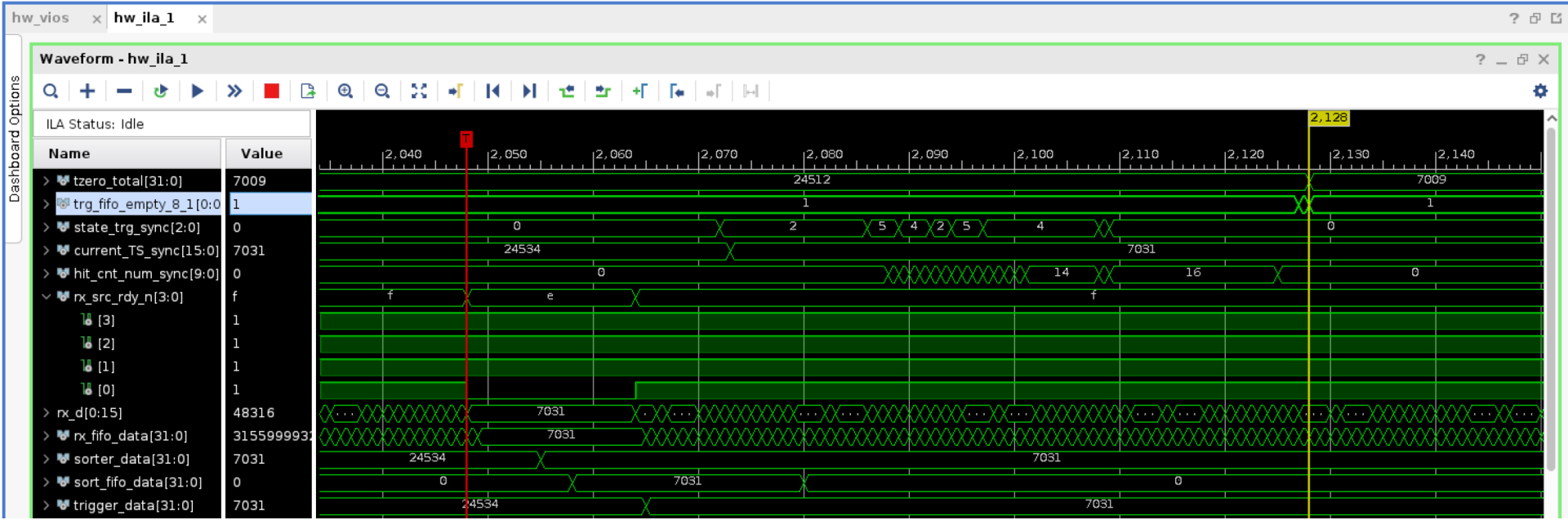
1.SI570 programmable oscillator – 127.22MHz

2.Clock Master – 127.22MHz

Pulse at 100Hz:

4 carriers * 4 ASICs * 1channel = 16 timestamps for each pulse

TOPTRG FW (one bar) on VCU108 evaluation board



Pulse at 100Hz:
4 carriers * 4 ASICs * 1channel = 16 timestamps for each pulse

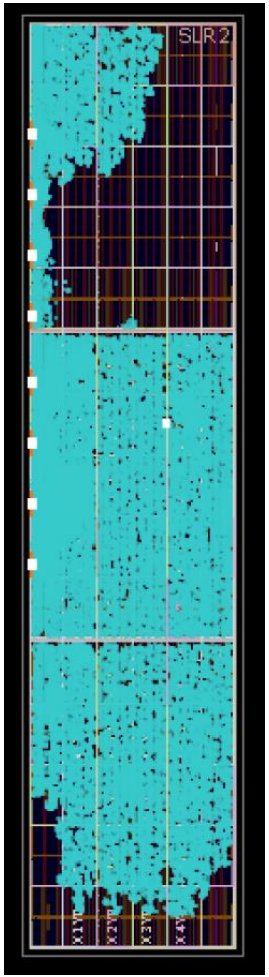
TOPTRG receive 16 timestamps and generate the t0 decisions correctly

TOPTRG FW (8 bar) for UT4

Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	244486	1074240	22.76
LUTRAM	2273	231840	0.98
FF	369388	2148480	17.19
BRAM	66	3780	1.75
IO	2	702	0.28
GT	32	76	42.11
BUFG	13	1800	0.72
MMCM	1	30	3.33



TOPTRG FW (8 bar) for UT4 without B2L/VME/b2tt is ready for test.

Backup

TOPTRG->GRL data format

Flags for slot-t0:
1bit * 16slots = 16bits

Number of hits: range [0,255]
8bits * 16slots = 128bits

Slot-t0: range [0,46080] / 2ns
16bits * 16slots = 256bits
MSB ~~10~~11 bits are common for all slots (reject slot-t0 outside 64*2=128ns window),
~~10~~11bits + ~~6~~5bits * 16slots = ~~106~~91bits

However, MSB ~~10~~11 bits should be sent from both UT3s for validation.

~~Total: 16+128+106(+10) = 250(260)bits~~
Total: 16+128+91(+11) = 235(246)bits

GTH 8 lanes from TOPTRG to GRL:
5Gbps: 256bits/127MHz

TOPTRG->GRL data format

bit	0	1	2	3	4	5	6	7
[0:7]	Flag slot 1-8							
[8:15]	Hit numbers slot 1							
[16:23]	Hit numbers slot 2							
[24:31]	Hit numbers slot 3							
[32:39]	Hit numbers slot 4							
[40:47]	Hit numbers slot 5							
[48:55]	Hit numbers slot 6							
[56:63]	Hit numbers slot 7							

TOPTRG->GRL data format

bit	0	1	2	3	4	5	6	7
[64:71]	Hit numbers slot 8							
[72:79]	MSB 11 bits of slot T0							
[80:87]				T0 slot 1-8				
[88:95]								
[96:103]								
[104:111]								
[112:119]								
[120:127]				Spare 5bits				