TOPTRG Status

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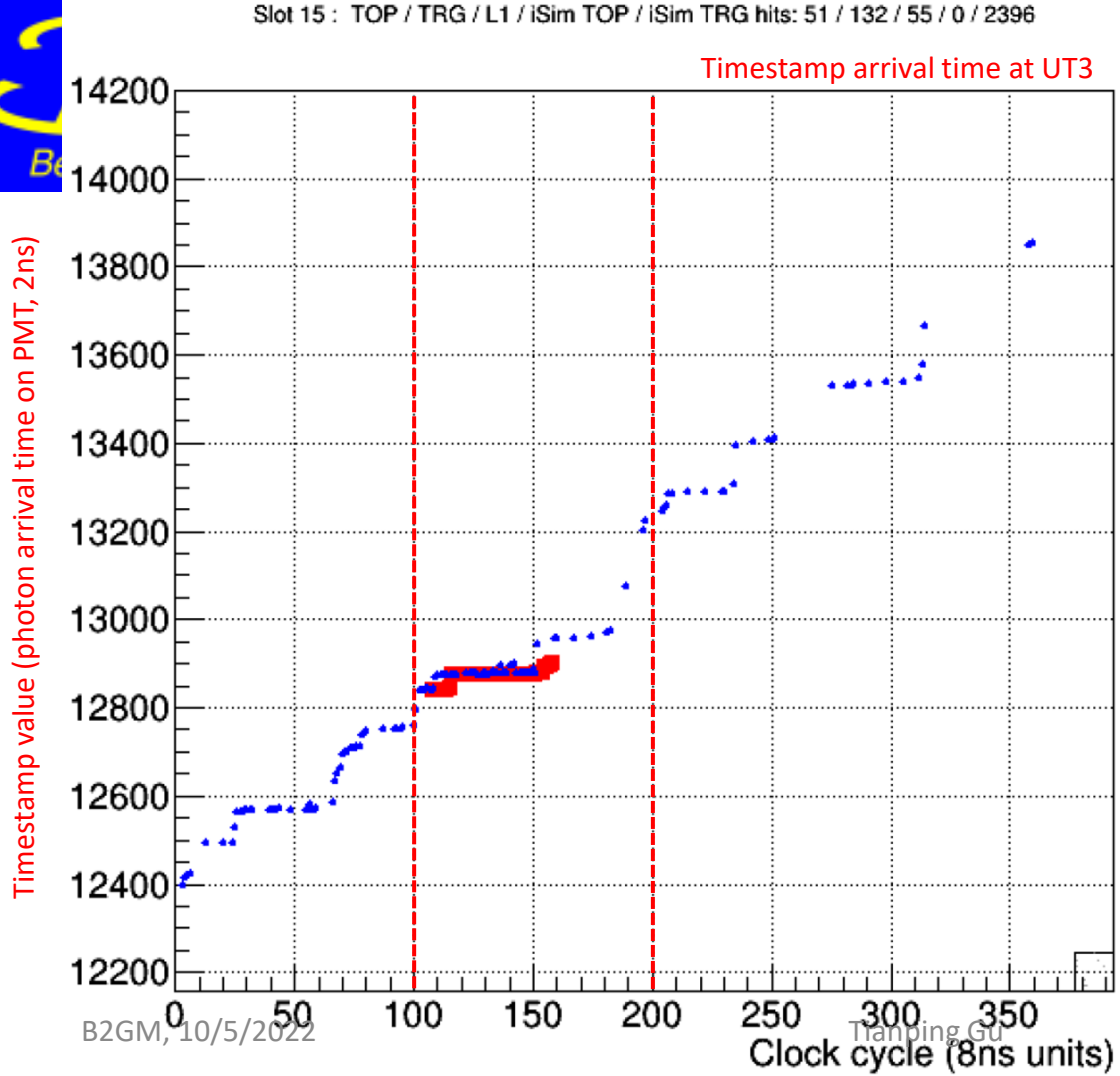
TOP TRG Status Since Last B2GM

As reported at previous B2GM, standalone TOP-based triggering does not seem to be possible due to excessively high beam-related background.
To understand how to make TOP TRG work in presence of such background we have been investigating using correlations of TOP TRG info with CDC 2D TRG tracks.

Since last B2GM, we:

- Performed offline simulation for several slot-level and combined timing algorithms using trigger readout data.
- Investigated the TOP TRG efficiency for hadronic events of relatively high charged particle multiplicity.
- (Tentatively) agreed on the CDC-TOP matching algorithm.
- Agreed to stream all TOPTRG slot decisions to GRL and perform matching at GRL.

- Started to port TOPTRG FW to UT4, core logic ported successfully.
- Tested the data link between UT4 and TOPFEE.
- Confirm the TOPTRG core logic work on UT4.



Collision data exp/run 26/766:

Red: TOP main readout hits

Blue: TOP TRG waveform readout timestamps

Currently, TOP TRG makes its timing decisions completely independently of ECL and CDC.

Therefore, in contrast to TOP main readout, TOP TRG is unable to reject background timestamps using digitization window w.r.t. the actual L1 decision.

We choose a narrow clock cycle window (e.g., between 100 and 200 clock cycles) to exclude slot-level background-based timing decisions.

This is an approximation for CDC-TOP TRG-level matching, grlcdc bits could be set to "high" for 200 clock cycles when there is a track pointing at a slot.

CDC-TOP matching

Performed offline simulation for several slot-level and combined algorithms:

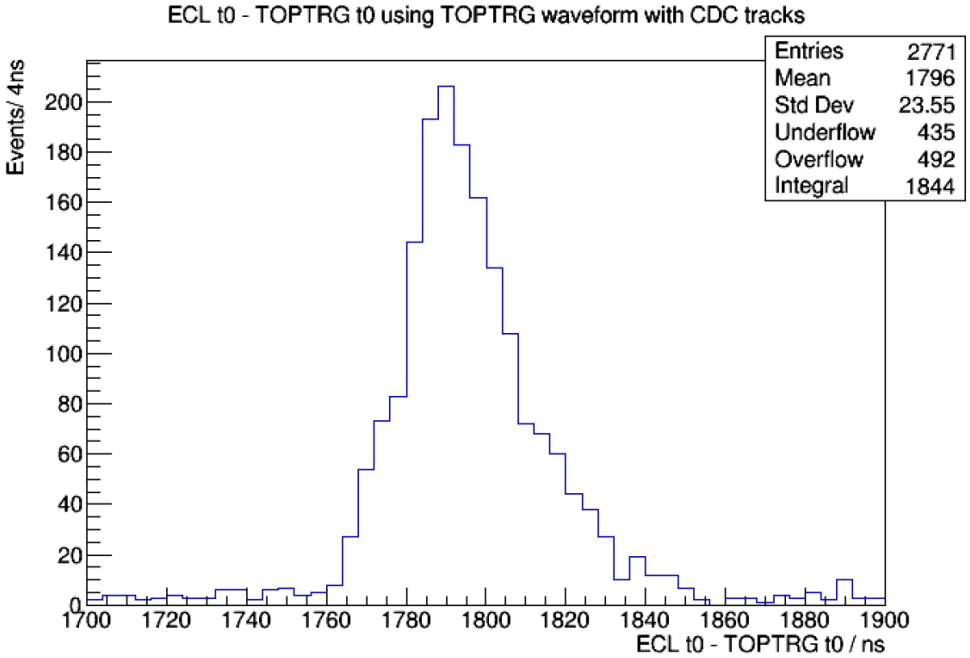
1.
Slot-level: maximum loglikelihood in the fixed timing range [100,200]. (logL threshold cut)
Combined: average of slot-level decisions with CDC 2D TRG track matching.
To be sent to GDL: this combined decision.

2.
Slot-level: maximum loglikelihood in the fixed timing range [100,200]. (logL threshold cut)
Combined: slot-level decision with the most hits with CDC 2D TRG track matching.
To be sent to GDL: this combined decision.

3.
Slot-level: generate slot-level decision on every clock cycle. (logL threshold cut)
Combined: average of slot-level decisions for the same clock cycle with CDC 2D TRG track matching.
To be sent to GDL: combined decision with the largest number of slot-level decisions.

4.
Slot-level: generate slot-level decision on every clock cycle. (logL threshold cut)
Combined: slot-level decision with the most hits of the same clock cycle with CDC tracks matching.
To be sent to GDL: combined decision with the largest number of slot-level decisions.

Approach 2: exp26 run 766, hadronic events



Collision exp26 run 766, hadronic events
Loglikelihood threshold: 10000000 (equivalent to ~15 timestamps)
Physics region (waveform readout clock cycles): [100, 200]
TOP TRG trigger waveform used in simulation
TOP-CDC matching is required for slots included in the algorithm
Figure of merit: TOP TRG timing w.r.t. ECL timing

Approach 2:

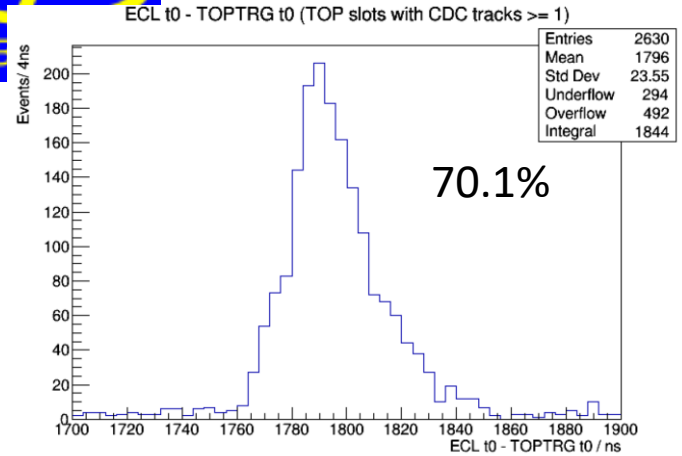
Slot-level timing decisions: maximum loglikelihood in the fixed timing range [100,200]. (logL threshold cut)

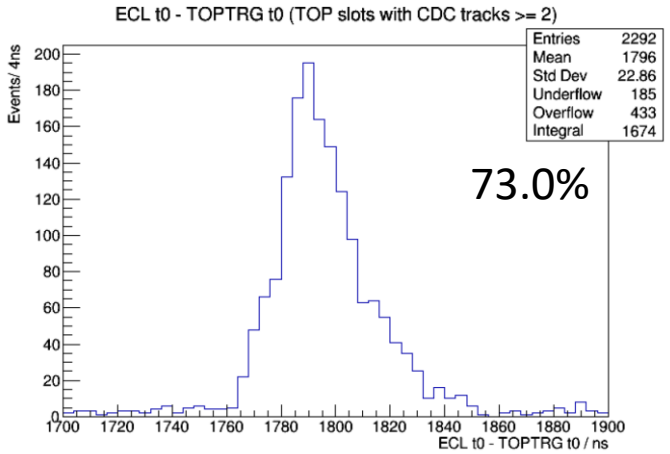
Combined timing decision: slot-level decision with the most timestamps with CDC 2D TRG track matching.

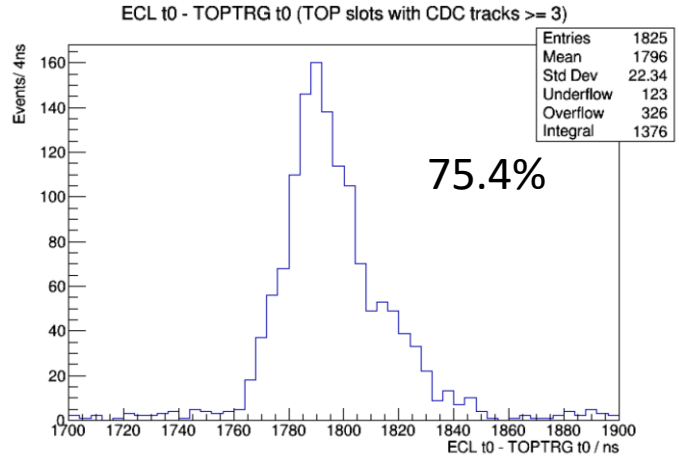
Use the slot t0 with most hits instead of average of all slot t0s
=> suppress background

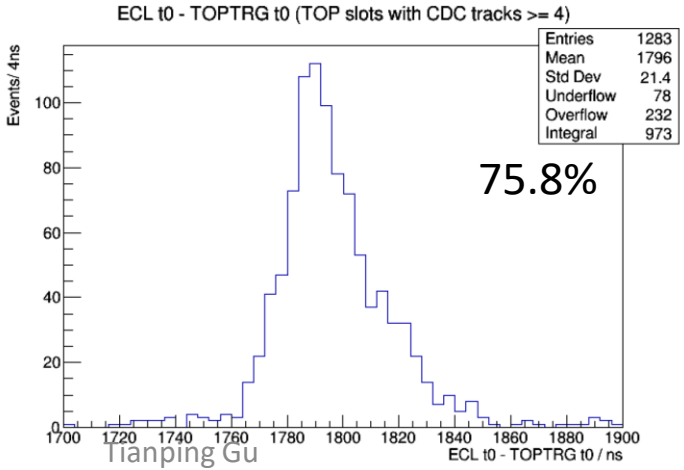
Efficiency: 1844/2771 = 66.5%
RMS: ~ 24 ns, Resolution: ~ 15 ns
Resolution improves significantly

Approach 2: exp26 run 766, hadronic events with high particle multiplicity









- Collision exp26 run 766 hadronic events
- Loglikelihood threshold: 10000000 ~15 hits
- Physics region: [100, 200]

TOP TRG t0 distributions for events which have more than n TOP slots with CDC tracks pointing to.

Efficiency for high-multiplicity hadronic events ~75%
RMS: ~ 22 ns
Resolution: ~ 13 ns

Summary of CDC-TOP matching studies

- Offline simulation performed for several slot-level and combined algorithms.
- Currently, the best results obtained using approach 2
  (using timing from the slot with the largest number of timestamps):

  Efficiency for hadronic events: ~67%
  Efficiency for high-multiplicity hadronic events: ~75%
  (ECL-TOP) timing resolution for hadronic events: ~15 ns
  (ECL-TOP) timing resolution for high-multiplicity hadronic events: ~13 ns

Discussion:
- Agreed to use approach 2 as tentative CDC-TOP matching algorithm.
- Agreed to stream all TOPTRG slot decisions to GRL and perform matching at GRL.
- Proposed TOPTRG -> GRL data format, send slot-level info to GRL (T0, hit number, flag).

TOPTRG->GRL data format

Flags for slot-t0:
1bit * 16slots = 16bits

Number of hits: range [0,255]
8bits * 16slots = 128bits

Slot-t0: range [0,46080] / 2ns
16bits * 16slots = 256bits
MSB 11 bits are common for all slots (reject slot-t0 outside 32*2=64ns window),
11bits + 5bits * 16slots = 91bits

However, MSB 11 bits should be sent from both UT3s for validation.

Total: 16+128+91(+11) = 235(246)bits

GTH 8 lanes from TOPTRG to GRL:
5Gbps: 256bits/127MHz

bit	0	1	2	3	4	5	6	7
[0:7]	Flag slot 1-8							
[8:15]	Hit numbers slot 1							
[16:23]	Hit numbers slot 2							
[24:31]	Hit numbers slot 3							
[32:39]	Hit numbers slot 4							
[40:47]	Hit numbers slot 5							
[48:55]	Hit numbers slot 6							
[56:63]	Hit numbers slot 7							

bit	0	1	2	3	4	5	6	7
[64:71]	Hit numbers slot 8							
[72:79]	MSB 11 bits of slot T0							
[80:87]				T0 slot 1-8				
[88:95]								
[96:103]								
[104:111]								
[112:119]								
[120:127]				Spare 5bits				

Porting TOPTRG to UT4

Utilization Post-Synthesis | **Post-Implementation**

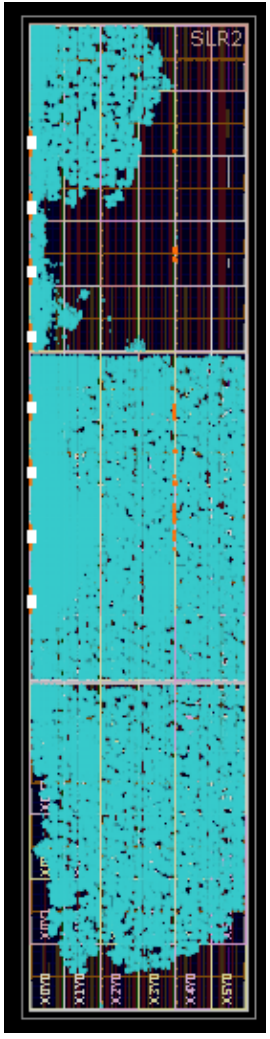
Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	245599	1074240	22.86
LUTRAM	2673	231840	1.15
FF	373064	2148480	17.36
BRAM	109.50	3780	2.90
IO	36	702	5.13
GT	32	76	42.11
BUFG	18	1800	1.00
MMCM	2	30	6.67

Power **Summary** | On-Chip

Total On-Chip Power:	**19.51 W**
Junction Temperature:	**40.5 °C**
Thermal Margin:	59.5 °C (69.2 W)
Effective θJA:	0.8 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Medium

Implemented Power Report

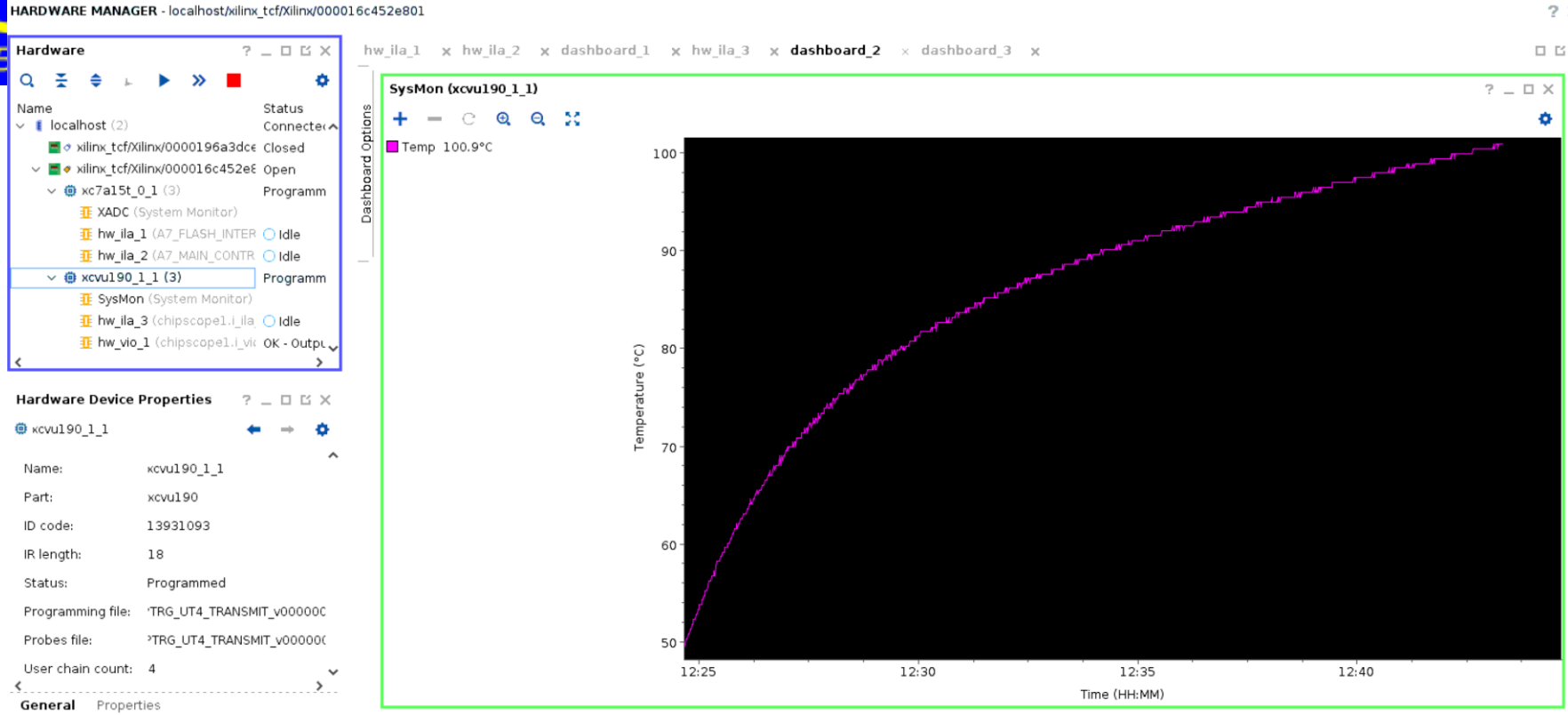


32 Aurora 8b10b (GTY transceiver) data links between TOPFEE and TOPTRG.

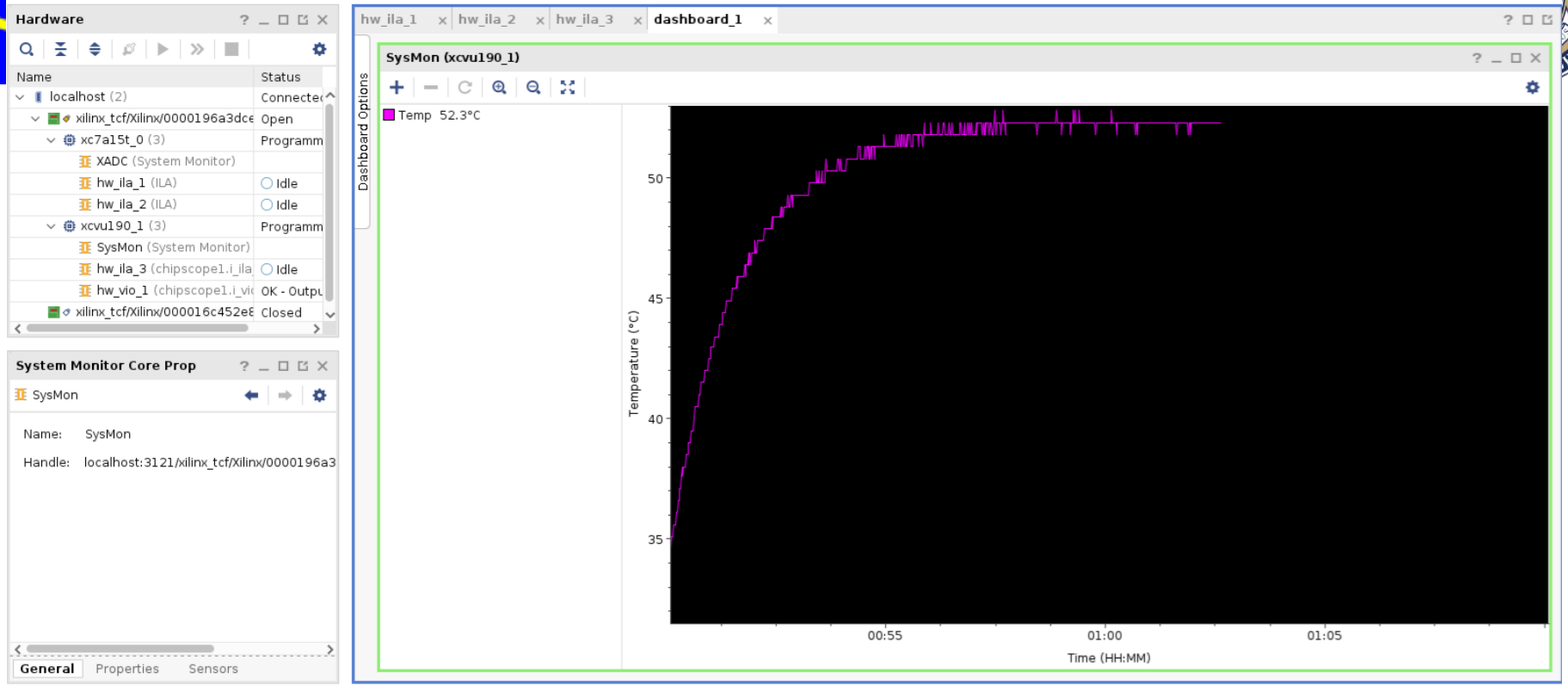
Core logic for slot decision making.

Successfully test on UT4 at KEK using test generator / pulser.

Thermal issue of UT4



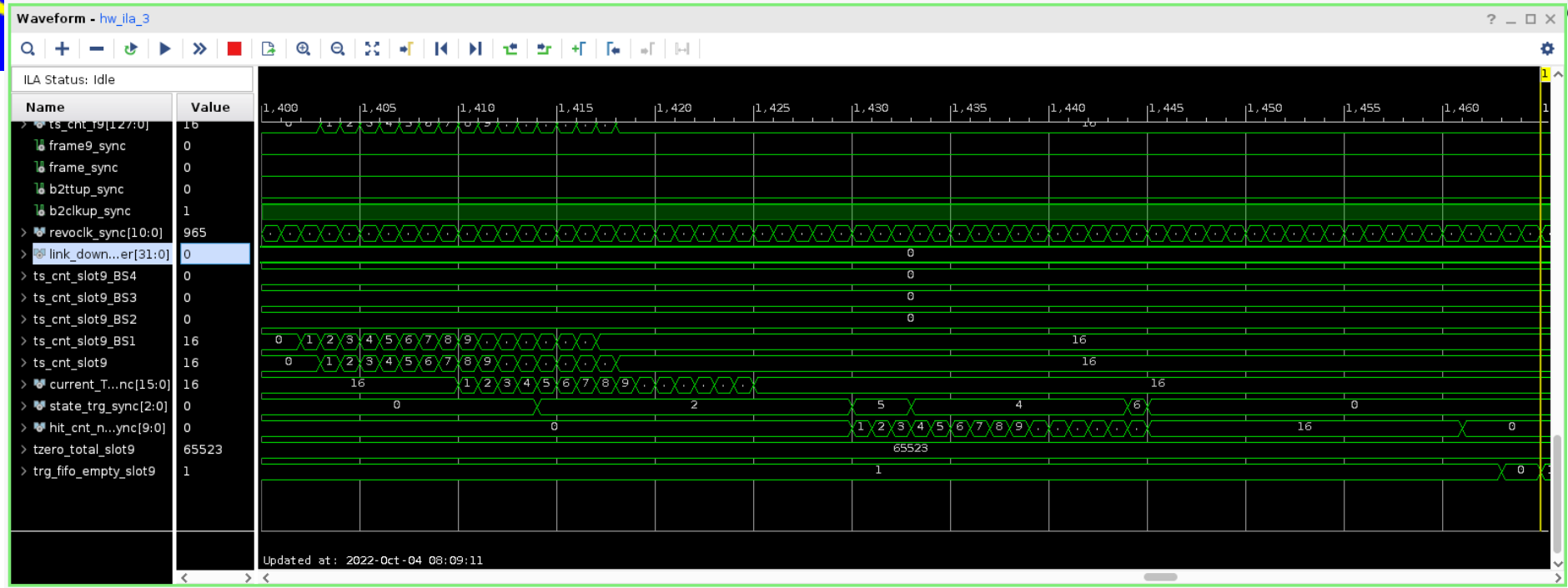
Thermal issue of UT4



Unno-san and Koga-san adjusted the VME crate and the location of UT4.

Now both UT4s are good, stabilize at ~50 °C

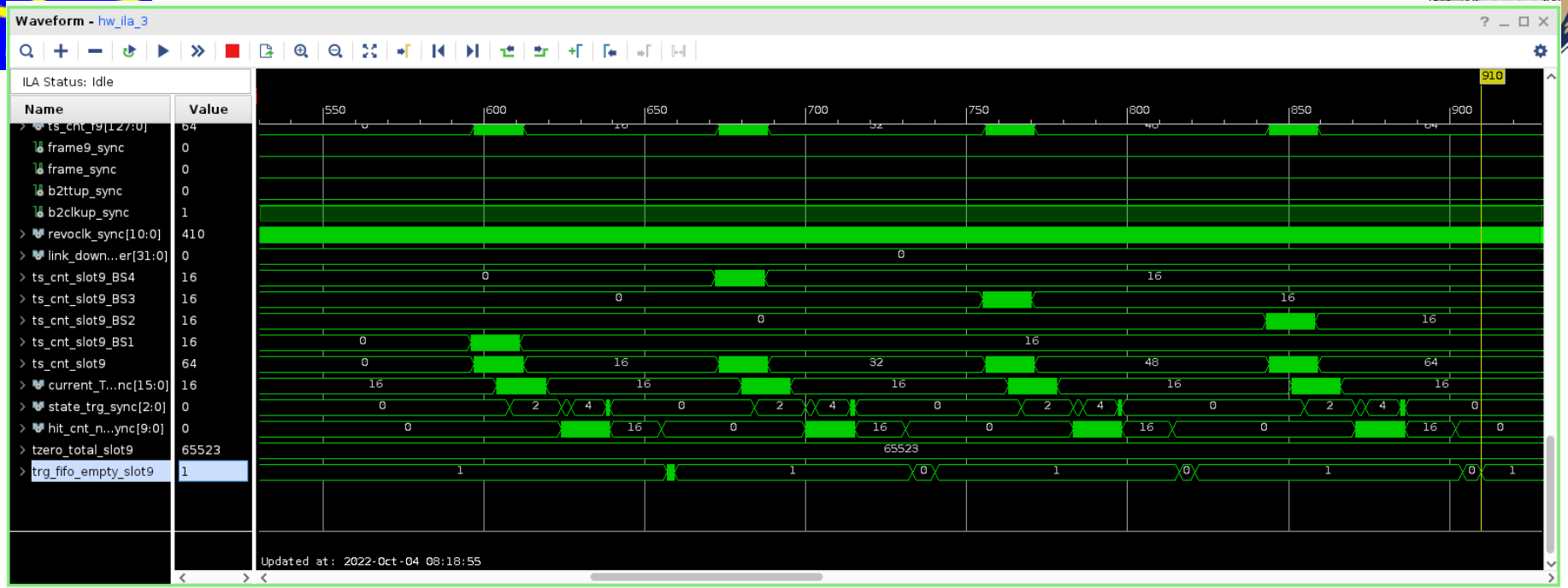
TOPFEE -> TOPTRG data link (slot 9)



SCROD test generator : s09a generates 16 timestamps.

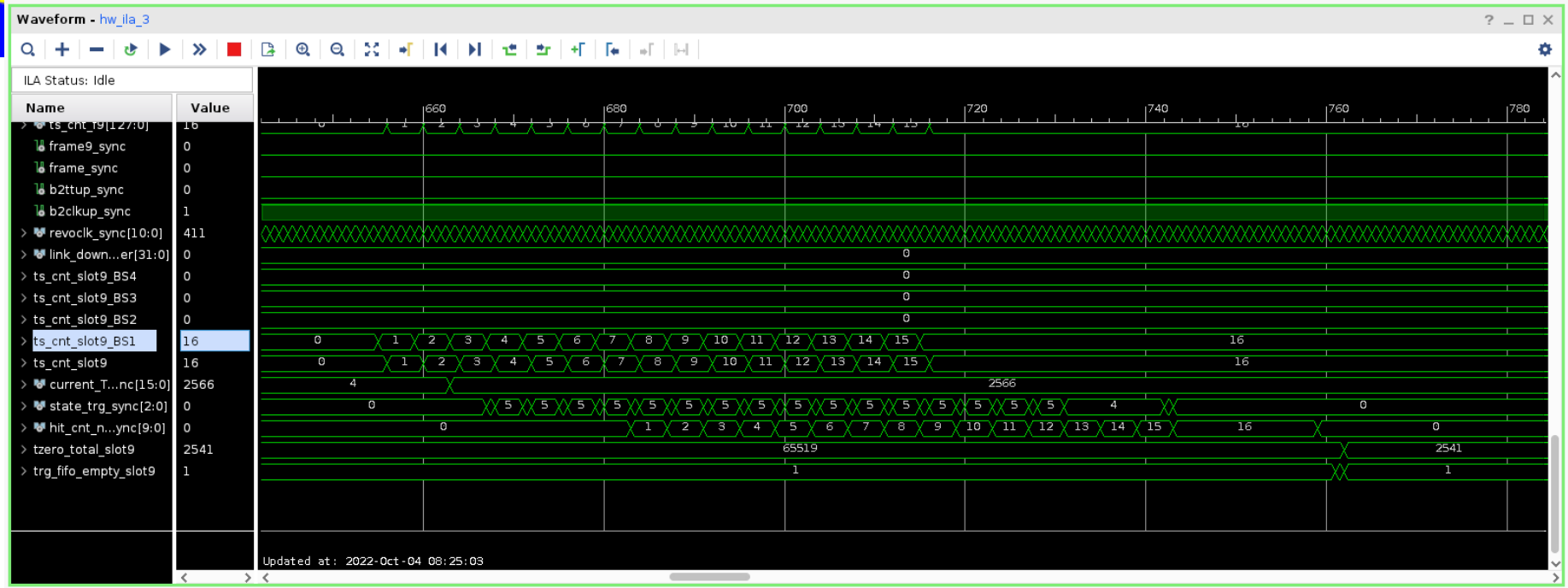
TOPTRG receive 16 timestamps and generate the t0 decisions correctly.

TOPFEE -> TOPTRG data link (slot 9)



SCROD test generator : each boardstack generates 16 timestamps.
TOPTRG receive 4 bunches of timestamps and generate the t0 decisions respectively.

TOPFEE -> TOPTRG data link (slot 9)



Carrier test generator : s09a carrier 0 generates 16 timestamps.

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- Started to port TOPTRG FW to UT4, core logic ported successfully.
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- Confirm the TOPTRG core logic work on UT4.

- Next steps:
- Set up the link between TOPTRG and GRL with new TOPTRG->GRL data format
- Work on implementing CDC-TOP matching logic on GRL
- Set up other necessary part e.g. VME, TOPTRG->GDL, etc.