Current Outlook on TOP TRG Schedule During LS1

Need to fully validate TOP FEE -> UT4 trigger path (this is the highest priority project)

Current line rate used: 5.08Gbps (128MHz / 32 PMTs = 4MHz/PMT)

Possible line rate (validated in Pittsburgh) 10.16Gbps (8MHz/PMT)

half of the bandwidth is being wasted: possible to go to 16MHz/PMT
there are still some issues to work out in trigger path on TOP FEE
(more studies are needed for TOP FEE -> UT4 trigger path)

Shorter FIFOs? Resets in TOP FEE to discard very late trigger information?
Higher trigger thresholds? The effect on PID performance?

Will be working on initial validation of all links before Nov.'22 shutdown of eHut.

Need to run user FW on UT4 at a higher clock frequency.
Note that we merge streams for four boardstacks (currently: 4x128MHz)
Current clock: 128MHz
Achieved (after many tries): 256MHz
Ideally would like to do: 512MHz

Some work has been done in this area already.
More work will be done in November-December
The new slot-level algorithm makes this project more challenging

Thermal environment on UT4 is a matter of concern.
Need to monitor the die temperature, probably need to have an interlock?
One of TOP UT3s had its heat sink cracked.
VIRTEX UltraScale runs significantly hotter than VIRTEX-6.

TOP TRG -> GRL/GDL communications: new protocol is being implemented.
Slot-level t0 decisions will be streamed to GRL/GDL.
Expect progress in time for the next B2GM in Jan.-Feb. 2023.

Need to integrate our FW with VME readout / belle2link readout / slow control on UT4.
Will be worked on probably only after the next B2GM.

belle2link over GTH / is a faster clock (for belle2link readout) possible? Need to investigate.

Currently, we are only able to send ONE decision to GRL/GDL every frame (i.e., in 1280 clock cycles)
The algorithm for this needs to be developed from scratch. There are some complications here,
as our tentative t0 decisions from individual slots are not necessarily time-ordered.
Impementation of posting individual slot-level decisions to GDL/GRL is likely challenging.

Resources and Timescale

Tentatively would like to have everything in place and working by the end of summer 2023.

Currently, Tianping is practically the only really active developer,
VS is very busy until May'23,
Erfei needs to focus on his PhD thesis now.
But everyone would, of course, participate as necessary. Especially in Summer'23.

Will try to train another developer (but there is no project-allocated manpower support from the DOE)

Will work with Vasily S. (Hawaii) to understand what to do in TOP FEE.

Will need a discussion with TOP group concerning PID performance and trigger thresholds.

Data analysis will continue (and tools ae available)

Working out how our information could be used together with CDC at GRL: Summer and Fall'23.