

GDL

B2GM 20221005

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Upgrade to UT4

- UT3 (hx565t)
 - Resource > 70%
 - Tight timing score

	Strategy	Host	Output	Status	Timing Score	Run Time	LUTs	Slice Registers	WorstCaseSlack
<input type="checkbox"/>	impTA	btrgpc08	run1	Done	177	03h 10m 05s	190,073 (53%)	132,484 (18%)	-0.115ns
<input checked="" type="checkbox"/>	impTAJB2	btrgpc08	run2	Done	0	03h 10m 41s	190,367 (53%)	132,512 (18%)	0.006ns
<input type="checkbox"/>	impTAJB3	btrgpc08	run3	Failed Par	None	08h 59m 29s	191,885 (54%)	132,964 (18%)	0.004ns
<input type="checkbox"/>	impTAJB5	btrgpc08	run4	Done	177	03h 19m 49s	190,073 (53%)	132,484 (18%)	-0.115ns
<input type="checkbox"/>	impTAJB6	btrgpc08	run5	Done	2228	03h 36m 42s	172,092 (48%)	132,478 (18%)	-2.029ns
<input type="checkbox"/>	impTAJB7	btrgpc08	run6	Done	177	03h 17m 37s	190,073 (53%)	132,484 (18%)	-0.115ns
<input type="checkbox"/>	impTAJB8	btrgpc08	run7	Done	213466	03h 30m 40s	190,534 (53%)	132,483 (18%)	-2.944ns
<input type="checkbox"/>	impTAJB2CT2	btrgpc08	run8	Failed Par	None	05h 25m 26s	189,691 (53%)	132,512 (18%)	3.045ns
<input type="checkbox"/>	impTAJB2CT3	btrgpc08	run9	Done	736	03h 11m 58s	190,647 (53%)	132,513 (18%)	-0.323ns
<input type="checkbox"/>	impTAJB2CT4	btrgpc08	run10	Failed Par	None	05h 02m 38s	189,503 (53%)	132,513 (18%)	-3.978ns
<input type="checkbox"/>	impTAJB2CT5	btrgpc08	run11	Done	0	03h 07m 08s	189,578 (53%)	132,513 (18%)	0.016ns
<input type="checkbox"/>	impTAJB2CT6	btrgpc08	run12	Done	0	03h 02m 48s	190,228 (53%)	132,512 (18%)	0.005ns
<input type="checkbox"/>	impTAJB2CT7	btrgpc08	run13	Done	244	03h 05m 34s	190,019 (53%)	132,512 (18%)	-0.148ns
<input type="checkbox"/>	impTAJB2CT8	btrgpc08	run14	Done	0	02h 40m 21s	190,175 (53%)	132,512 (18%)	0.005ns
<input type="checkbox"/>	impTAJB2CT9	btrgpc08	run15	Failed	None	00h 00m 04s	None	None	None
<input type="checkbox"/>	impTAJB2CT10	btrgpc08	run16	Failed	None	00h 00m 04s	None	None	None
<input type="checkbox"/>	impTAJB2CT11	btrgpc08	run17	Failed	None	00h 00m 04s	None	None	None
<input type="checkbox"/>	impTAJB2CT12	btrgpc08	run18	Failed	None	00h 00m 04s	None	None	None
<input type="checkbox"/>	impTAJB2CT13	btrgpc08	run19	Failed	None	00h 00m 04s	None	None	None
<input type="checkbox"/>	impTAJB2CT14	btrgpc08	run20	Failed	None	00h 00m 04s	None	None	None

Optical Links

	UT4	dclk MHz	GB/s	FIFO	data
GRL	GTU0	127	8	126x4	42x4
KLM	GTU1	127	8	126x4	42x4
ETM	GTU4	8	8	16x1	256x1
ETF	GTU5	32	12	126x4	42x4
TOP	GTH1	127	5	16x4	32x4
B2L	GTH7		2.5		

- Refclk GTU=254MHz, GTH=254MHz

Compile

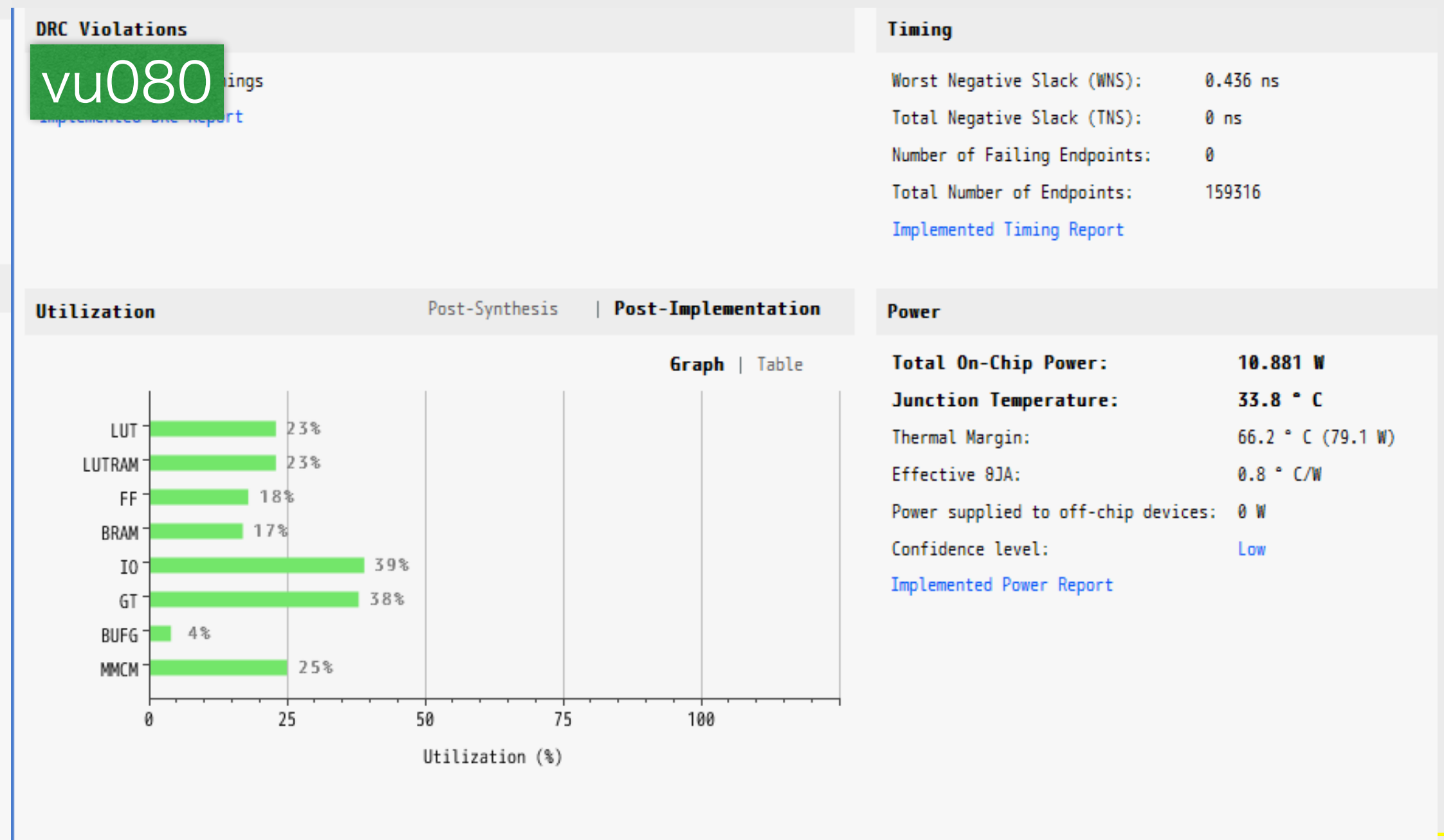
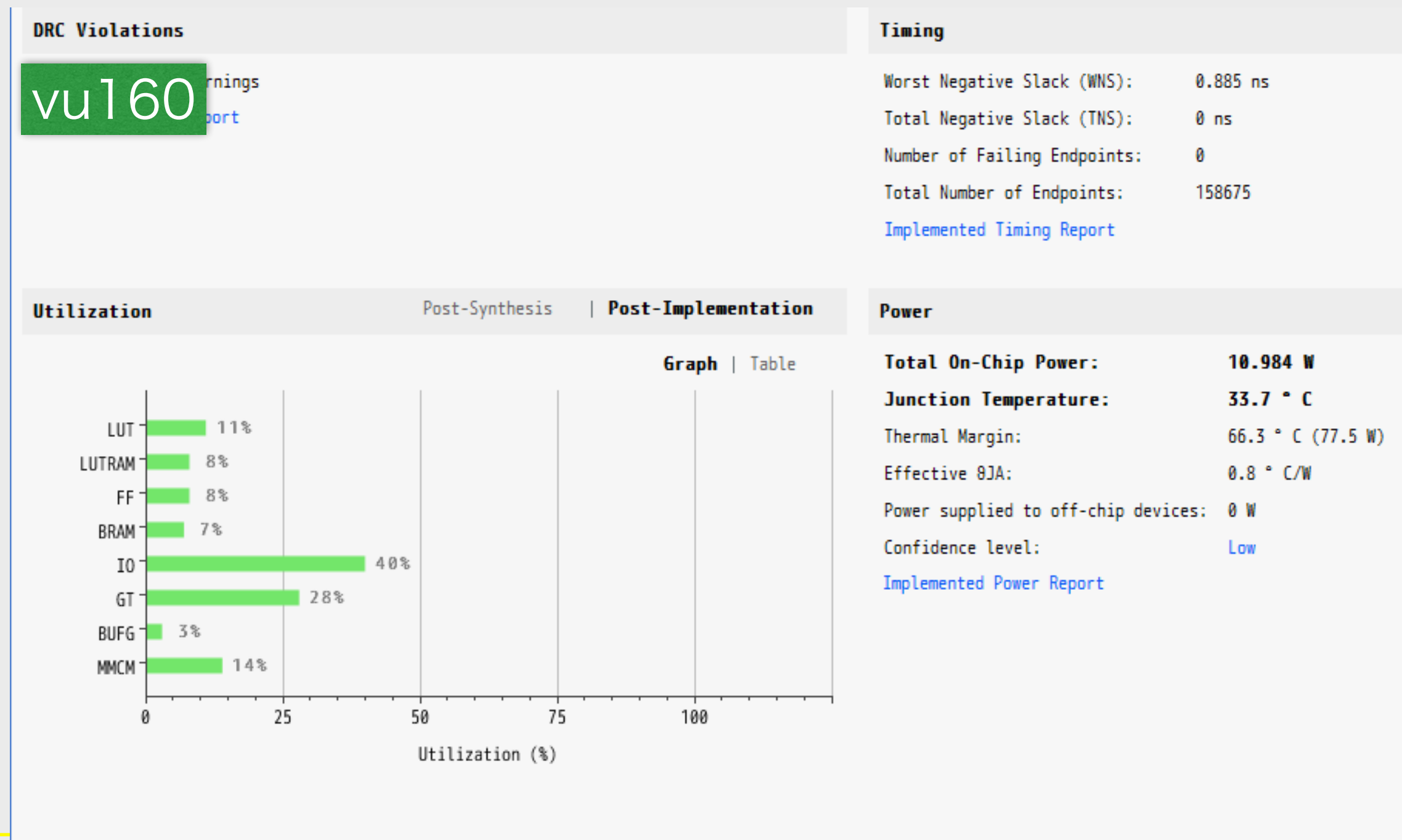
- Both vu080 and vu160 Tested

- Difference:

- set_property INTERNAL_VREF 0.6 in UT4_Main_GLOBAL.xdc
- set_properly LOC gen_ictrl1.map_ic (vu160)

- No timing errors

- MVSYCLK, clk50m, clk20m are ignored (set_false_path). Is this OK?
- Resource usage of vu160 is less than half of vu080.



ftdl v46

- <https://confluence.desy.de/pages/viewpage.action?pageId=75106458>
- LVDS 4 ports (UT3) -> 2 ports (UT4)
 - 32 bit for 1 port
 - All GRL signals (CDCTRG, matching) via LVDS due to limited latency.
 - UT3 (4 LVDS ports)
 - 3 for GRL, 1 for ETF for future modification.
 - UT4 (2 LVDS ports)
 - 2 for GRL
 - Removed:
Input: s2fo, s2f3, s2f5, s2so, s2s3, s2s5, grlgg1, grlgg2, bwdsb, fwdsb, bwdnb, fwdnb, brlnb1, brlnb2, brlfb1, brlfb2, ieklm
Output: fso(0), syo(1), syoecl(0),
 - New LVDS extension board?
- New input bits
 - tx_3 “pulse of # of NN veto cut track > 3”
- New output bits
 - tx3 <= tx and !injection

Status and Summary

- ECLTRG signals seen.
 - GTH (UT3) -> GTY (UT4)
 - Consistent rates with ETM
 - ecl-ing=1 (~3 for UT3)
 - Arrival timing can be delayed by 1 127m clock.
- B2L readout OK (vu160 not yet tested)
 - Need to learn how to look into data
- Need to test other connections
 - Link to KLM and TOP up
 - Link to ETF (only 12g) and GRL (same config with KLM) down.
- Will use vu160 unless urgent need of vu160 from other module.