Compton HVMAPS Detector Work Update

Belle II Collaboration Meeting
October 2022

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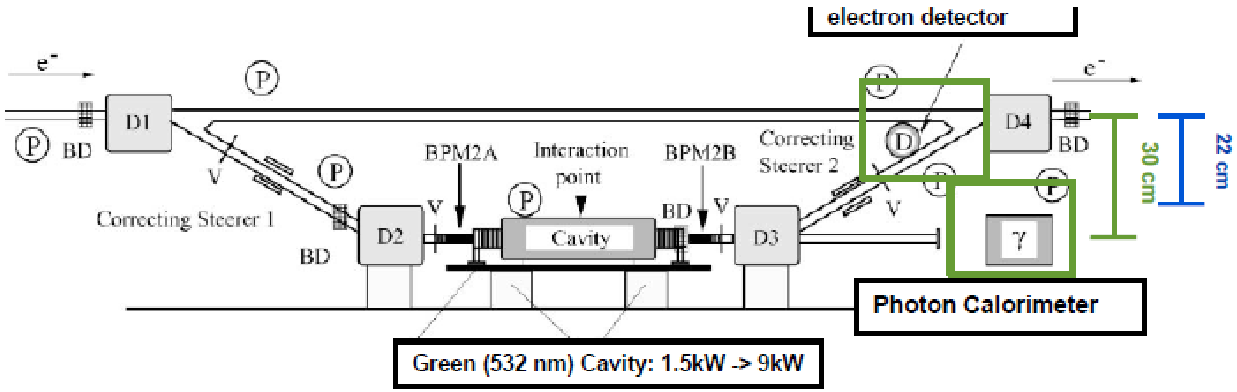
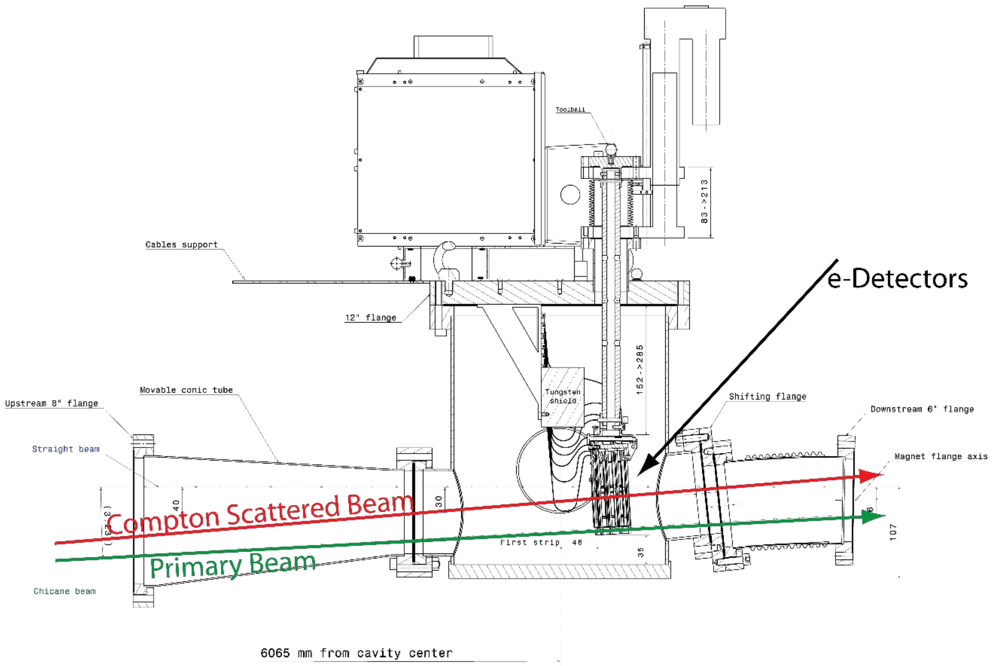
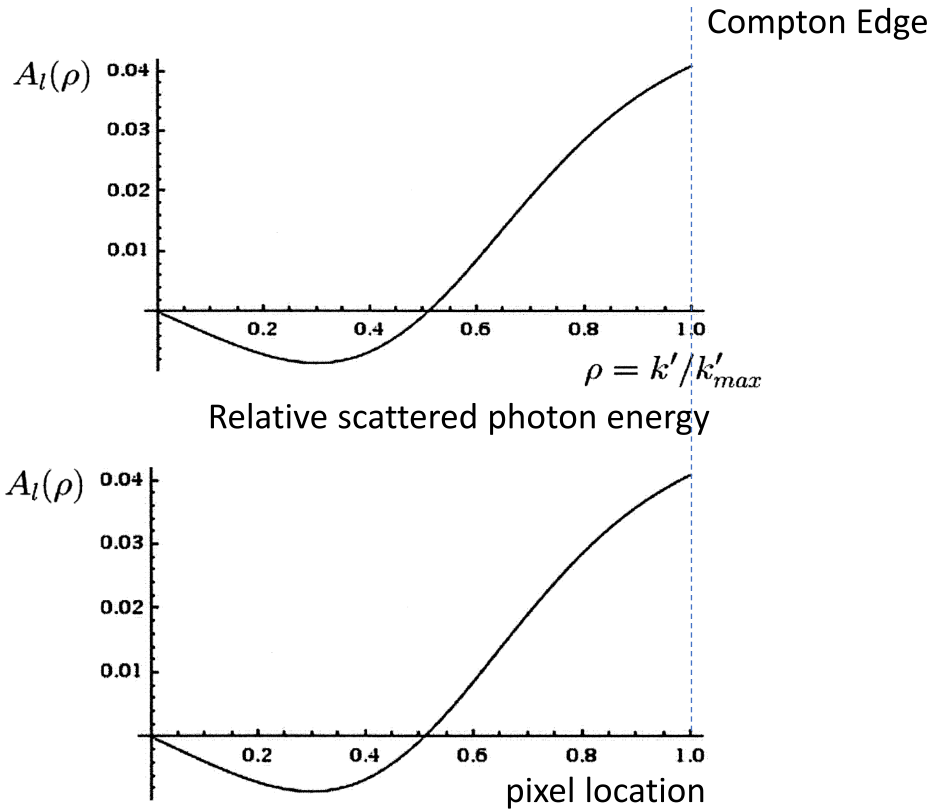
Initial Assumptions:

- Initial ideas were based on experience with JLab HallA & C polarimeters
  - Measure electron energy by deflection in dipole field (D3)
  - Higher photon energy → lower electron energy
  - Lower electron energy → more bending away from beam
  - build a detector that can accurately measure electron deflection

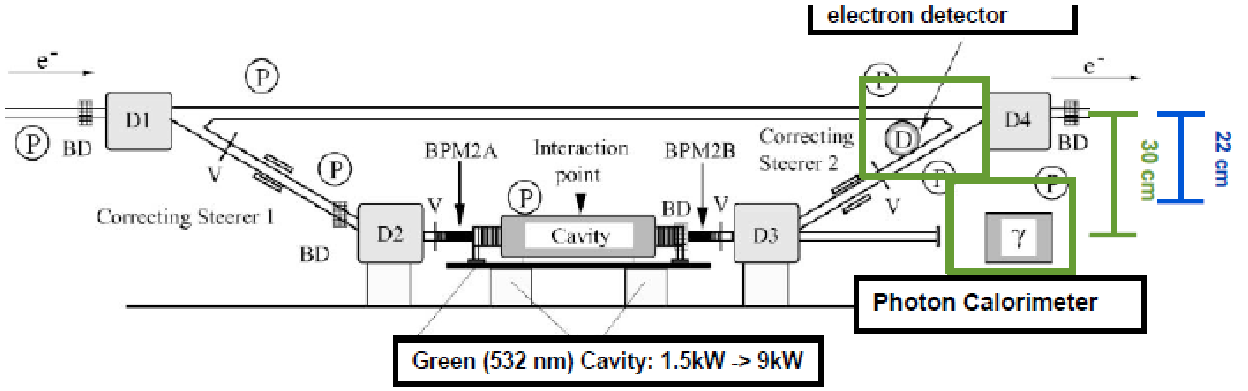


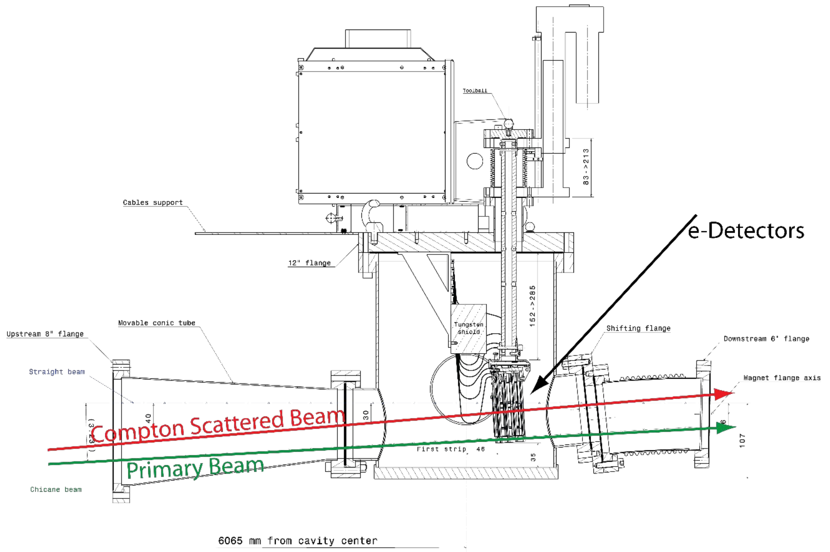




Realities:

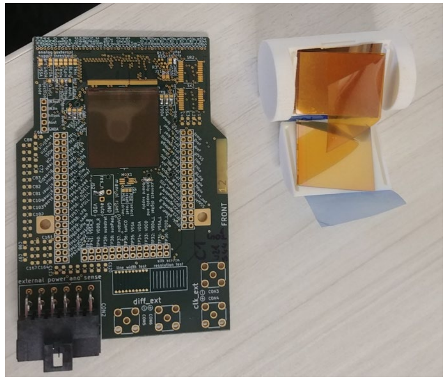
- Having a Chicane and separate Compton dipole not possible for SuperKEKB
- Have to use existing beam line dipoles and fit Compton interaction region between them
  - It would not be in a straight line-of-sight to IP
  - Have to model transport or measure transverse polarization (EIC plans to use HVMAPS in front of the photon detector to measure the photon position asymmetry to determine transverse polarization)
- Possibly implement thin Beryllium window in beampipe to allow electrons to exit primary beam vacuum
  - Still build an analyzing dipole
  - Effect of position resolution at the EDet would need to be studied

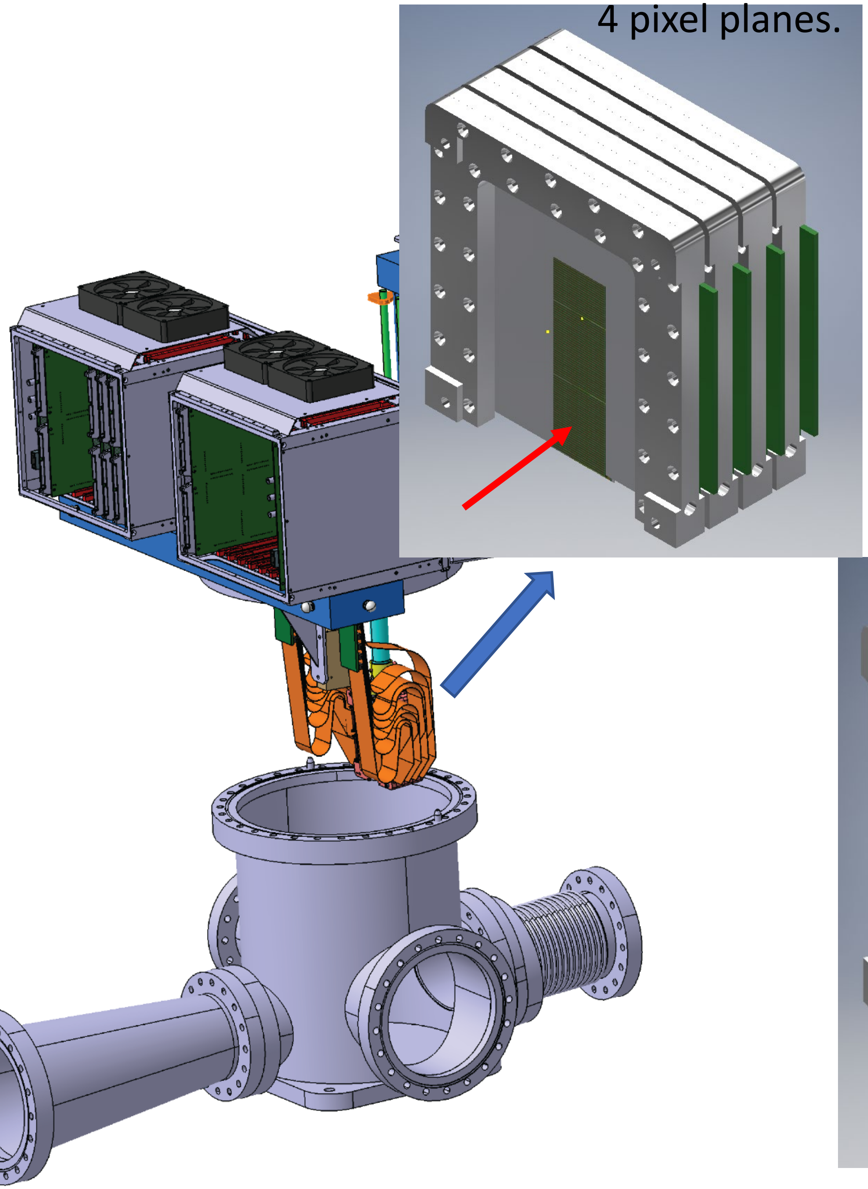


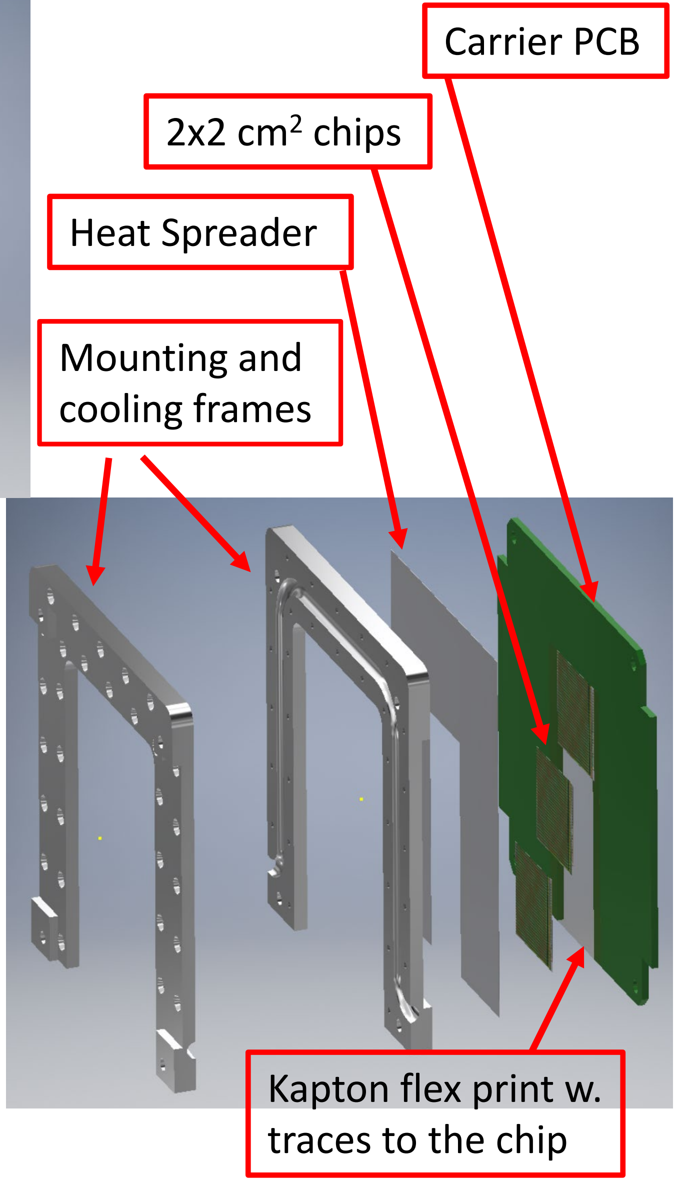


Position Sensitive Detector Design:

- 4 pixel detector planes
- HVMAP pixel detectors
- 3 $2 \times 2\ cm^2$ chips per plane (TBD based on profile)
- $80 \times 80\ \mu m$ pixels
- Original chip design based on ATLASPix & MuPix (designed at KIT, Heidelberg, Mainz)
- Specific modifications for MOLLER/P2
- Specific ChiralBelle mods probably possible, if need be

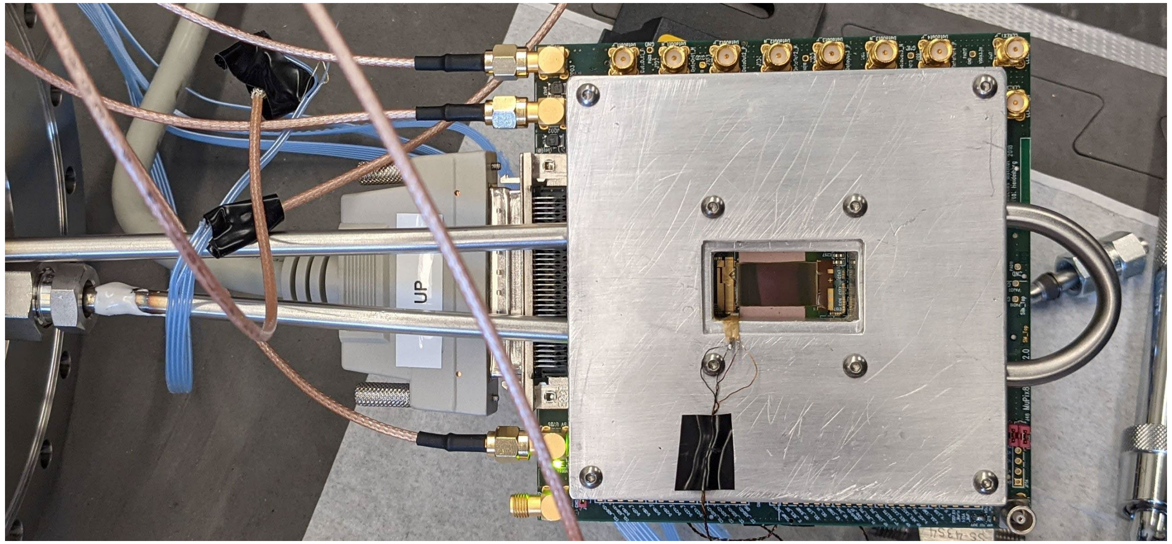




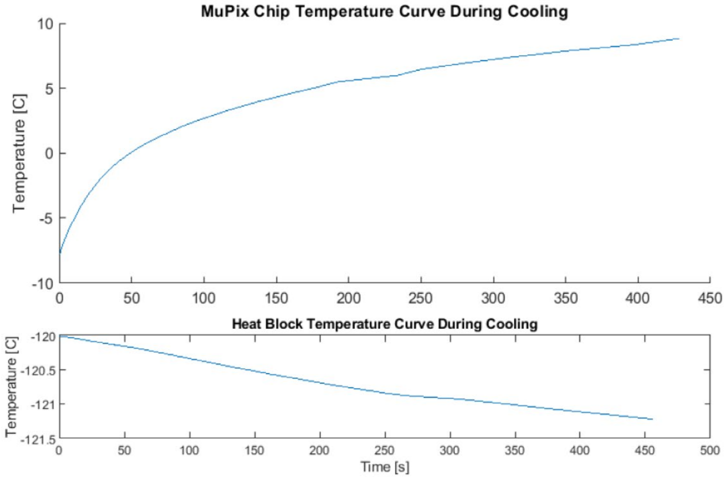


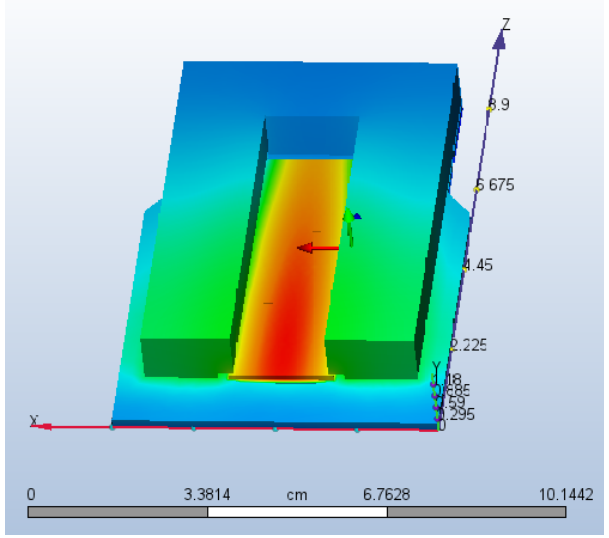
Detector Prototyping:

- The full $2 \times 2\ cm^2$ chip draws about 1 Watt
- We need some form of cooling inside the vacuum
- Shown on the left is a prototype board that was located in a test vacuum chamber
- Final implementation has no other electronics inside the vacuum, besides the detector chip
- The powered chip does not heat up with cooling
- Only during active readout does chip heat up
- Readout digital electronics cause draws most of the power
- Plan to have the chip edge in thermal contact with a cooled heat sink (water-glycol ?)
- Possible cooling mechanism to be confirmed with facility



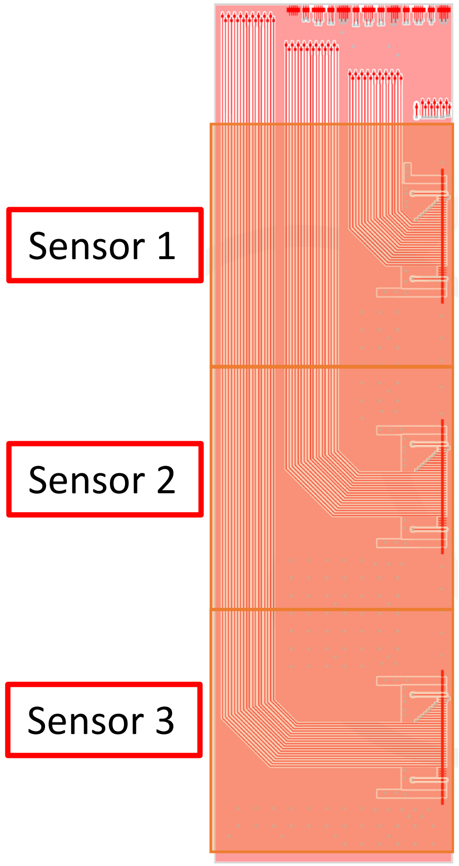
Work by Nafis Niloy

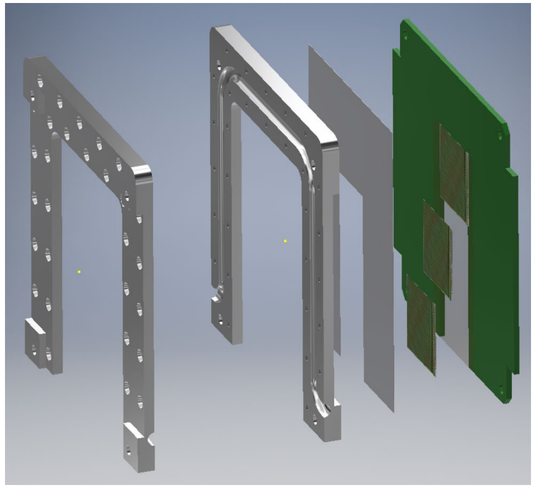




Detector Prototyping:

- Plan to have 3 HVMAPS per flexprint (depends on profile)
- About 30 data lines per plane + GND, VDD, Sense
- Flexprint to end of chip block PCB – then connect to ribbon cable
- Ribbon to outside vacuum onto custom designed readout board
- Connect to commercial FPGA board away from detector
- Need to produce new translation stage and top-flange design (depends on actual layout at SuperKEKB)
- Continuing with actual mounting block design and more cooling tests for MOLLER, but will apply what we learn to ChiralBelle design
- Flexprint and carrier board design is underway for MOLLER, but may require additional changes for ChiralBelle, depending on what we want for that chip (Gating, interface to the DAQ etc.)

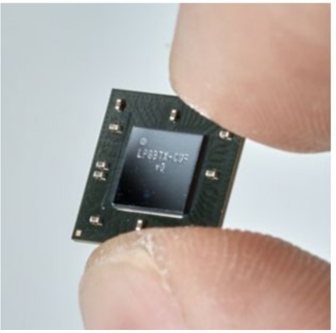




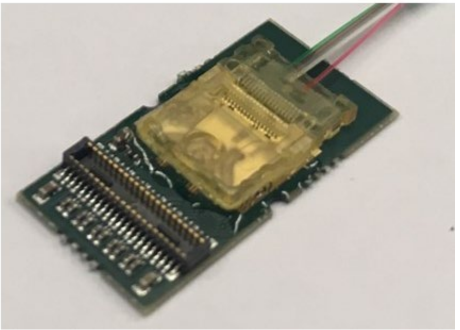
Readout Prototyping:

- Readout from the detector module can be done via low power gigabit transceiver (lpGBT) SER/DES chip and the associated VTRX+ optical transceiver.
- Both were developed by CERN for the LHC experiments and are radiation hard
- Sales contract with CERN has been signed for MOLLER needs, with enough overhead to do ChiralBelle prototyping, but prefer to make separate arrangements for ChiralBelle when the time comes (different accounts).
- The other end would be a commercial Xilinx FPGA board
  Xilinx kcu105 currently used for prototyping
- The Manitoba group recently hired an engineer to organize and carry out the design process for these interfaces
- Currently prototyping with CERN developed prototype board that integrates the two chips
- Looking for resources to design of the final front-end board that will incorporate these (MRS or lab support).

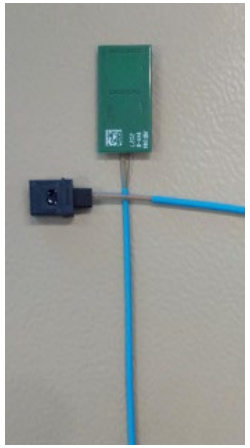
lpGBT



VTRx



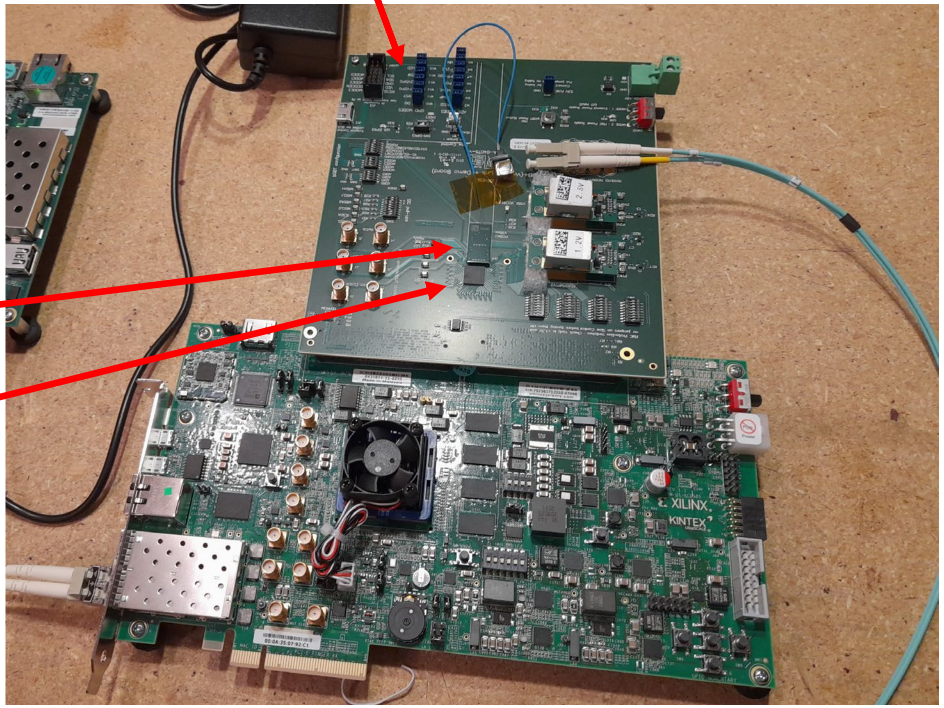
New



CERN lpGBT and VTRX+ test board

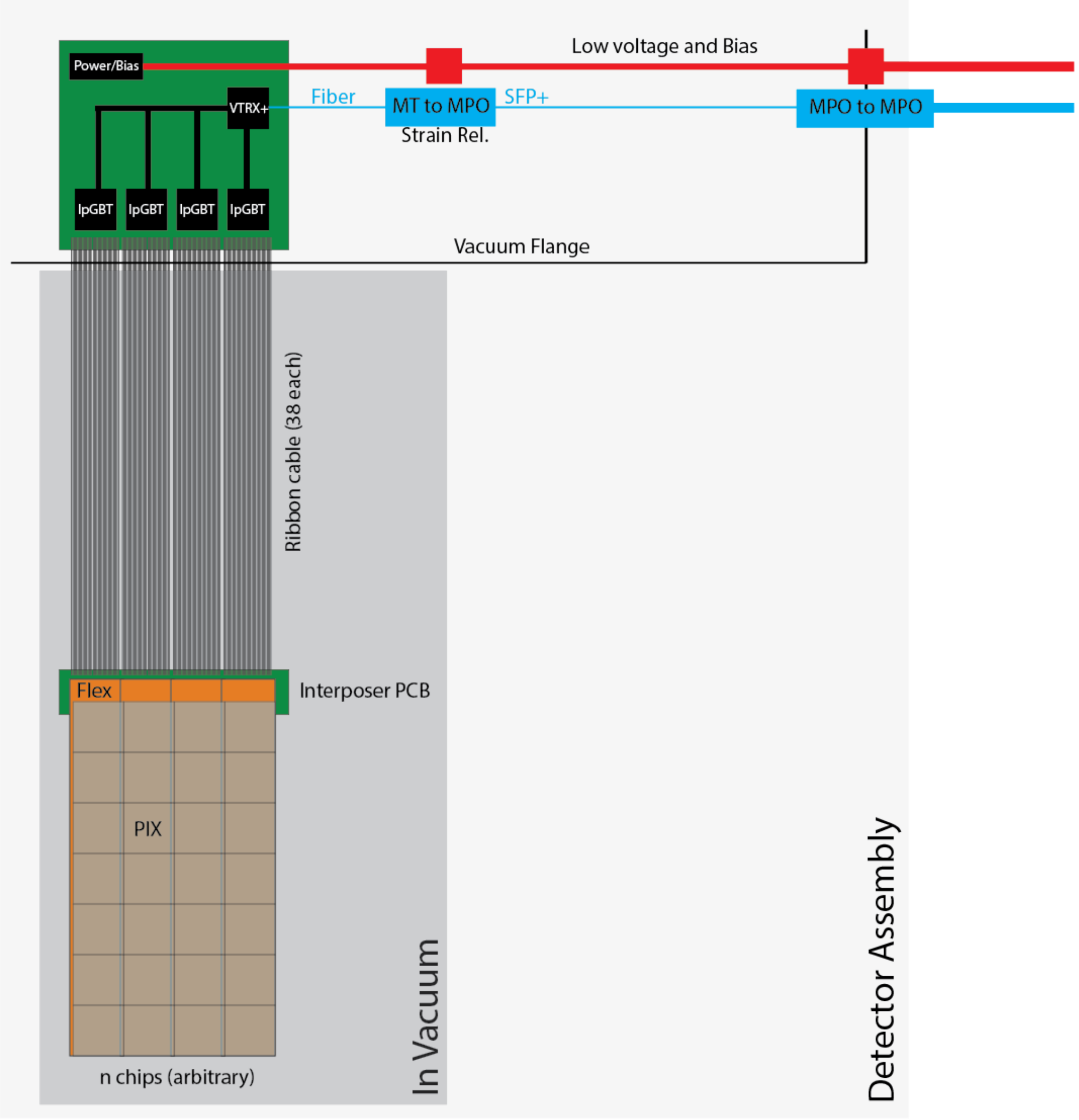
VTRX+

lpGBT



Readout Prototyping:

- Readout interface concept
- Assembly inside mounted to motion stage
- Cooling via cold-finger ribbon or direct gas/fluid (to be designed)
- No DC/DC power conversion – bias and operating voltages to be supplied directly from power supplies
- Need to know about SuperKEKB infrastructure to determine cable lengths.



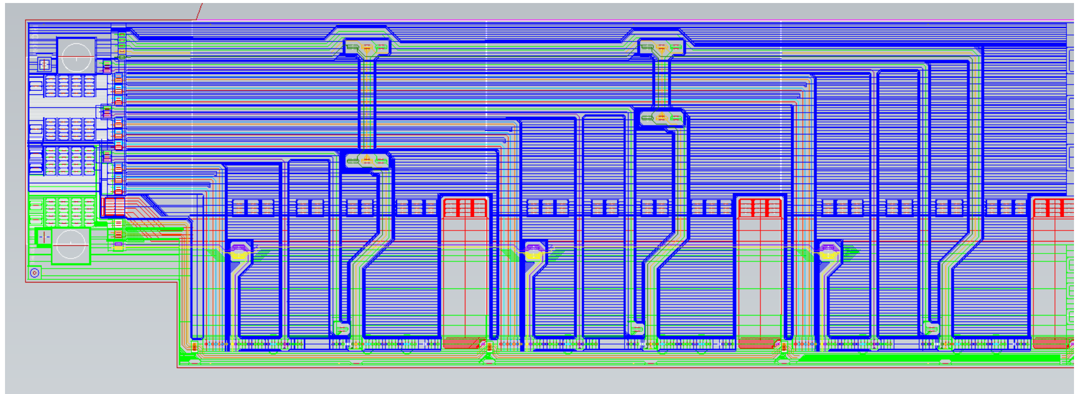
Power

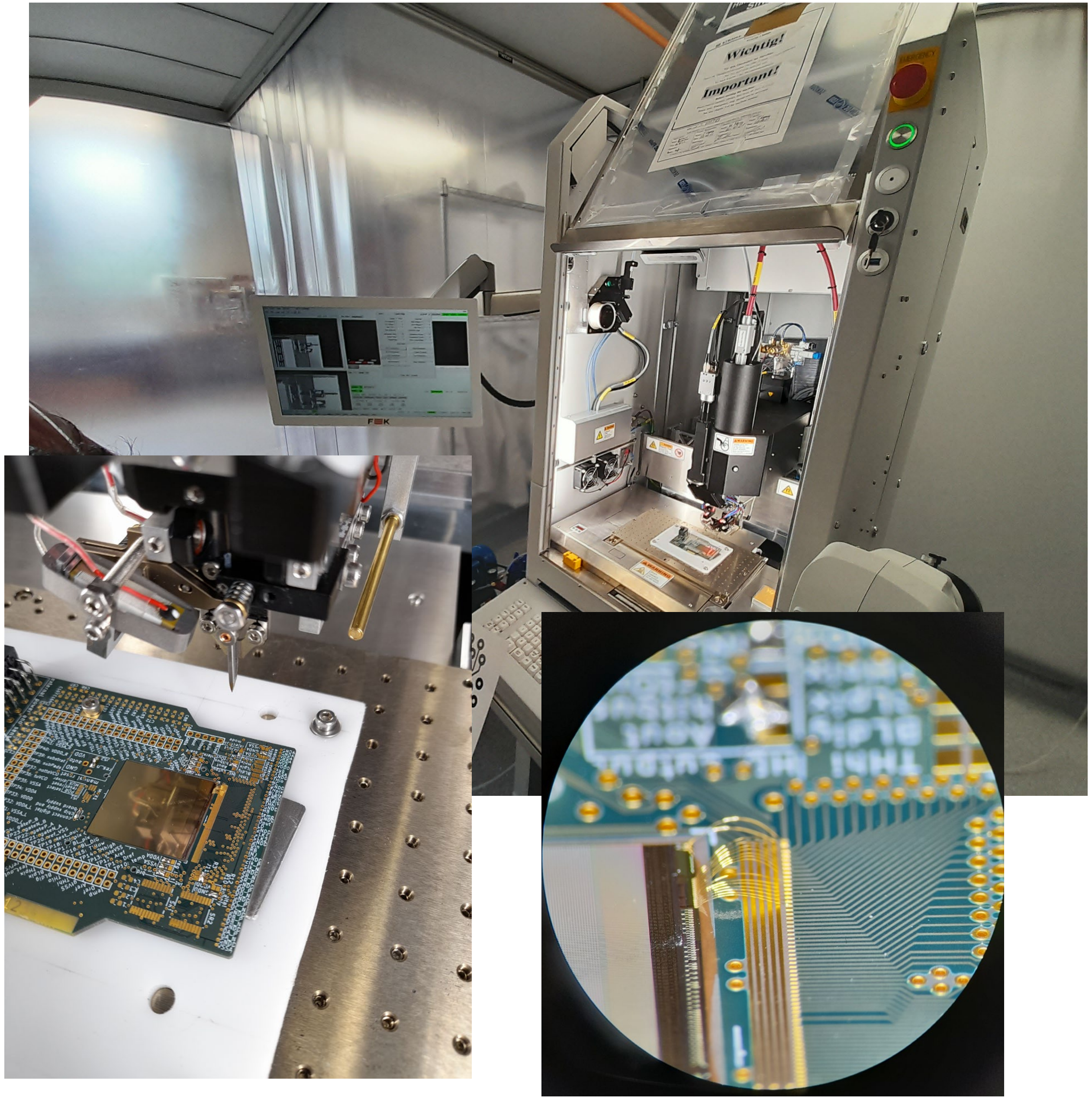
n cables w. 14 AWG , 30 ft @ (2V, 0.5 A) HVMAPS
n cables w. 14 AWG, 30 ft (return) HVMAPS
2n cables w. 23 AWG , 30 ft (2V sense and return)
2n cables w. 23 AWG , 30 ft (1.2V sense and return)
2n cables w. 23 AWG , 30 ft (2.5V sense and return)

1 cable w. 23 AWG, 30 ft (2.5V, 0.08A) VTRX+
1 cable w. 23 AWG, 30 ft (return) VTRX+
4 cables w. 14 AWG, 30 ft (1.2V, 0.33A) lpGBT, VTRX+
4 cables w. 14 AWG, 30 ft (return) lpGBT, VTRX+

Detector Prototyping:

- The Manitoba group recently purchased a chip bonder which is currently being used to bond the HVMAPS to prototype boards
- This machine will be used to build the Compton EDet planes
- Chips to be bonded to flexprint or directly to PCB, depending on bond type
- Bonding to flexprint better with spTAB – Aluminum pads





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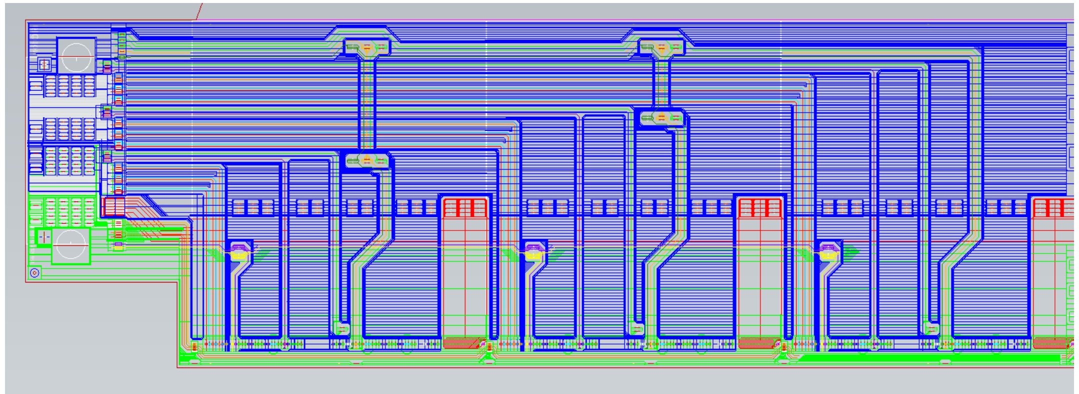

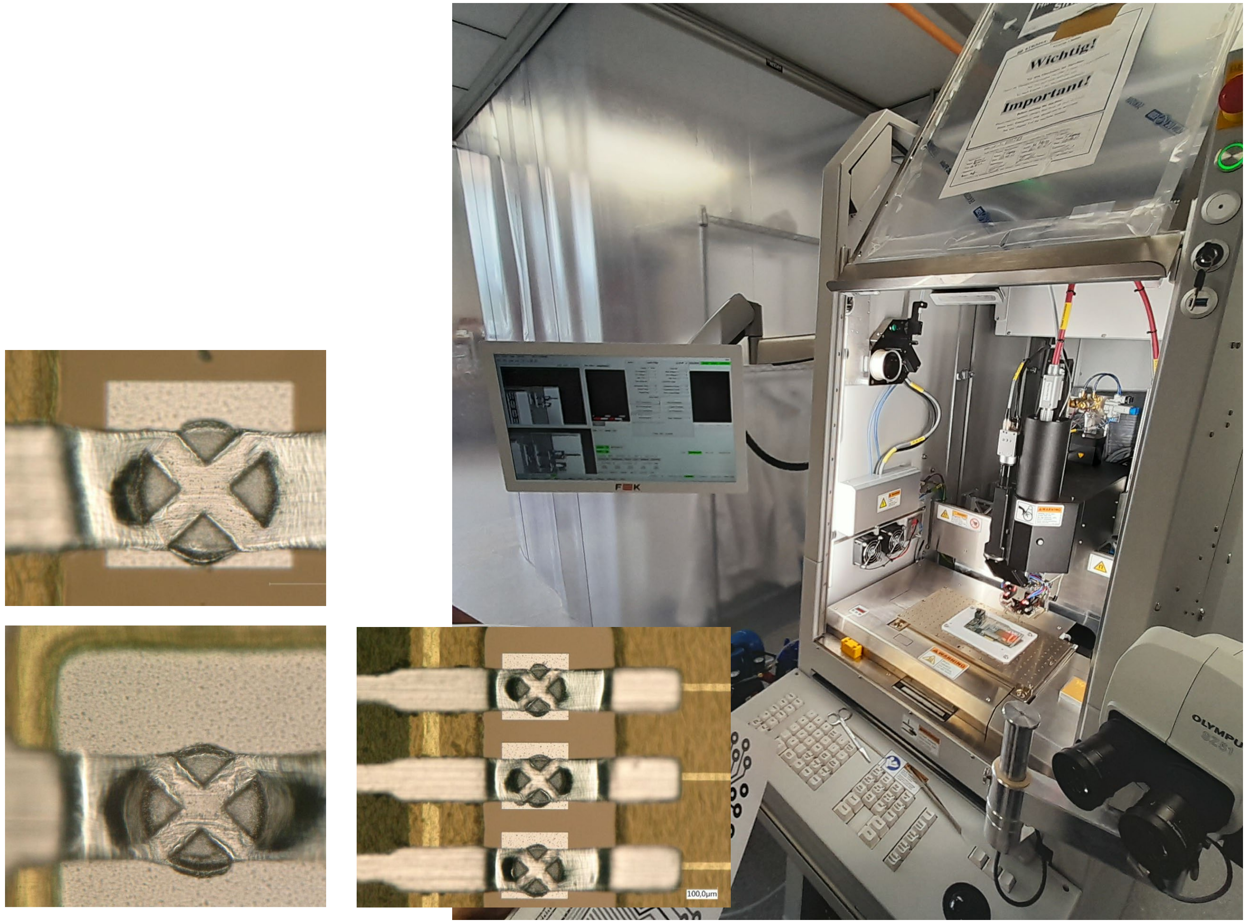

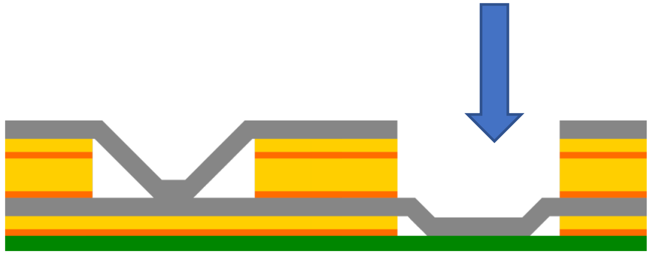

Near term development plans:

- Complete flexprint design for the 3 chip Compton ladder (issue: spTAB bonding flexprint manufacturer is located in the Ukraine – may go back to standard wedge bonding to Cu traces and pads – industry standard flexprint)

- Modify chip design to include gating option and match to lpGBT clock (depends on designer schedule) – this may not be relevant to ChiralBelle or more development may be needed for that – needs to be discussed

- Develop full prototype mounting structure for Compton E-det and redo cooling tests

- Develop prototype front-end readout board for lpGBT and VTRX+, with power distribution

- Develop vacuum enclosure and motion, cooling, and electronics feedthroughs/flange – this may not be relevant to ChiralBelle – input needed on what that design is going to look like

- Develop gluing and bonding setup for the HVMAPS flexprint / PCB to chip assembly