TOPTRG Status

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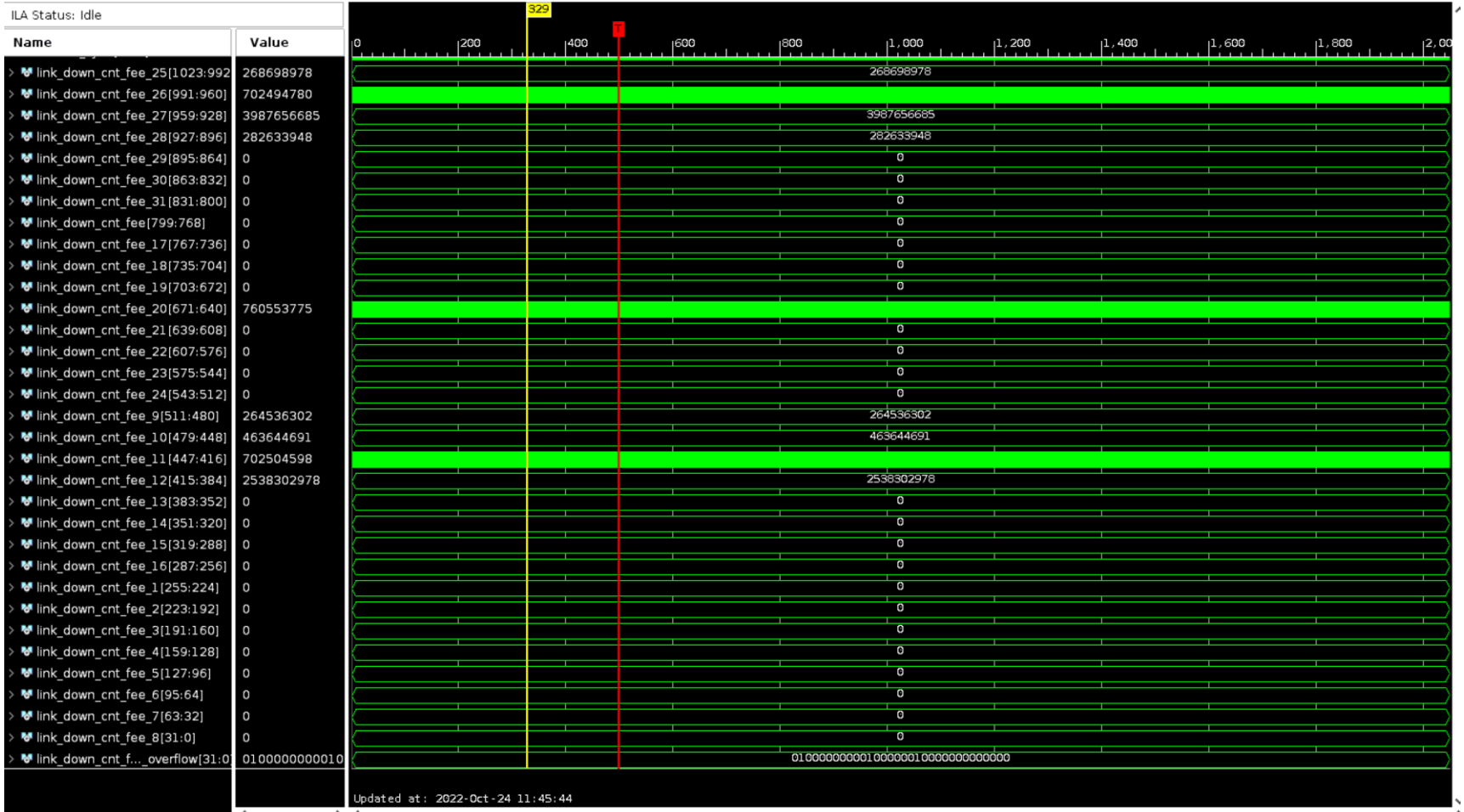
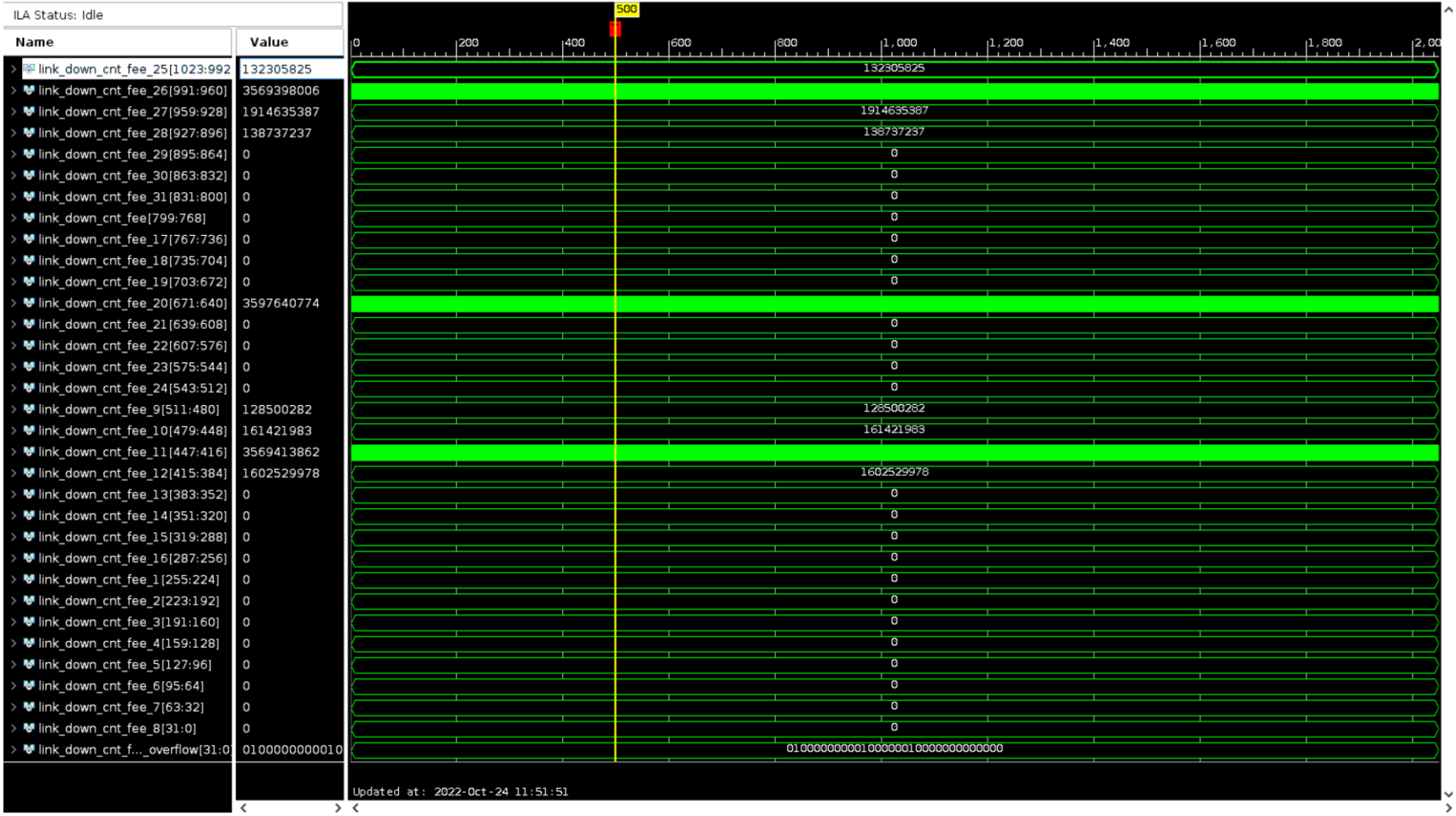
Slot 1-8 @3.9MHz – 5 minutes

s04b, s06a, s08c are broken

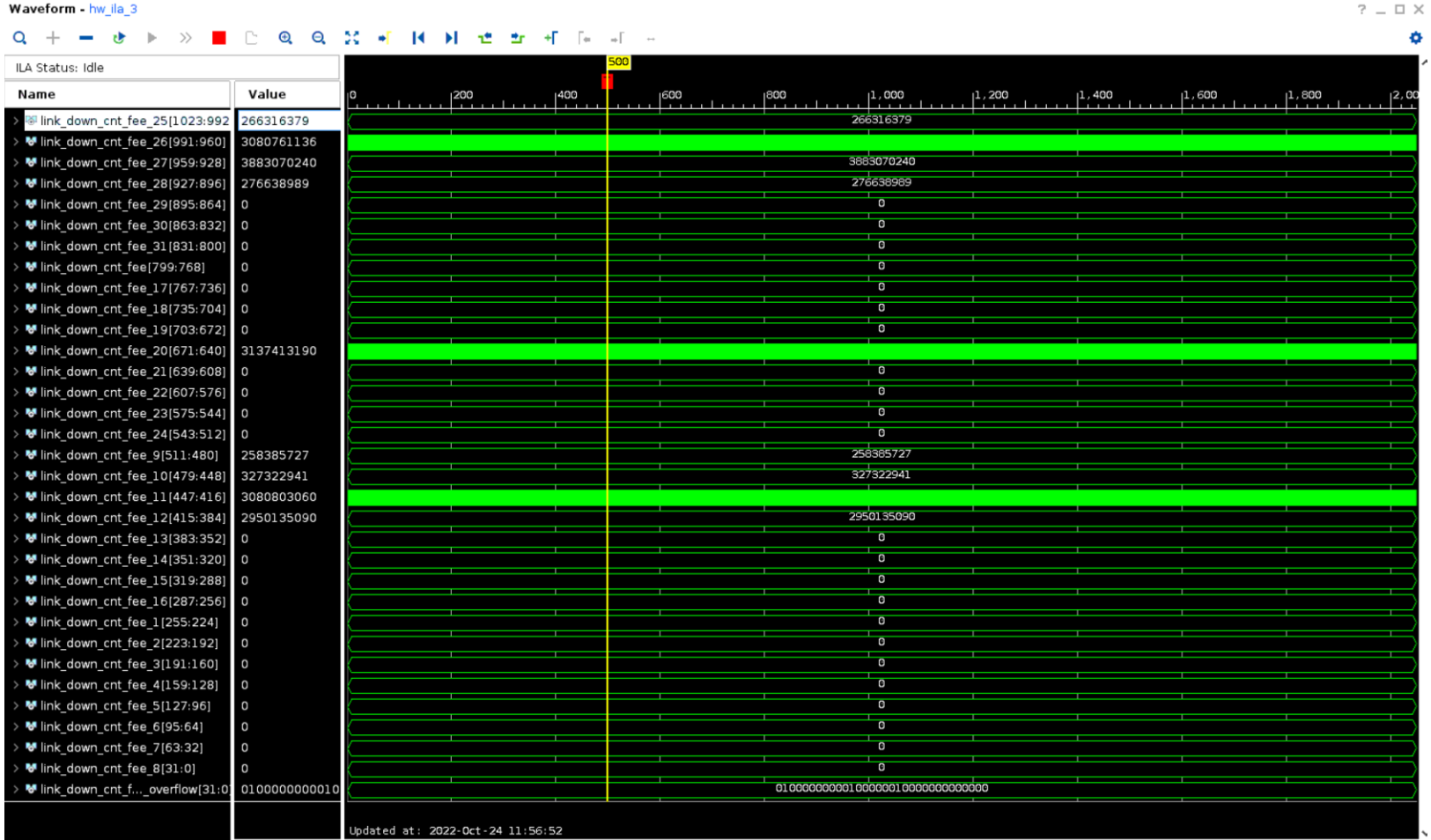
Slot 1-8 @3.9MHz – 10 minutes



Slot 1-8 @0.1MHz – 5 minutes



Slot 1-8 @0.1MHz – 10 minutes



```
assign auto_rst_0  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[0]|rx_link_up_x[1]|rx_link_up_x[2]|rx_link_up_x[3]))?1'b1:1'b0;
assign auto_rst_1  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[4]|rx_link_up_x[5]|rx_link_up_x[6]|rx_link_up_x[7]))?1'b1:1'b0;
assign auto_rst_2  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[8]|rx_link_up_x[9]|rx_link_up_x[10]|rx_link_up_x[11]))?1'b1:1'b0;
assign auto_rst_3  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[12]|rx_link_up_x[13]|rx_link_up_x[14]|rx_link_up_x[15]))?1'b1:1'b0;
assign auto_rst_4  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[16]|rx_link_up_x[17]|rx_link_up_x[18]|rx_link_up_x[19]))?1'b1:1'b0;
//assign auto_rst_5  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[20]|rx_link_up_x[21]|rx_link_up_x[22]|rx_link_up_x[23]))?1'b1:1'b0;
assign auto_rst_5  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[21]|rx_link_up_x[22]|rx_link_up_x[23]))?1'b1:1'b0;
assign auto_rst_6  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[24]|rx_link_up_x[25]|rx_link_up_x[26]|rx_link_up_x[27]))?1'b1:1'b0;
assign auto_rst_7  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[28]|rx_link_up_x[29]|rx_link_up_x[30]|rx_link_up_x[31]))?1'b1:1'b0;
```

Link down observed in slot 4 and slot 8.
No link down observed in other slots in 30 minutes @0.1/3.9MHz

The frequent link down is due to the (wrong) way of implementing auto-reset.
Current auto-reset bind the 4 channels of each slot, i.e., when one channel is down, all 4 channels are reset.
In current FW, we only exclude s06a.
However, the s04b and s08c broke recently and we did not handle it in the TOPTRG FW.
That's why s04a/c/d, s08a/b/d are reset from time to time.

Current broken boardstacks: s04b, s06a, s08c, s13d

10 min	Down count	rate
s05a	2950135090	3.87%
s05b	N/A	N/A
s05c	327322941	0.43%
s05d	258385727	0.34%

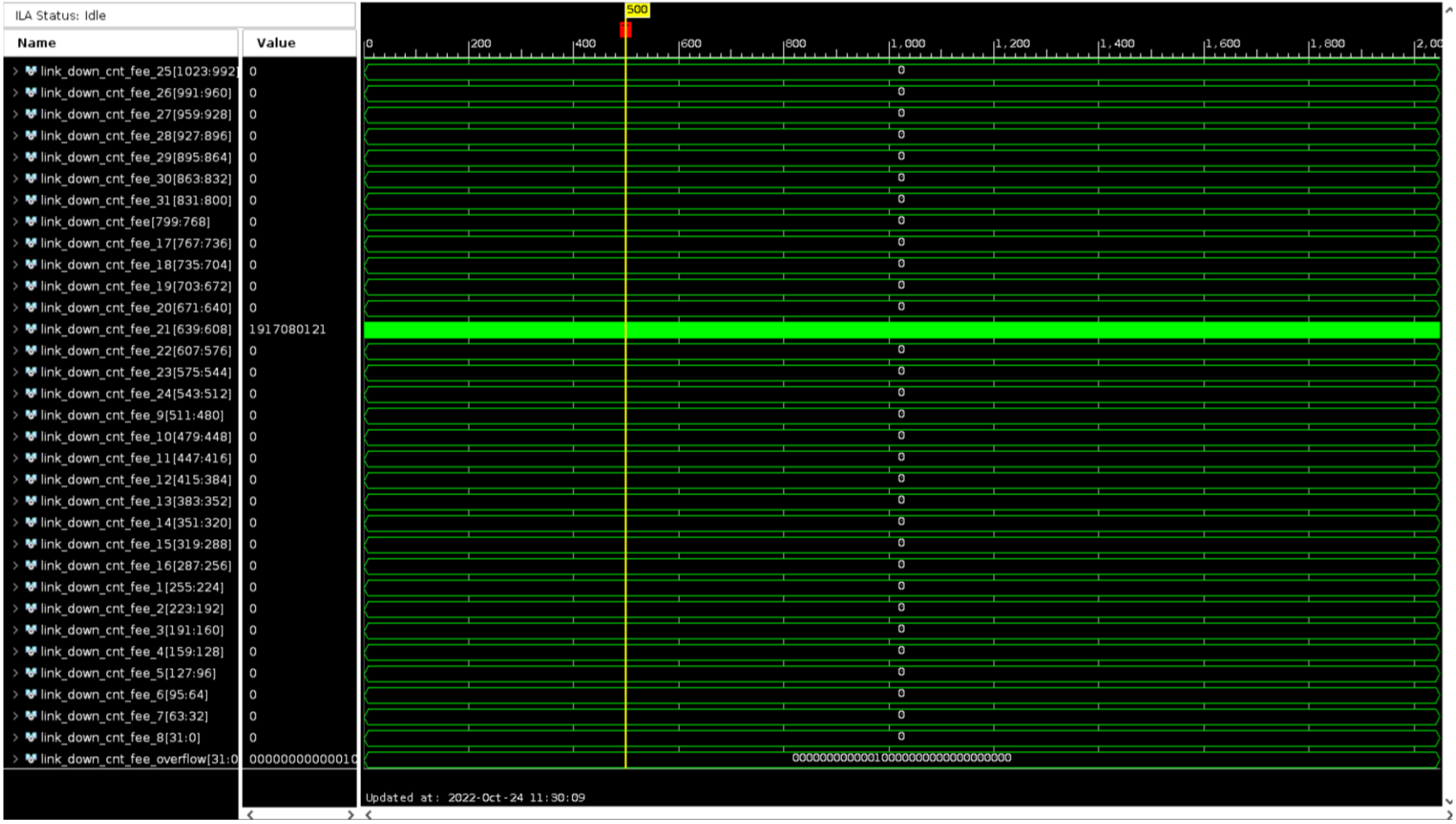
5 min	Down count	rate
s05a	1364217525	3.58%
s05b	N/A	N/A
s05c	232915991	0.61%
s05d	131476210	0.34%

10 min	Down count	rate
s08a	276638989	0.36%
s08b	3883070240	5.09%
s08c	N/A	N/A
s08d	266316379	0.35%

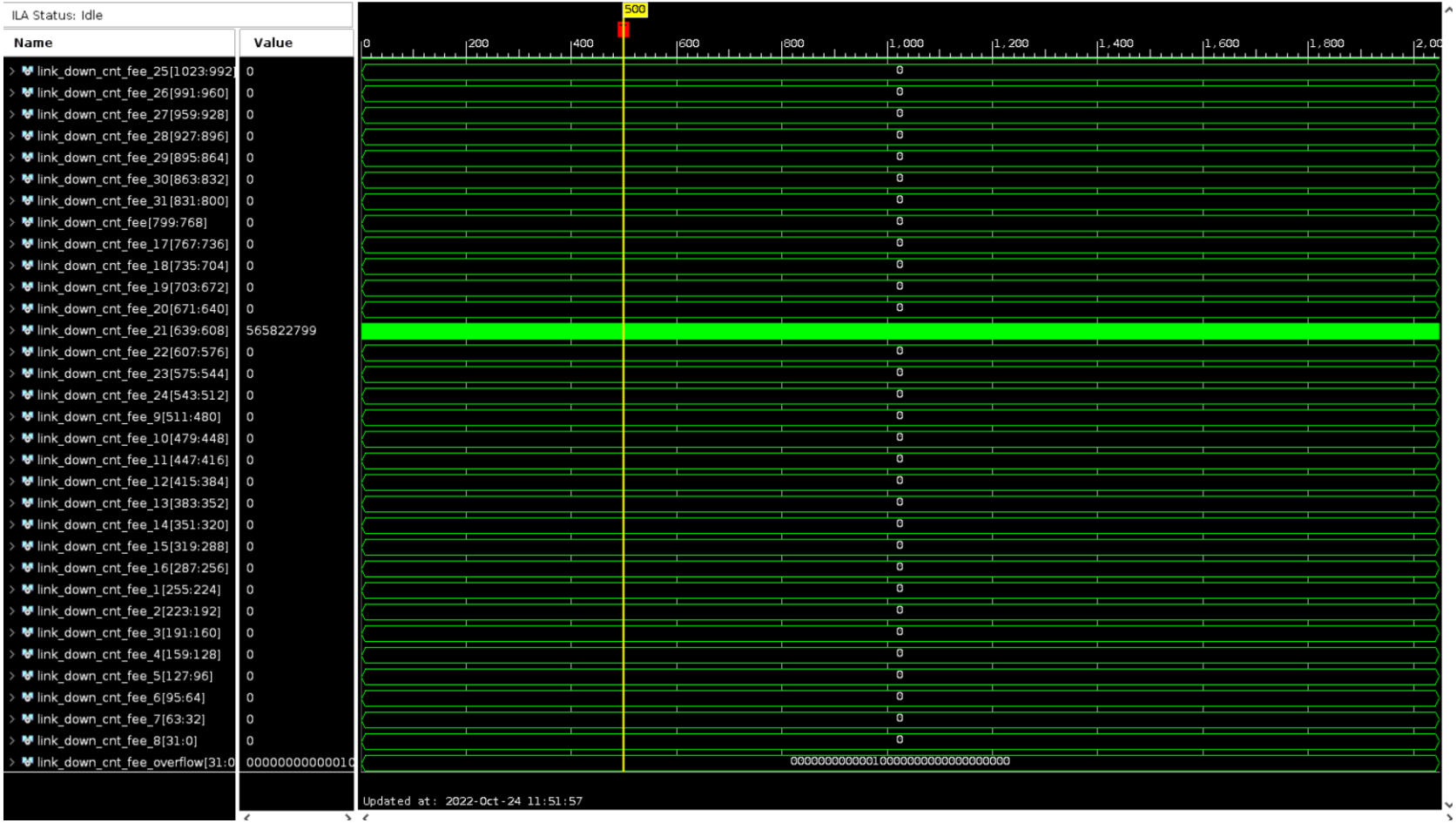
5 min	Down count	rate
s08a	141042124	0.37%
s08b	1654864223	4.34%
s08c	N/A	N/A
s08d	134314311	0.35%

Differences between Link down rates measured in 5-min test and 10-min test are due to manual timing.

Slot 9-16 @3.9MHz – 30 minutes



Slot 9-16 @0.1MHz – 30 minutes



```
assign auto_rst_0  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[0]|rx_link_up_x[1]|rx_link_up_x[2]|rx_link_up_x[3]))?1'b1:1'b0;
assign auto_rst_1  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[4]|rx_link_up_x[5]|rx_link_up_x[6]|rx_link_up_x[7]))?1'b1:1'b0;
assign auto_rst_2  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[8]|rx_link_up_x[9]|rx_link_up_x[10]|rx_link_up_x[11]))?1'b1:1'b0;
assign auto_rst_3  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[12]|rx_link_up_x[13]|rx_link_up_x[14]|rx_link_up_x[15]))?1'b1:1'b0;
//assign auto_rst_4  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[16]|rx_link_up_x[17]|rx_link_up_x[18]|rx_link_up_x[19]))?1'b1:1'b0;
assign auto_rst_4  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[16]|rx_link_up_x[17]|rx_link_up_x[18]))?1'b1:1'b0;
assign auto_rst_5  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[20]|rx_link_up_x[21]|rx_link_up_x[22]|rx_link_up_x[23]))?1'b1:1'b0;
assign auto_rst_6  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[24]|rx_link_up_x[25]|rx_link_up_x[26]|rx_link_up_x[27]))?1'b1:1'b0;
assign auto_rst_7  = ((rst_cnt>5 && rst_cnt<25)&&(rx_link_up_x[28]|rx_link_up_x[29]|rx_link_up_x[30]|rx_link_up_x[31]))?1'b1:1'b0;
```

No link down observed in 30 minutes @0.1/3.9MHz

For slot 9-16, the only broken s13d is handled correctly.

Current broken boardstacks: s04b, s06a, s08c, s13d

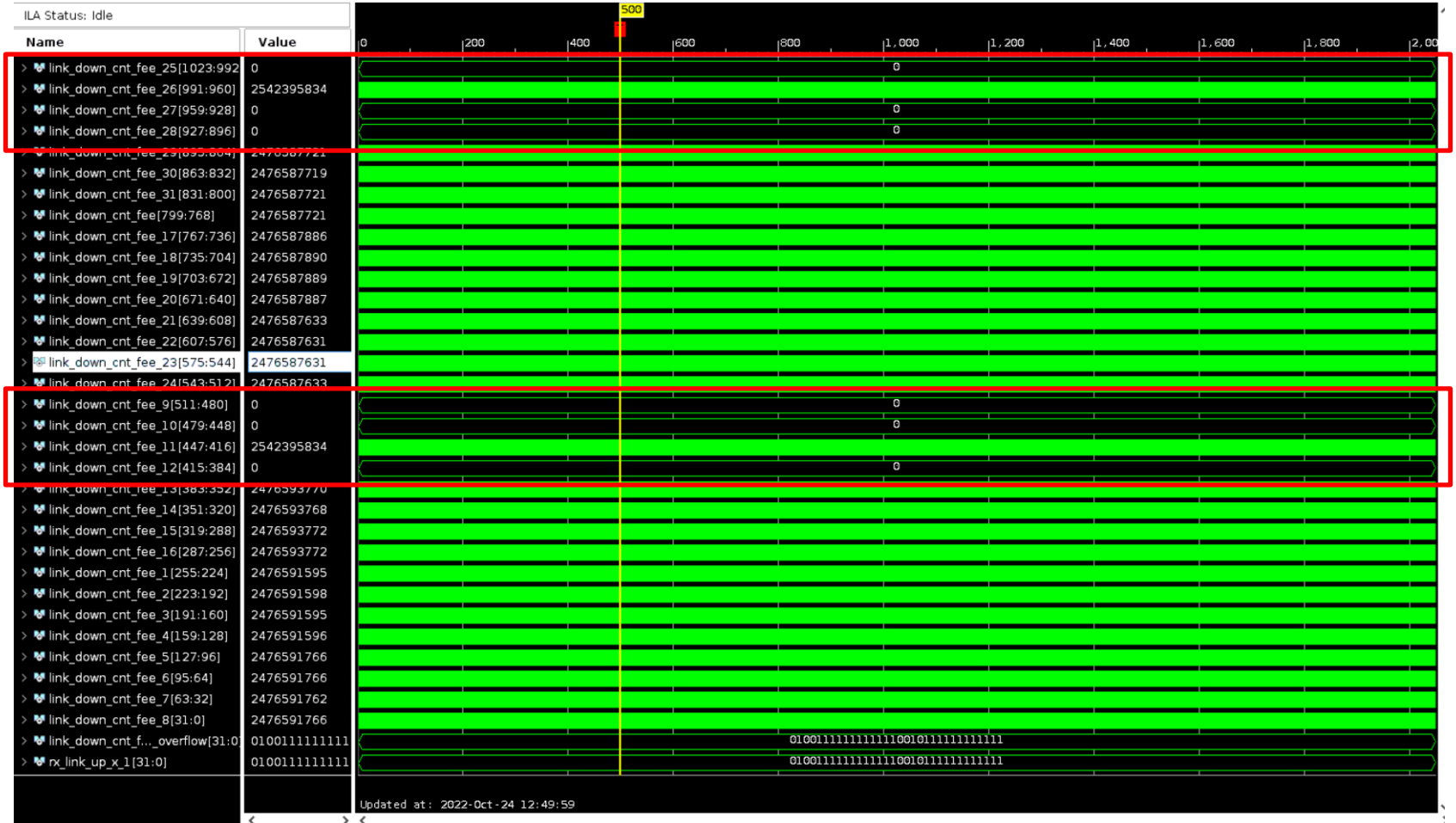
Slot 4/8 test
New FW (auto-rst fixed)

Slot 1-8 @3.9MHz – 30 minutes

No link down after fixing auto rest

Slot 1-8 @0.1MHz – 30 minutes

No link down after fixing auto rest



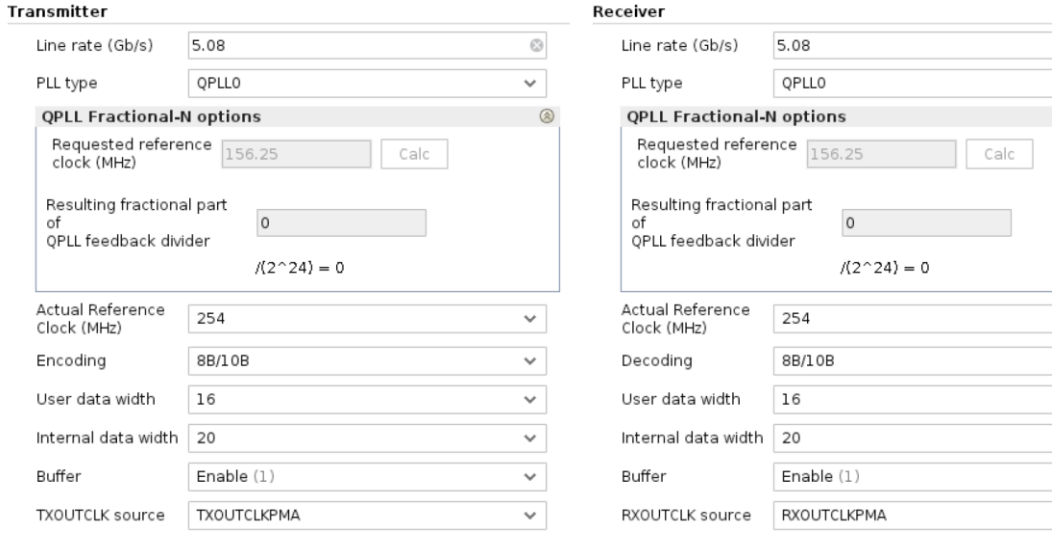
TOPTRG->GDL/GRL link

```
gth_8b10b_top_TOPoutput_5g gth_1
(
    .dataflow_stage(1'b0),
    //.TXUSERCLK(),
    //.RXUSERCLK(),
    .global_state(3'b010),
    .global_reset(1'b0),
    //.global_reset(global_reset_gth1),

    .LANE_UP(gth1_lane_up),
    .TX_DST_RDY_N(tx_dst_rdy_n_gth1),
    .TX_SRC_RDY_N(tx_src_rdy_n_gth1),
    .RX_SRC_RDY_N(rx_src_rdy_n_gth1),

    .mgtrefclk0_x0y0_p(GTH_REFCLK_P[0]),
    .mgtrefclk0_x0y0_n(GTH_REFCLK_N[0]),
    .RXN_IN(GTH_RX_N[3:0]),
    .RXP_IN(GTH_RX_P[3:0]),
    .TXN_OUT(GTH_TX_N[3:0]),
    .TXP_OUT(GTH_TX_P[3:0]),
    .rxpolarity_in(4'b0000),
    .txpolarity_in(4'b0000),

    .hb_gtwiz_reset_clk_freerun_in(clk_63),
    .dataclk(clk_127),
    .wr_req_TXFIFO(wr_req_gth1),
    .data_32b_to_lane0(data_32b_to_gth1_lane0),
    .data_32b_to_lane1(data_32b_to_gth1_lane1),
    .data_32b_to_lane2(data_32b_to_gth1_lane2),
    .data_32b_to_lane3(data_32b_to_gth1_lane3)
);
```



Left UT4:
GTH port 1 -> GRL

Right UT4:
GTH port 1 -> GRL
GTH port 2 -> GDL

Protocol:
UT4/FPGA/Library/libut4_02/OPT/8B10B

GTH optical module I2C control:
UT4/FPGA/gth_0-3_15g/rtl/reg_ctrl.v

TOPTRG->GDL/GRL link

```
// Test pattern by Tianping Oct 25, 2022
always@(posedge clk_127) begin
    if( rst_fsm ) begin
        wr_req_gth1 <= 1'b0;
        data_32b_to_gth1_lane0 <= 32'h0;
        data_32b_to_gth1_lane1 <= 32'h1;
        data_32b_to_gth1_lane2 <= 32'h2;
        data_32b_to_gth1_lane3 <= 32'h3;
    end
    else begin
        wr_req_gth1 <= 1'b1;
        data_32b_to_gth1_lane0 <= data_32b_to_gth1_lane0 + 1;
        data_32b_to_gth1_lane1 <= data_32b_to_gth1_lane1 + 1;
        data_32b_to_gth1_lane2 <= data_32b_to_gth1_lane2 + 1;
        data_32b_to_gth1_lane3 <= data_32b_to_gth1_lane3 + 1;
    end
end
```