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SI LAB Silizium Labor Bonn

Belle II Germany

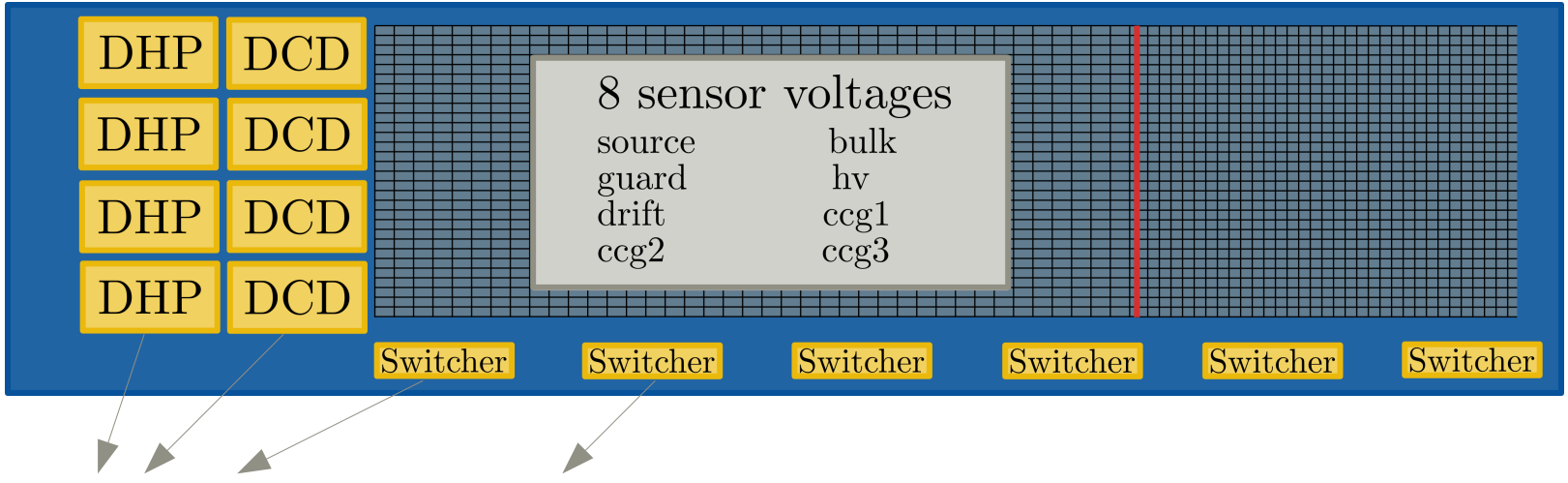
J.Schmitz, P. Ahlburg, F. Bernlochner, J. Dingfelder, H. Krüger, B. Paschen, B.Spruck
P. Wolf

PXD Power Supply - Over Voltage Protection (OVP) Studies

Belle II Germany Meeting 2023

September 26, 2023

PXD POWER REQUIREMENTS



9 ASIC voltages

sw-dvdd / sw-sub / sw-refin
dcd-avdd / dcd-dvdd / dcd-refin / dcd-amplow
dhp-io / dhp-core

6 steering voltages

gate-on1 / gate-on2 / gate-on3 / gate-off
clear-on / clear-off

→ **23 voltages** must be supplied to each PXD module

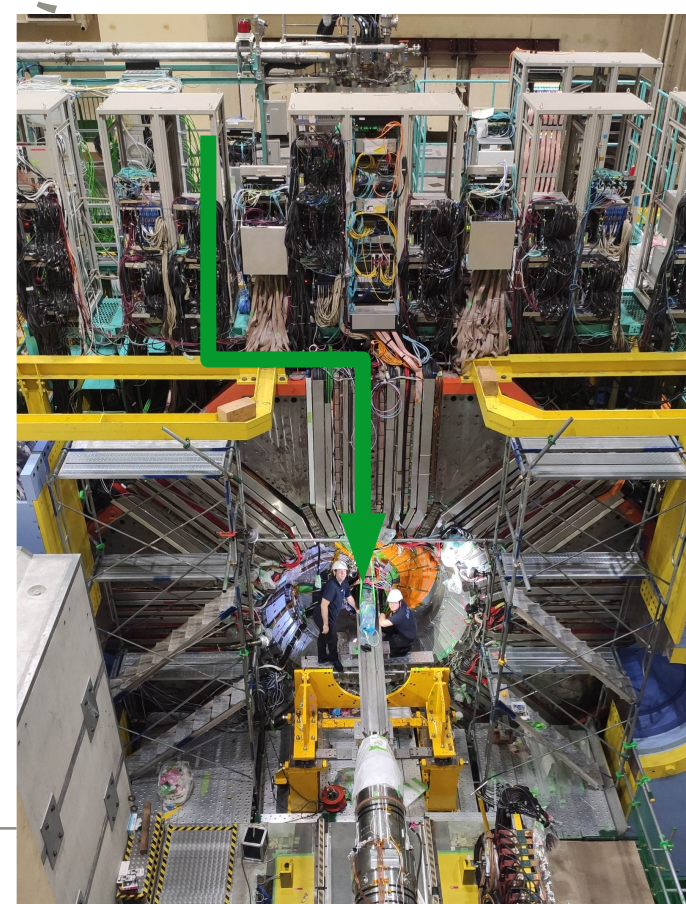
PXD POWERSUPPLY REQUIREMENTS

- Need 23 voltages, ranging from – 80V to + 20V with additional dependencies
- Currents up to 3A
- Enabling of hardware current limits
- Supplied via 15m long cables from top of Belle II

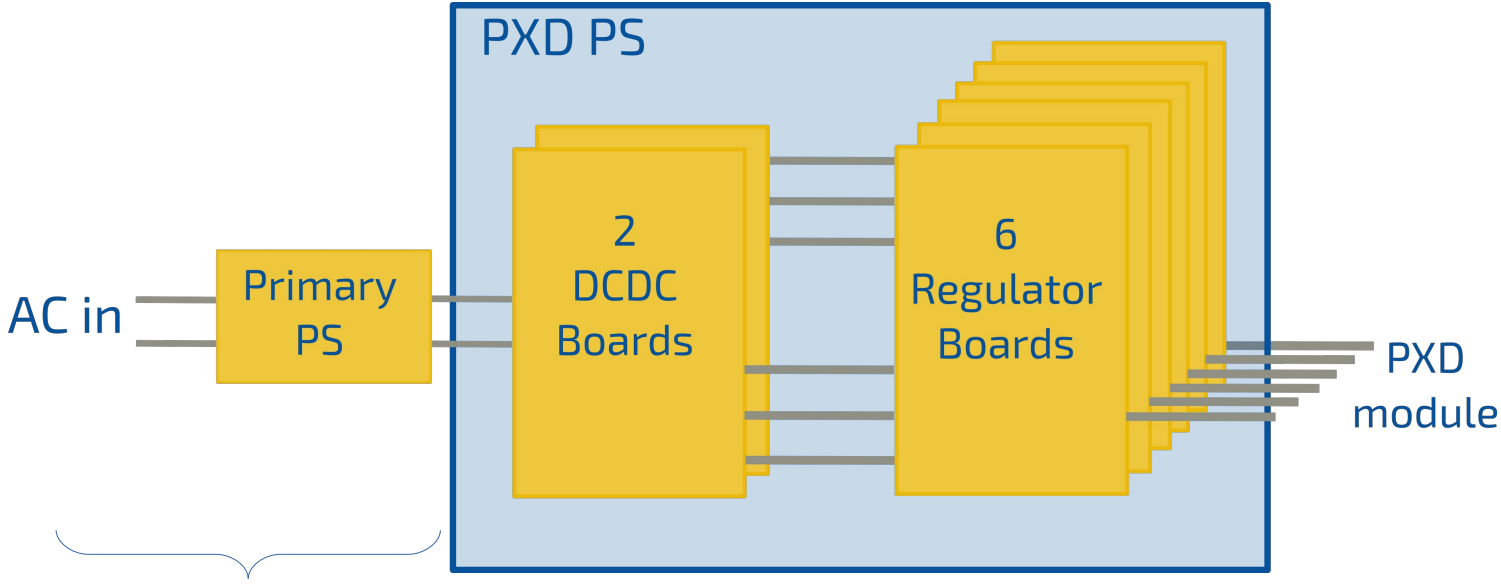
  → Compensate for voltage drop

  → 4-wire sensing and stable regulation

→ No commercial solution fulfilled all necessary features



PS SYSTEM ARCHITECTURE



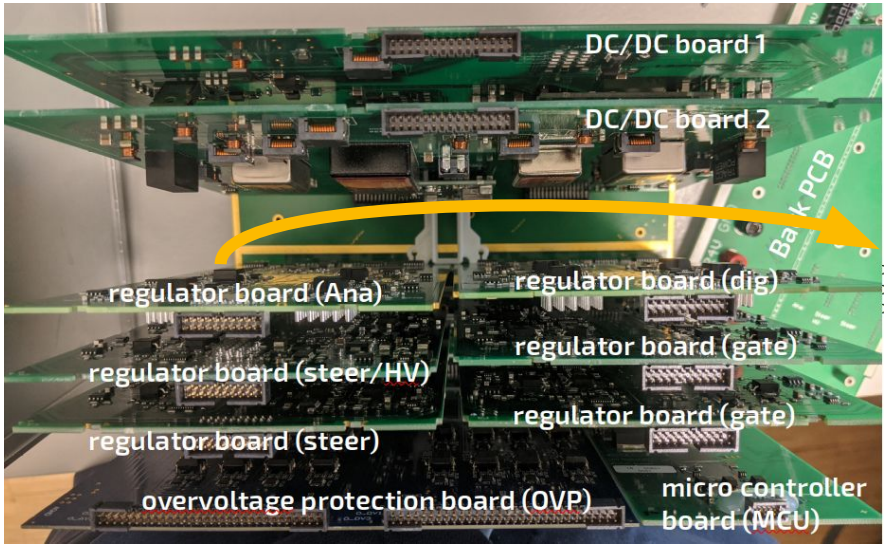
- AC/DC conversion
- NetV → 24V LV

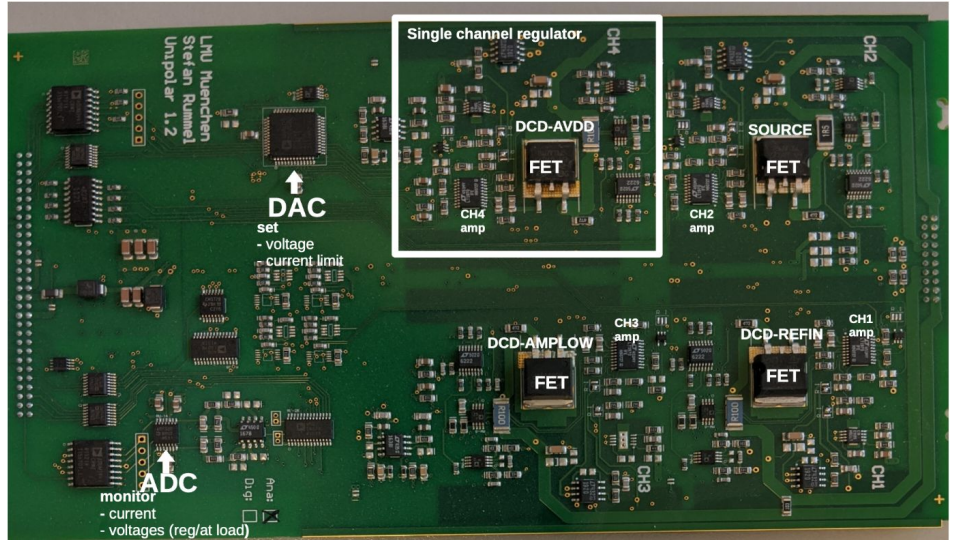
(Commercial component)

- DC/DC conversion for secondary voltages
- Electrical isolation

- Linear post regulation
- Readback of volt. & current
- Limiting of volt. & current

PXD PS INSIGHTS

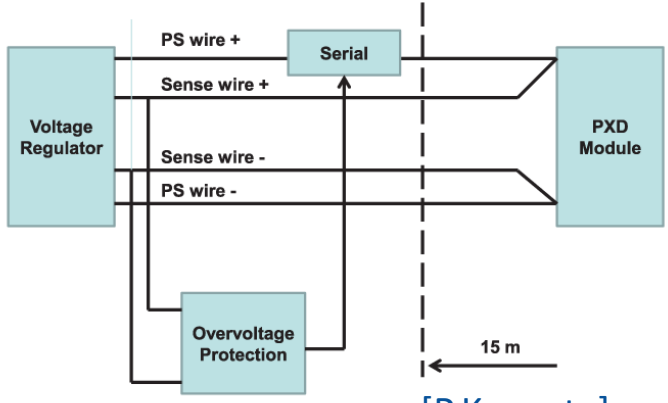




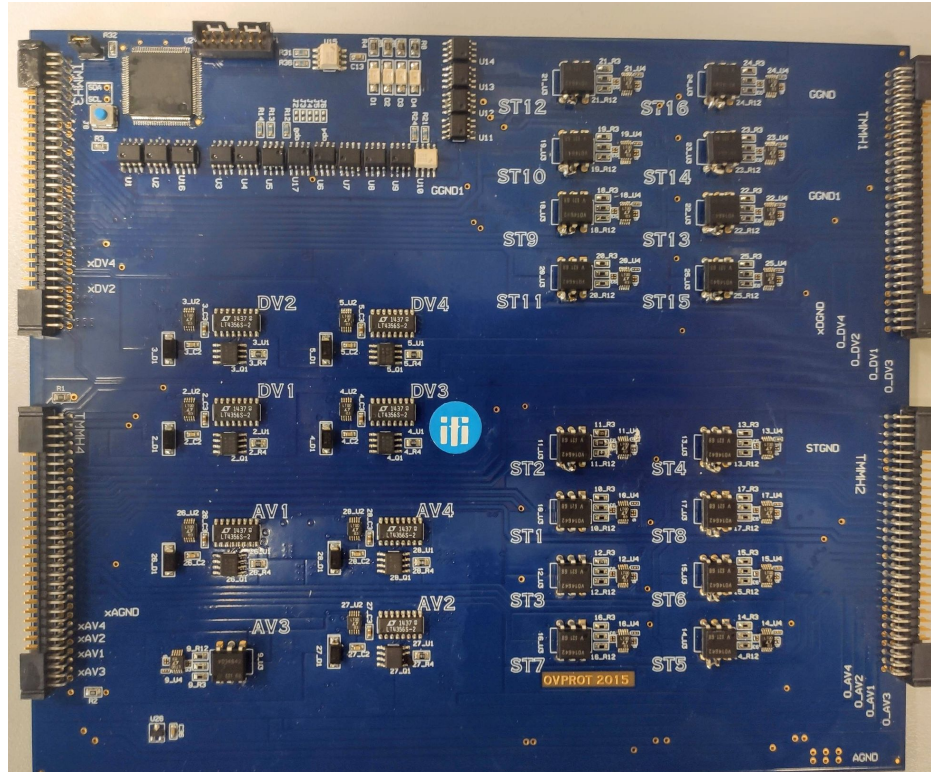
- 1 micro controller per PS performing all control and monitoring functions
- OVP board with protecting circuitry for each supply channel

OVER VOLTAGE PROTECTION LAYOUT

- **Protects** the detector and associated electronics (ASICs) against over-voltage/under-voltage conditions
- OVP board protects **24 conditions (23 voltage channels)**



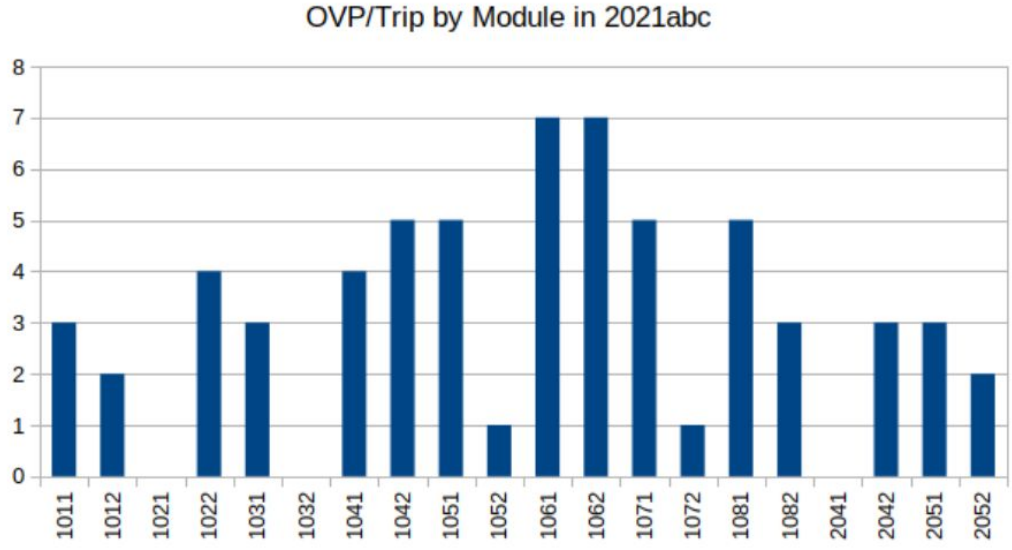
[P.Kapusta]



OVP ISSUES AT BELLE II

- OVP events ("***HV Trip***") rate increased in spring 2021 (beam currents were increased)
- Rate approx. 0.5-1 per day

  → Rises with increasing luminosity
- Talks by Björn Spruck:
  - PXD HV "Trips" Issues By Over-Voltage-Protection (link)
  - Update on PXD HV "Trips" Issues By Over-Voltage-Protection (link)



[B.Spruck]

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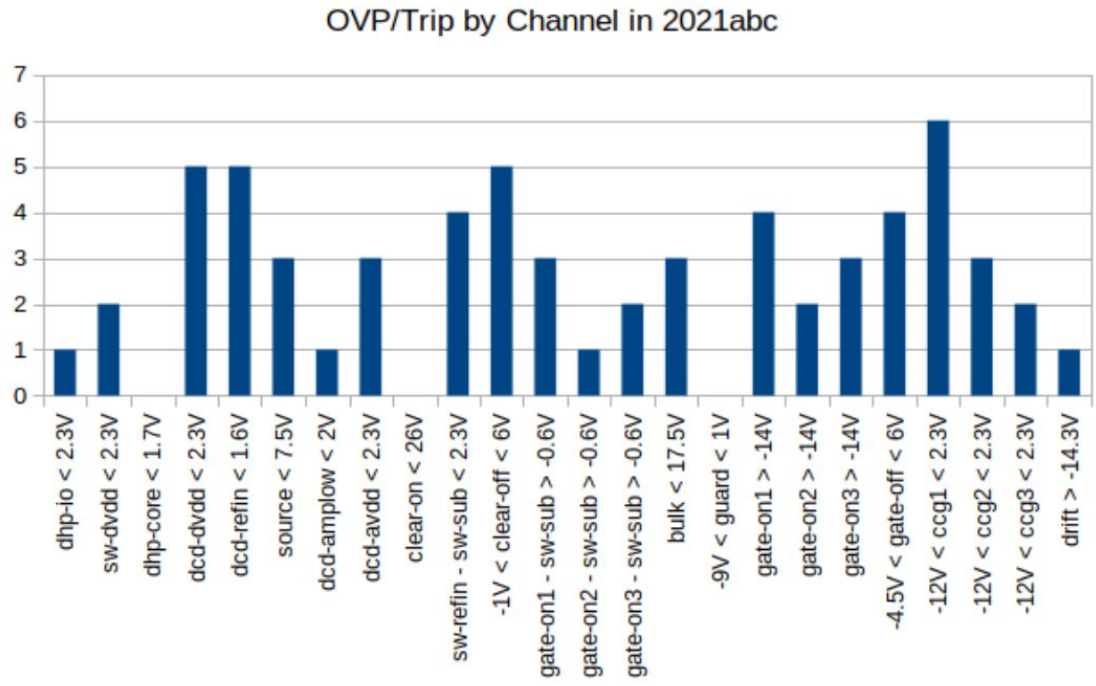

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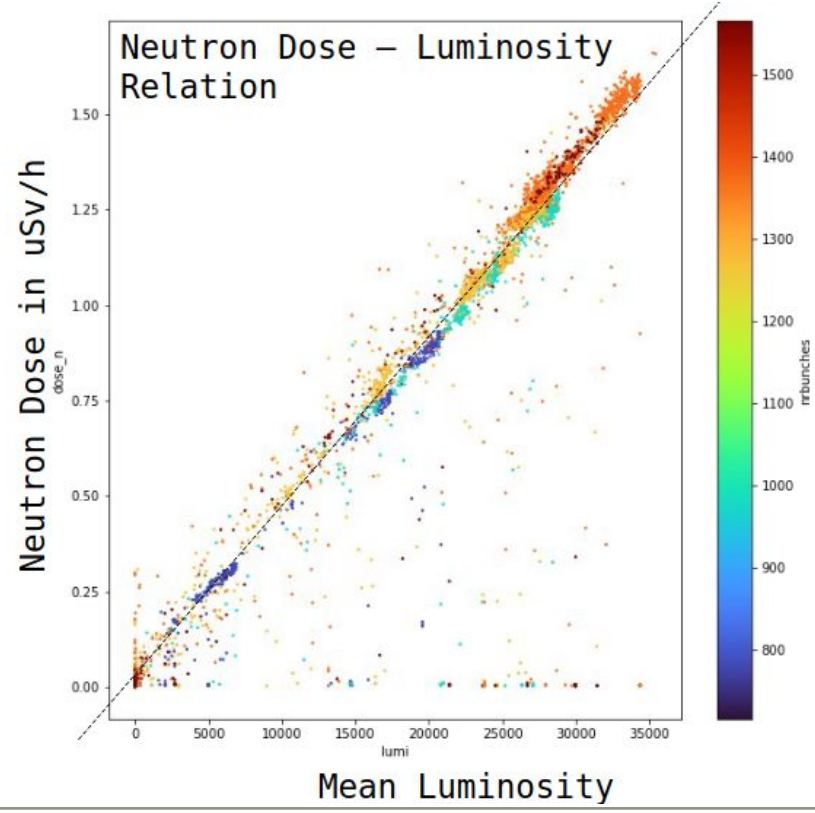

[B.Spruck]

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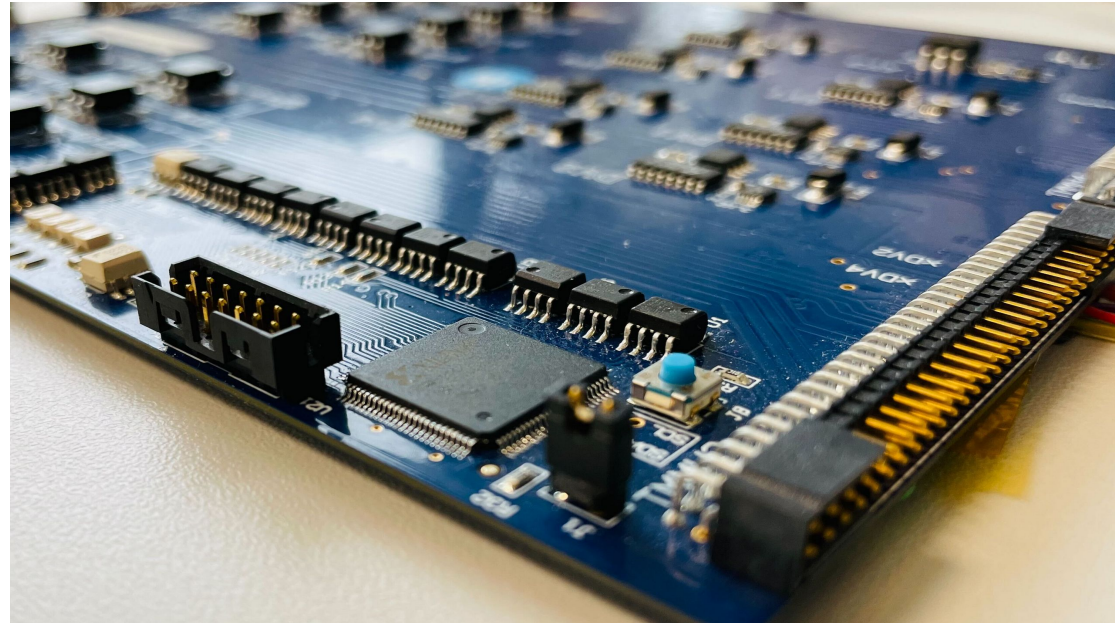
POSSIBLE REASONS FOR OVP EVENTS

- **Observation**: OVP events occur even when voltage regulators are switched off
- Effect of radiation on the logic can cause triggering of OVP events
- **Single Event Upsets (SEUs)** can trigger an OVP event
- Vulnerable to these events: Control logic implemented in the **Complex Programmable Logic Device (CPLD)**



CPLD on the OVP board

CPLD CONTROL LOGIC BEFORE

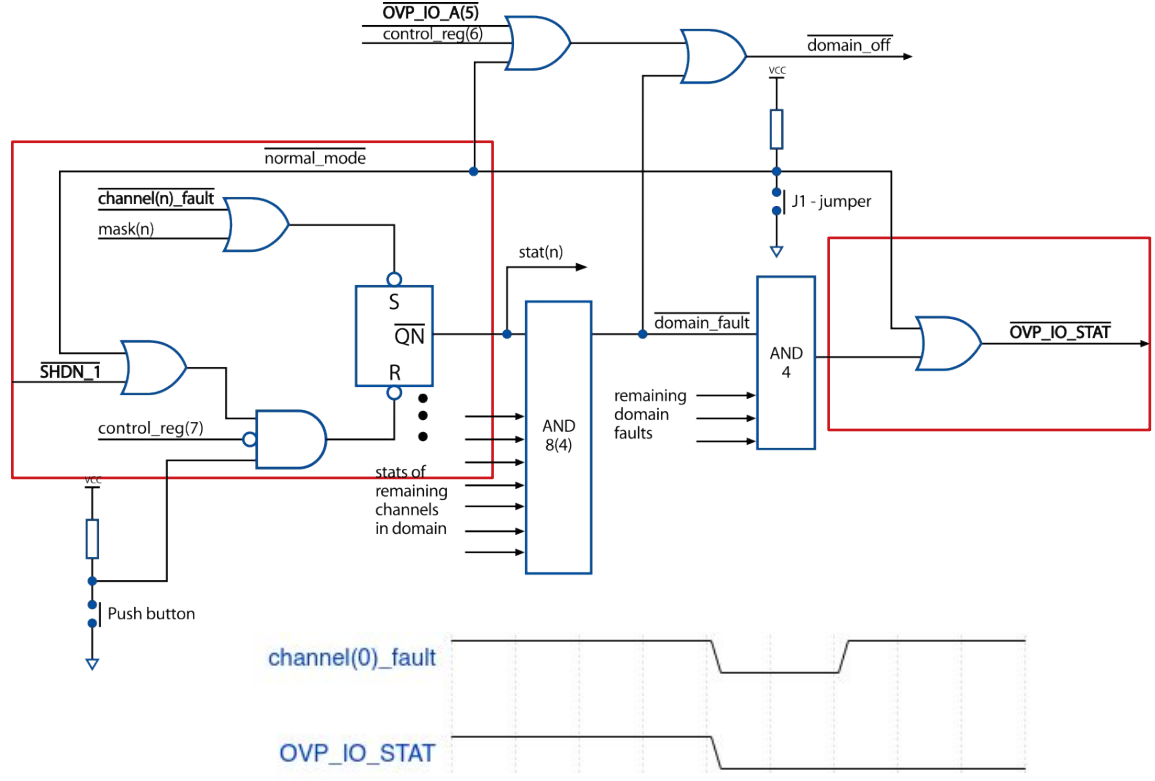
- Control logic in the CPLD:

  1. After detecting an error condition in a channel, ***channel(n)_fault*** is received

  2. The signal is fed into an asynchronous latch (set *S*)

  3. A general fault signal is sent: ***OVP_IO_STAT***

  4. An “emergency off” is issued



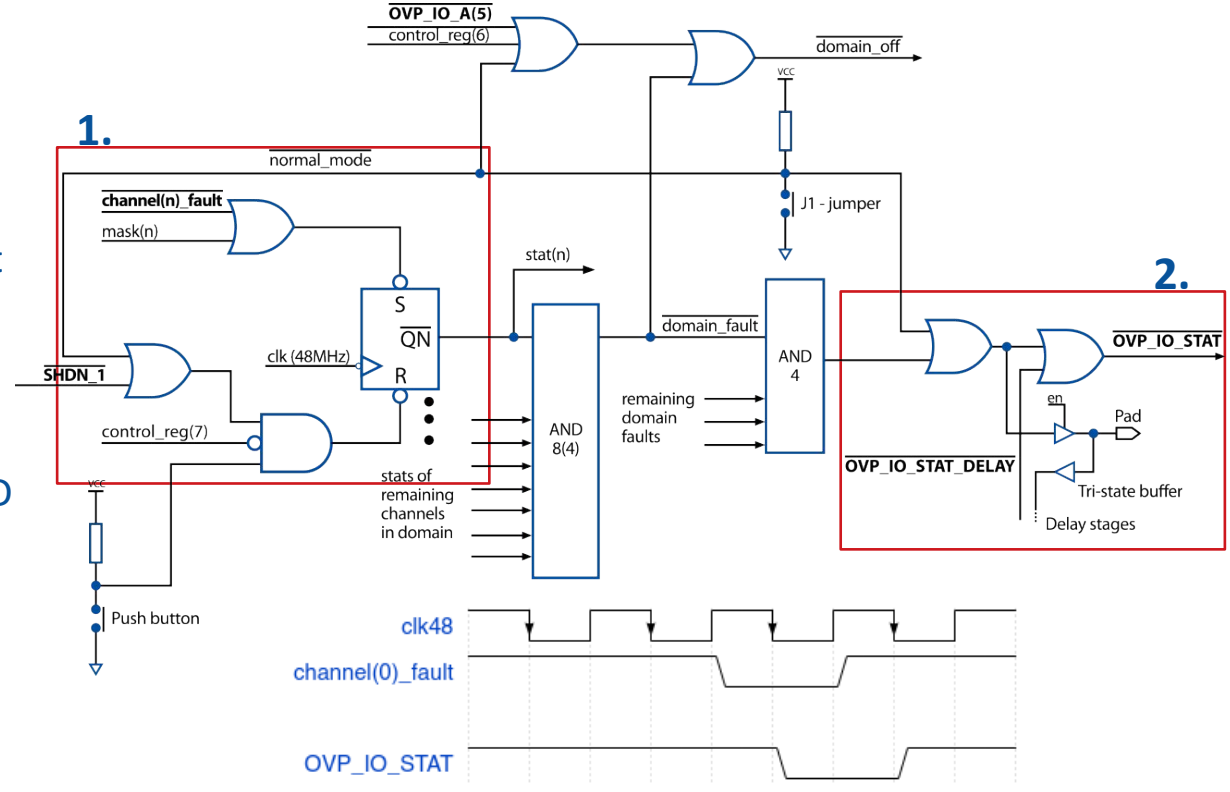
CPLD CONTROL LOGIC AFTER

- Countermeasures against SEUs:

  1. Use of a **flip-flop (clocked)** instead of latch: reduces the probability of triggering on a short fault signal / resets state after SEU

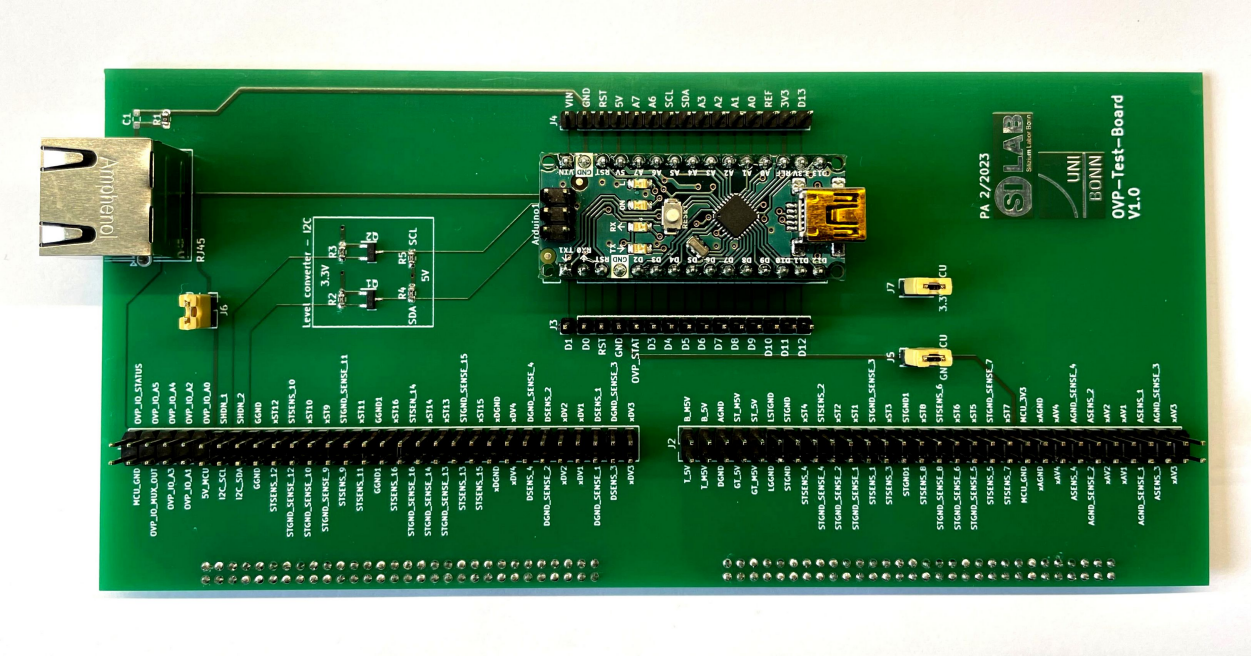
  2. **Pulse length filter** for ***OVP_IO_STAT*** signal to prevent short pulse signals within the CPLD

- Clock frequency is transmitted from second CPLD via an existing line



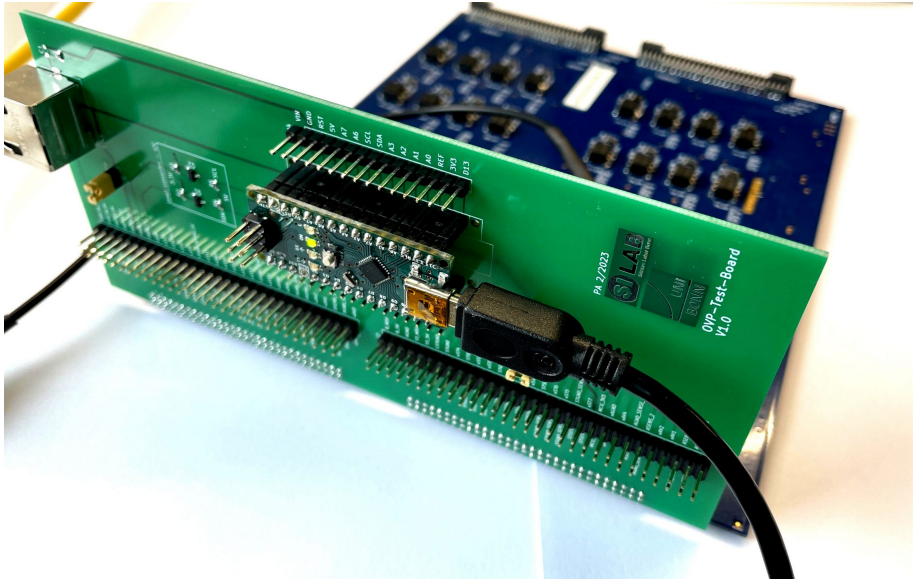
OVP-TEST-BOARD

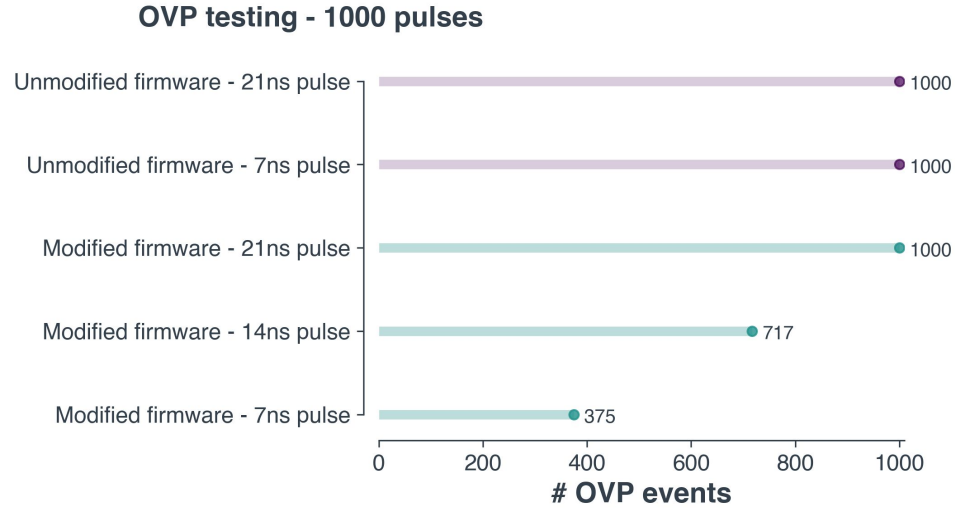
- Logic behavior tested in simulations
- **OVP-Test-Board** designed for stand-alone OVP tests
  - Houses an *Arduino Nano*
  - Communicate with auxiliary CPLD (via ***I2C***) -> status of individual channels, write masks or reset the control logic
- Signals on the OVP board can be measured



OVP-TEST-BOARD MEASUREMENTS

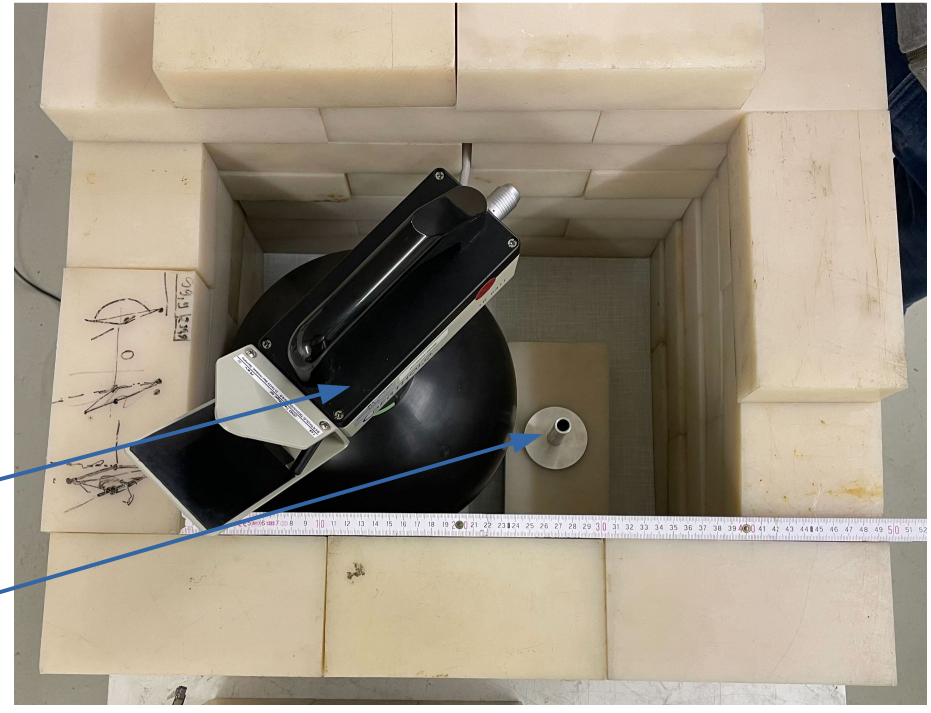
- Injecting short pulses to ***channel_fault***





VERIFICATION – NEUTRON SOURCE

- **Goal:** Verify that changes in logic lead to a reduction in OVP events by SEU
- Neutron source measurement at Helmholtz-Institut für Strahlen- und Kernphysik (HISKP) in Bonn
- Measured 303 muSv/h (distance 17.5cm)
- Duration of the measurement: 18 h



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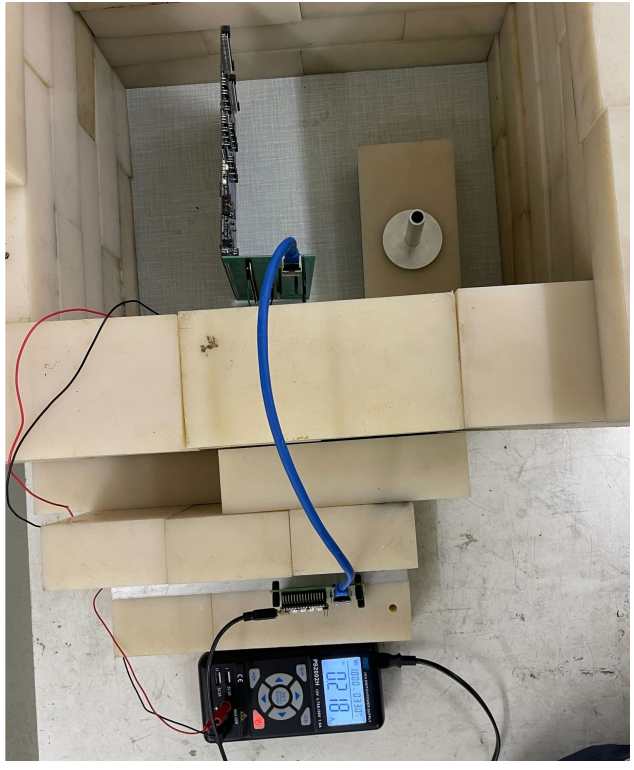

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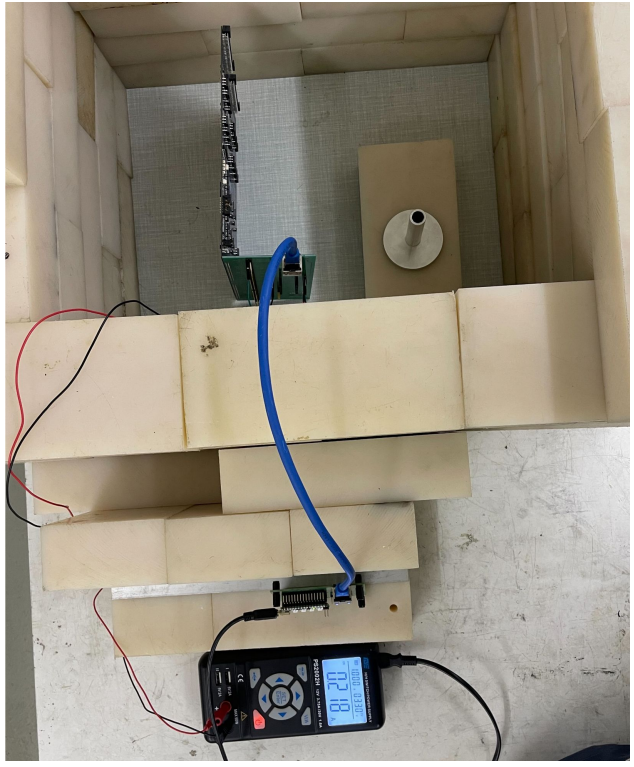
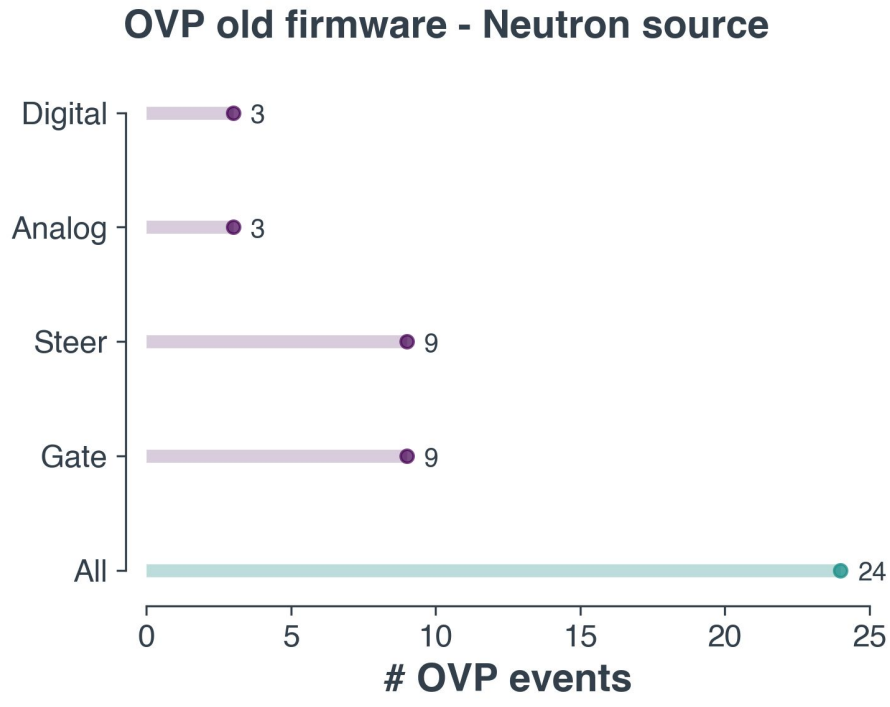
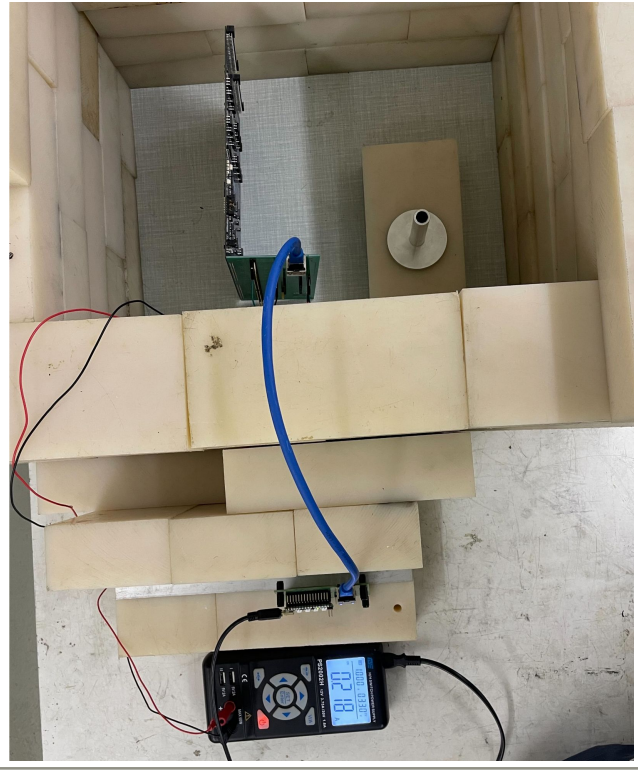
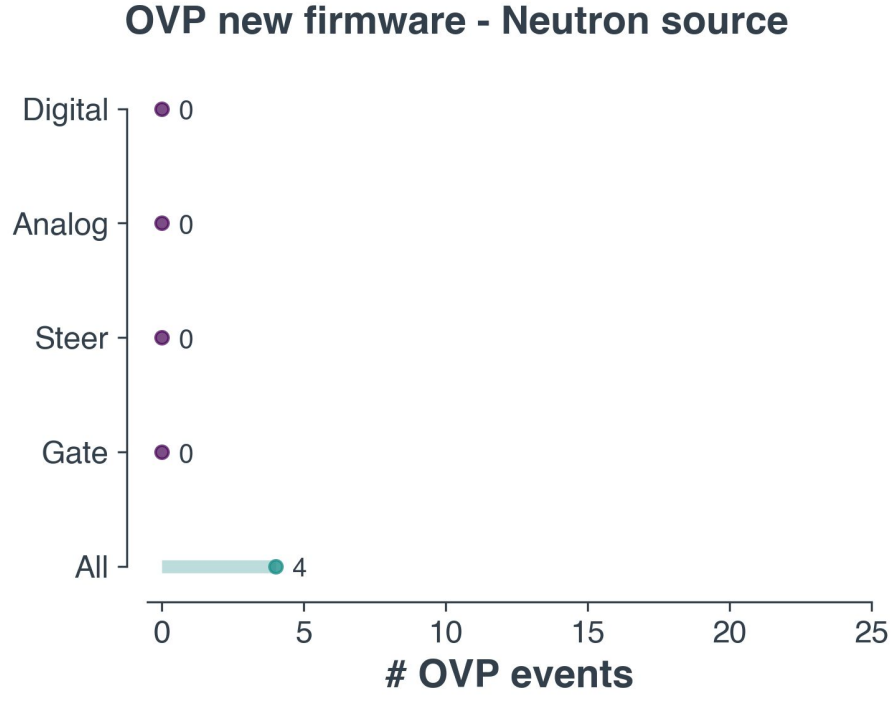




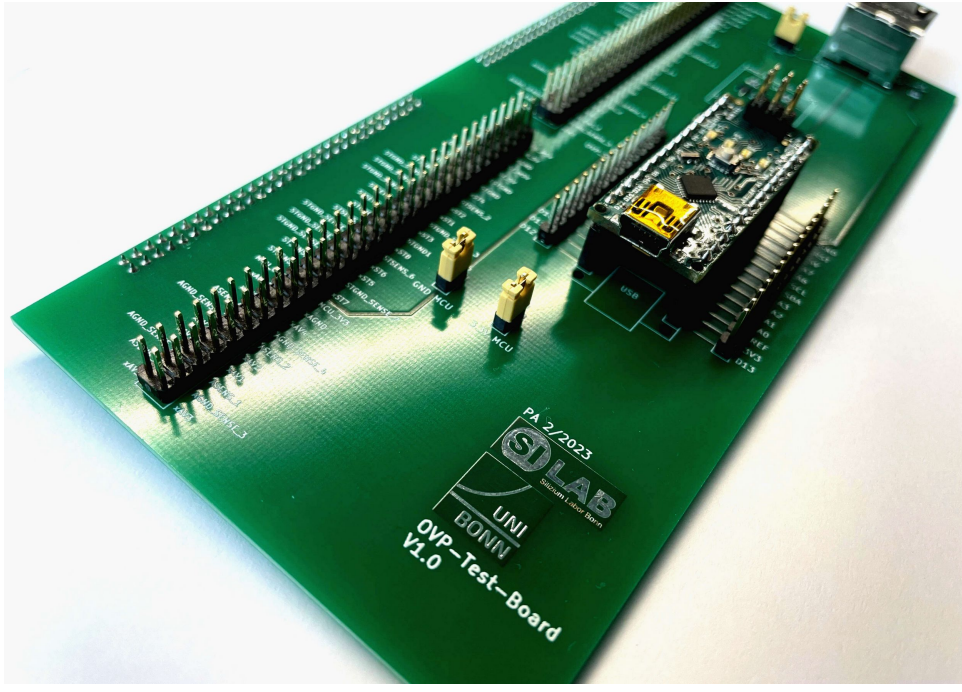
VERIFICATION – NEUTRON SOURCE





Note: Information about which channel triggered only implemented after this test

CONCLUSION



- Simulation and measurements show desired reduction of SEU triggered OVP events

  → Reduction by factor of 6

- Tests of the OVP board installed in the PXD-PS show the functionality of the new firmware

- Flashed new OVP firmware to all (but one) PSs at KEK

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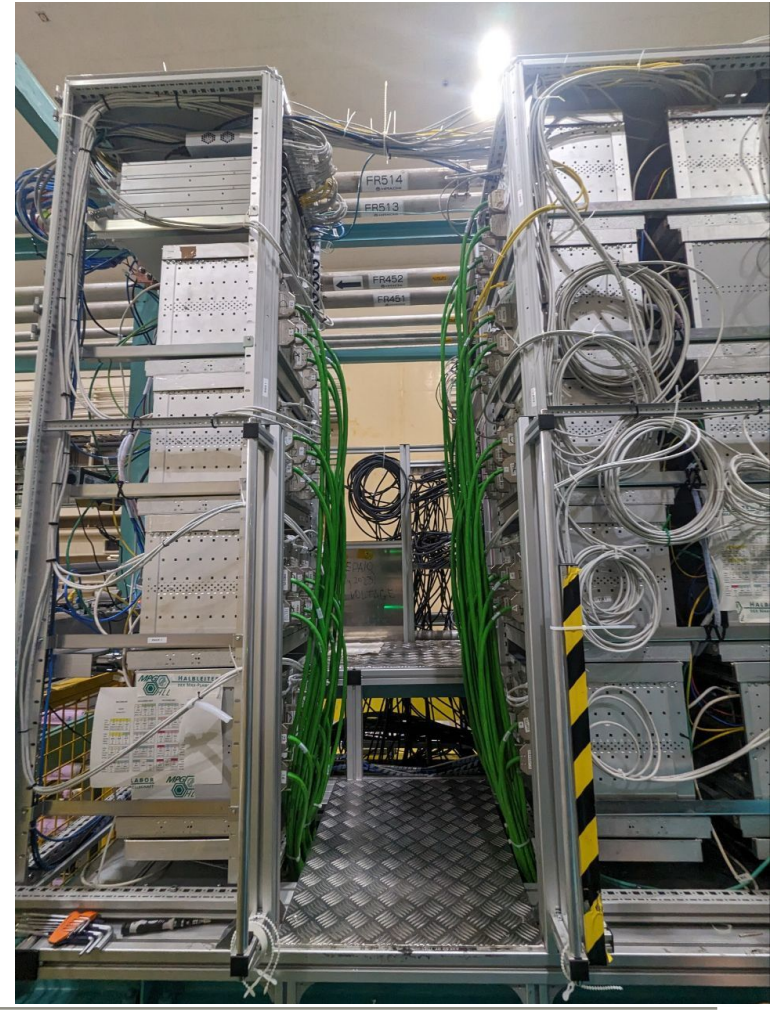
GENERAL PS WORK

- Agreed on requirements for PXD2 PSs
  - MCU modification (Removal of delay elements for shutdown)
  - 28mA HV current limit
  - DCD-AVDD regulator fix
  - Fresh calibration
  - Updated firmware
- Bonn Electronics-Workshop modified 25 PSs accordingly
- Several repairs on OVP boards + PS PCBs done
- Performed recalibration + developed testing routines

  → Now have 40 (+10 spare) working PS units at KEK



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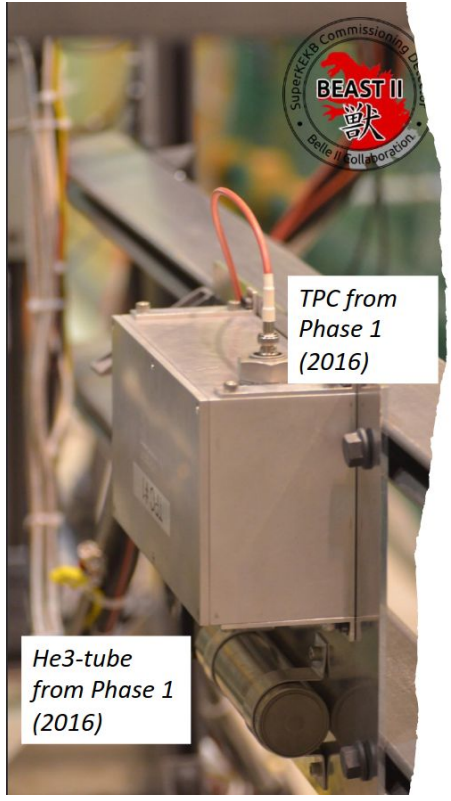
OUTLOOK



- Beam background group installed neutron detectors around PXD PS racks (Andrii Natochii 45th B2GM)
- He-3 tubes – thermal neutrons
- Time-Projection Chambers (TPCs) – fast neutrons

→ Study spectrum and direction of neutrons regarding origin and possible shielding

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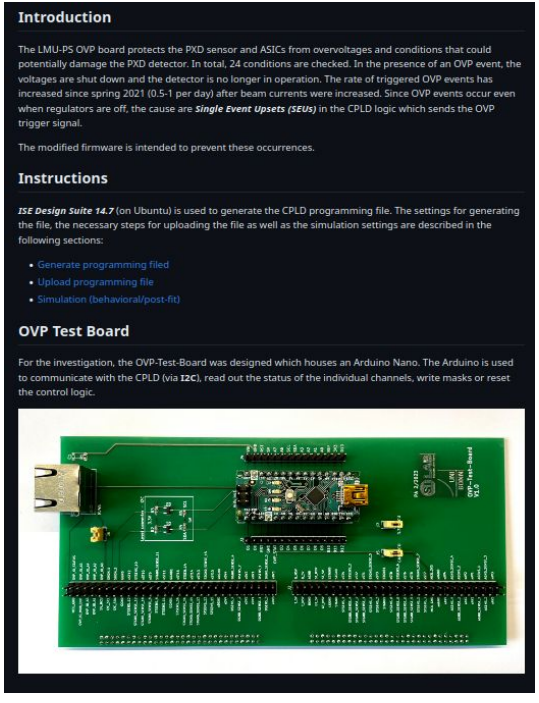
BACKUP

DOCUMENTATION

- Documentation and files on: https://github.com/SiLab-Bonn/PXD-OVP



Introduction

The LMU-PS OVP board protects the PXD sensor and ASICs from overvoltages and conditions that could potentially damage the PXD detector. In total, 24 conditions are checked. In the presence of an OVP event, the voltages are shut down and the detector is no longer in operation. The rate of triggered OVP events has increased since spring 2021 (0.5-1 per day) after beam currents were increased. Since OVP events occur even when regulators are off, the cause are ***Single Event Upsets (SEUs)*** in the CPLD logic which sends the OVP trigger signal.

The modified firmware is intended to prevent these occurrences.

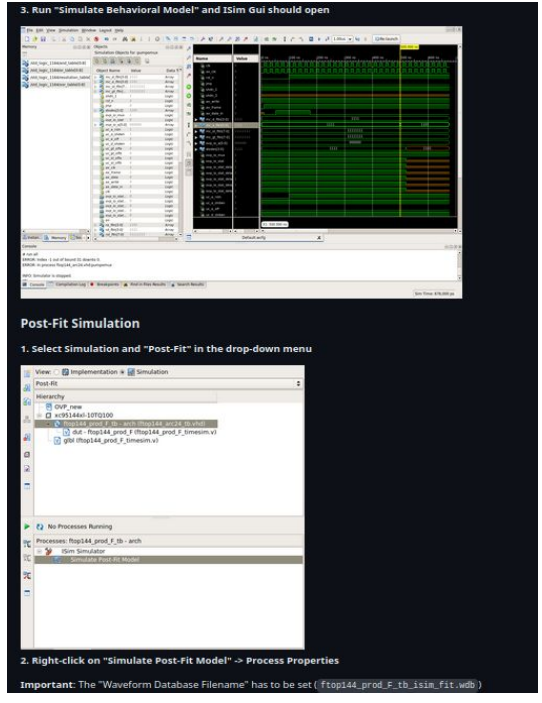
Instructions

ISE Design Suite 14.7 (on Ubuntu) is used to generate the CPLD programming file. The settings for generating the file, the necessary steps for uploading the file as well as the simulation settings are described in the following sections:

- Generate programming filed
- Upload programming file
- Simulation (behavioral/post-fit)

OVP Test Board

For the investigation, the OVP-Test-Board was designed which houses an Arduino Nano. The Arduino is used to communicate with the CPLD (via **I2C**), read out the status of the individual channels, write masks or reset the control logic.



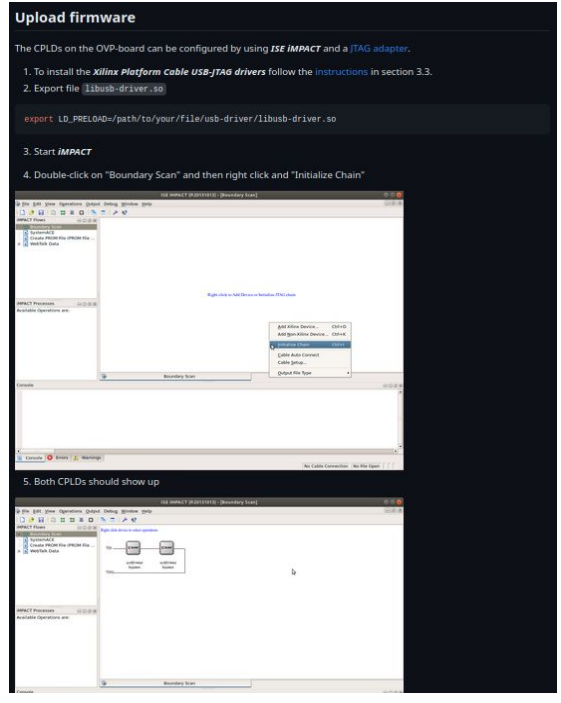
3. Run "Simulate Behavioral Model" and ISim Gui should open

Post-Fit Simulation

1. Select Simulation and "Post-Fit" in the drop-down menu

2. Right-click on "Simulate Post-Fit Model" -> Process Properties

Important: The "Waveform Database Filename" has to be set (`ftop144_prod_F_tb_isim_fit.wdb`)



Upload firmware

The CPLDs on the OVP-board can be configured by using ***ISE iMPACT*** and a JTAG adapter.

1. To install the ***Xilinx Platform Cable USB-JTAG drivers*** follow the instructions in section 3.3.
2. Export file `libusb-driver.so`

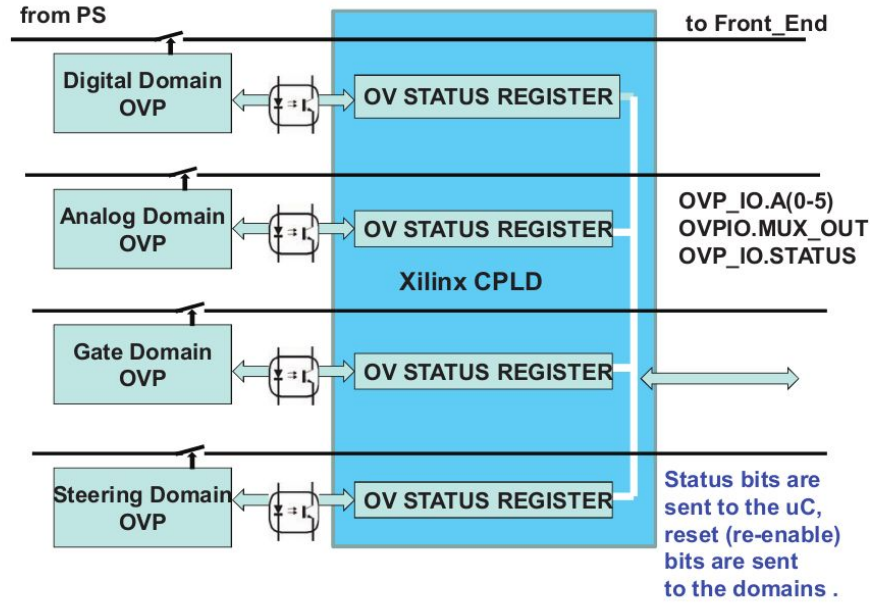
```
export LD_PRELOAD=/path/to/your/file/usb-driver/libusb-driver.so
```

3. Start ***iMPACT***
4. Double-click on "Boundary Scan" and then right click and "Initialize Chain"

5. Both CPLDs should show up

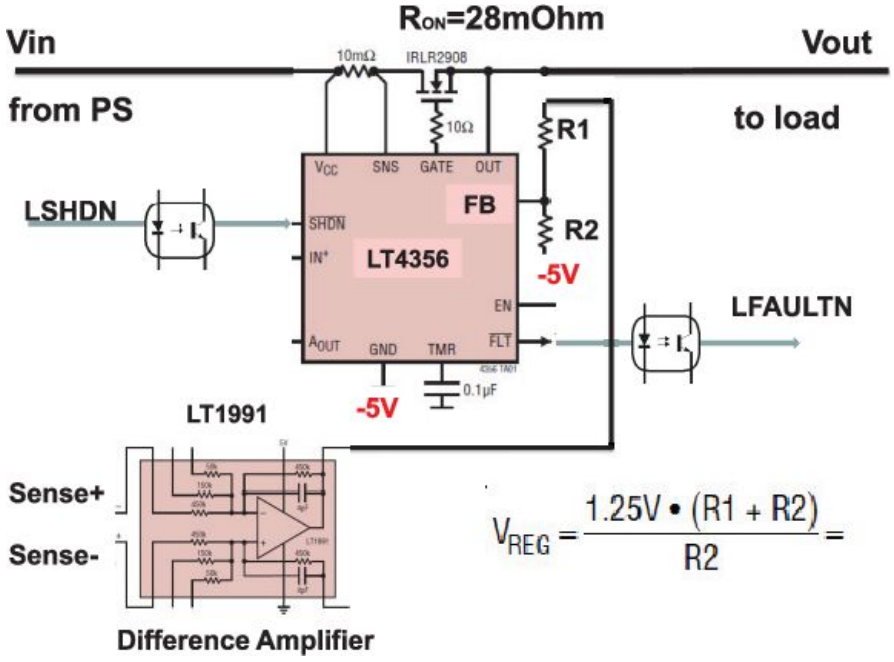
OVER VOLTAGE PROTECTION (OVP)

- Voltages are grouped in 4 domains: **Analog, Digital, Steering** and **Gate**
- Four independent grounds
- Each supply channel is equipped with the protecting circuitry
- Central logic unit (***Xilinx CPLD***) is connected to all protecting circuits (optocouplers)
- Collects status bits from every channel



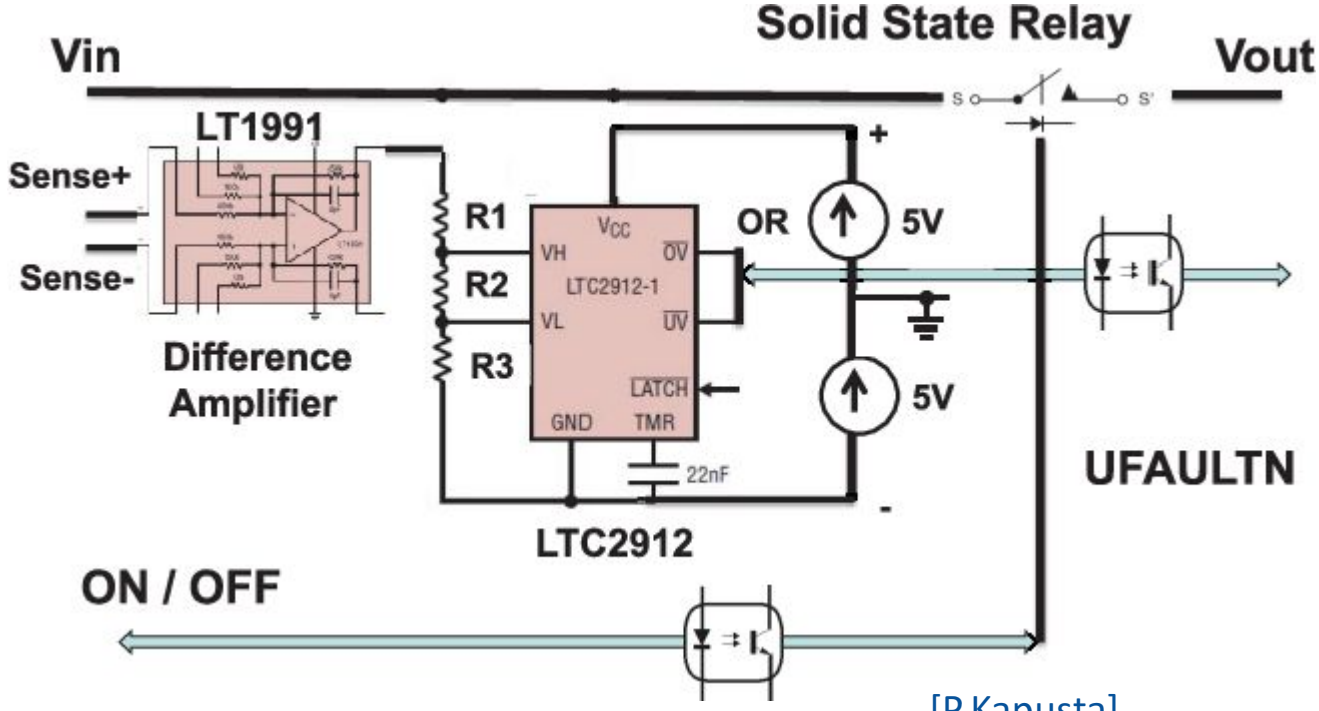
[P.Kapusta]

ANALOG/DIGITAL OVP DOMAINS



[P.Kapusta]

GATE/STEER OVP DOMAINS



[P.Kapusta]

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OVER VOLTAGE CHECKS

CH	NET (...)	CHECKED	CHECK DESCRIPTION	REL	LIMIT_L	LIMIT_H	HARDWARE
DV1	DHP_IO	itself	DHP_IO	<		2.3	LT4356
DV2	SW_DVDD	itself	SW_DVDD	<		2.3	LT4356
DV3	DHP_CORE	itself	DHP_CORE	<		1.7	LT4356
DV4	DCD_DVDD	itself	DCD_DVDD	<		2.3	LT4356
AV1	REF_IN	itself	REF_IN	<		1.6	LT4356
AV2	VSOURCE	itself	VSOURCE	<		7.5	LT4356
AV3	AMP_LOW	itself	AMP_LOW	<		2	LTC2912
AV4	DCD_AVDD	itself	DCD_AVDD	<		2.3	LT4356
ST1	Clear_ON	itself	Clear_ON	<		26	LTC2912
ST2	SW_RefIn	ST2,ST4	SW_Refin-SW_SUB	<		2.3	LTC2912
ST3	Clear_OFF	itself	Clear_OFF	<,<	-1	6	LTC2912
ST4	SW_SUB	ST9,ST4	Gate_ON_1-SW_SUB	>	-0.6		LTC2912
ST5	free	ST11,ST4	Gate_ON_3-SW_SUB	>	-0.6		LTC2912
ST6	HV	ST10,ST4	Gate_ON_2-SW_SUB	>	-0.6		LTC2912
ST7	VBulk	itself	Vbulk	<		17.5	LTC2912
ST8	VGuard	itself	Vguard	<,<	-9	1	LTC2912
ST9	Gate_ON_1	itself	Gate_ON_1	>	-14		LTC2912
ST10	Gate_ON_2	itself	Gate_ON_2	>	-14		LTC2912
ST11	Gate_ON_3	itself	Gate_ON_3	>	-14		LTC2912
ST12	Gate_OFF	itself	Gate_OFF	<.<	-4.5	6	LTC2912
ST13	CCG1	itself	CCG1	<,<	-12	2.3	LTC2912
ST14	CCG2	itself	CCG2	<,<	-12	2.3	LTC2912
ST15	CCG3	itself	CCG3	<,<	-12	2.3	LTC2912
ST16	VDrift	itself	Vdrift	>	-14.3		LTC2912