UNIVERSITÄT BONN

FTD

SI LAB
Silizium Labor Bonn

TEST STRUCTURE IRRADIATION

FSP MEETING
26.09.2023

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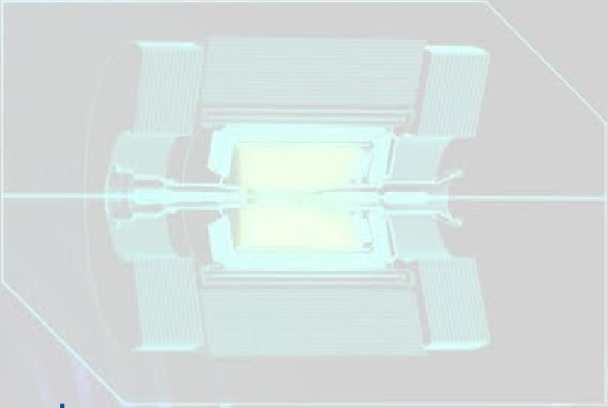
JENNIFER2
EU grant n.822070

bmb+f - Förderschwerpunkt
Elementarteilchenphysik
Großgeräte der physikalischen Grundlagenforschung

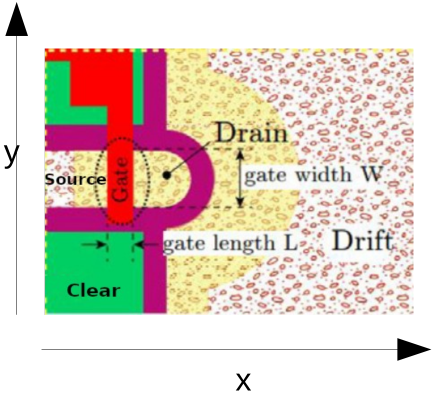
OVERVIEW

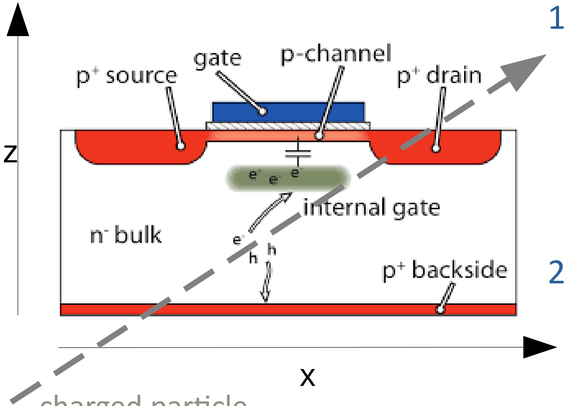


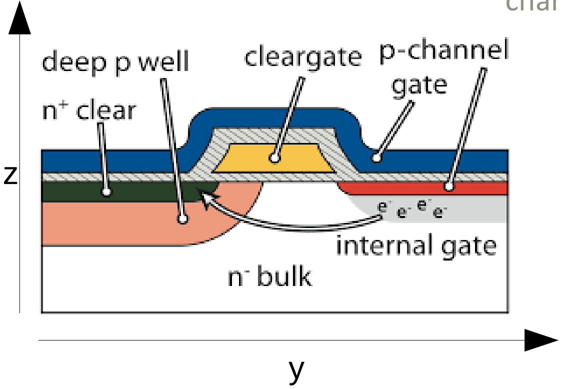
- Introduction
  - DePFET
  - High DePFET-backside currents
  - Mechanism
- Test structures
- X-ray irradiation setup
- Results
- Summary

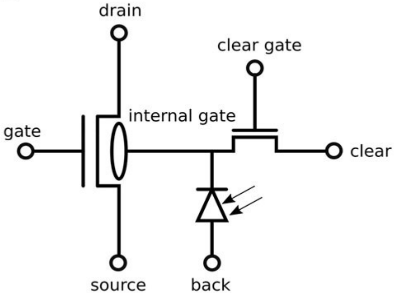
THE DEPFET STRUCTURE AND WORKING PRINCIPLE

Depleted P-channel Field Effect Transistor (DePFET)







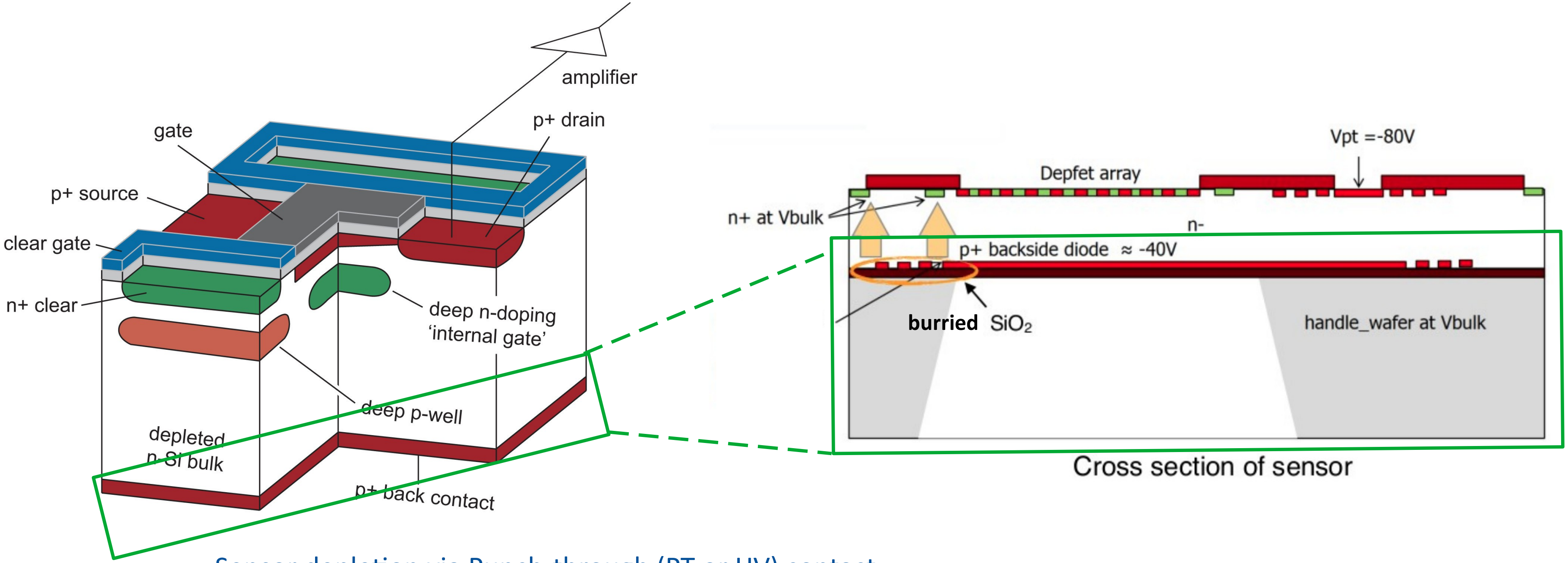


1. p-channel MOSFET operated in saturation
   - $V_{GS} > V_{th}$ and $V_{DS} \geq V_{GS} - V_{th}$
   - V_{GS} modulates I_{DS}

V_{GS}: gate voltage
V_{th}: threshold voltage
V_{DS}: drain-source voltage
I_{DS}: drain current

2. Internal gate
   - Fast charge collection (*O*(ns))
   - Additional I_{DS} modulation → Signal
   -
3. Additional FET for clear mechanism
   - Directly connected to internal gate
   - Large positive voltage applied to clear → empties internal gate

DEPFET BACKSIDE



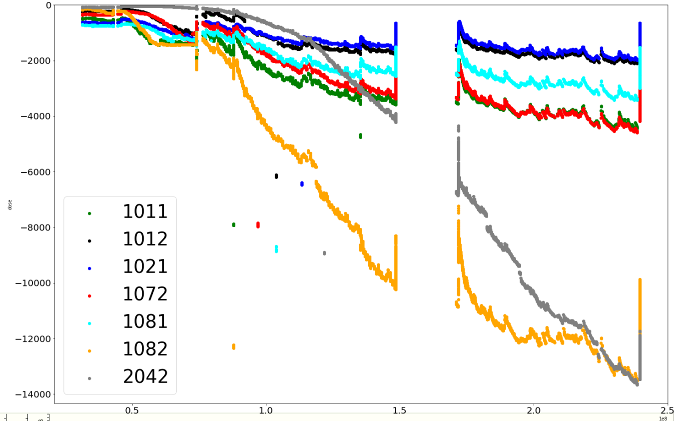
Cross section of sensor

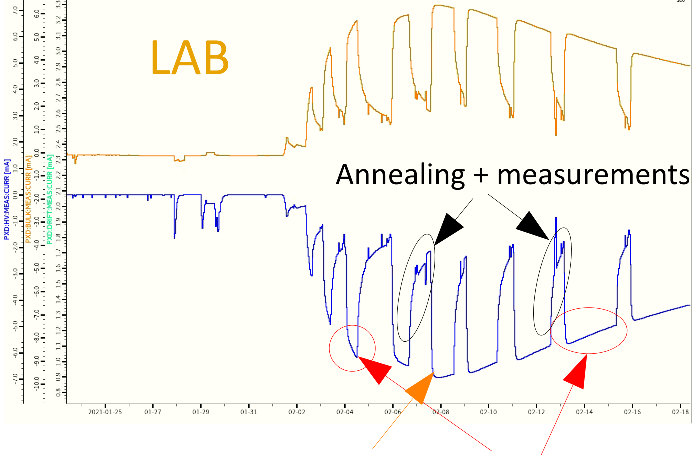
- Sensor depletion via Punch-through (PT or HV) contact
- Guard-ring structure surrounding the backside implant
- Guard-ring structure floating to ensure smooth electric field reduction towards the edge of the sensor
- IceMOS or Shin-Etsu bonded wafer

HIGH HV CURRENTS

- High HV currents observed in modules at KEK since spring 2020
- Verified by X-ray irradiation campaigns in the lab with full-scale and prototype modules
  - Saturation expected at **~ 1.5 Mrad** (burried SiO_2 TID) from lab measurements
  - **IceMOS → saturation @ ~7 mA**
  - HV current in IceMOS is **~10x higher** than Shin-Etsu
- As of now, dose of modules at KEK **up to 0.6 Mrad TID** , but currents go (far) beyond 7 mA
- Mechanism?

KEK

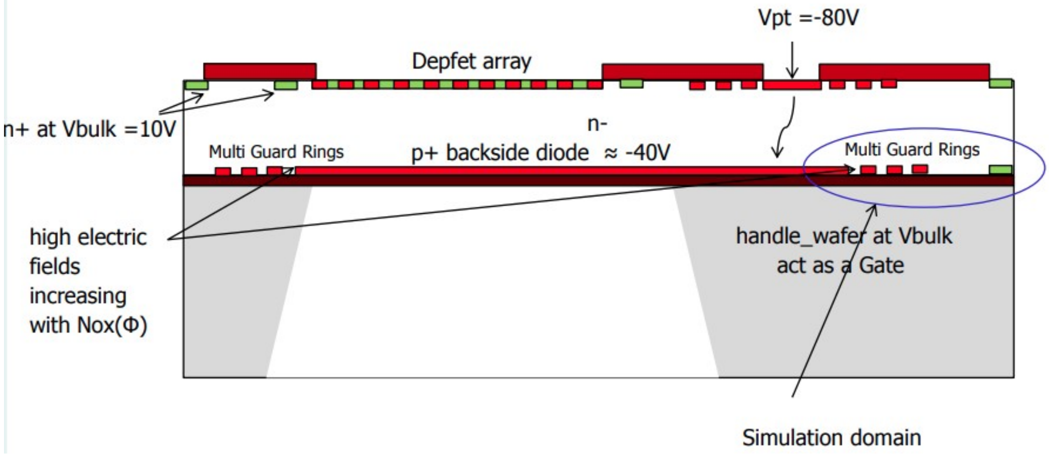


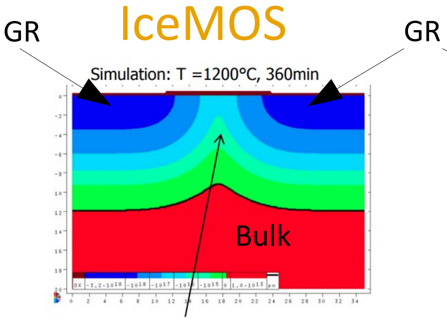


Saturation ~7 mA

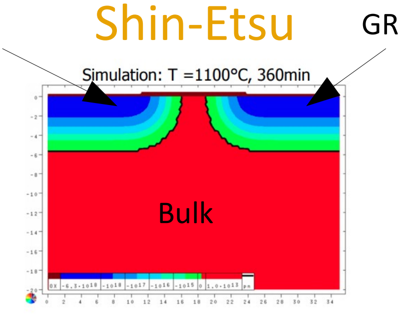
irradiation

HIGH HV CURRENT MECHANISM





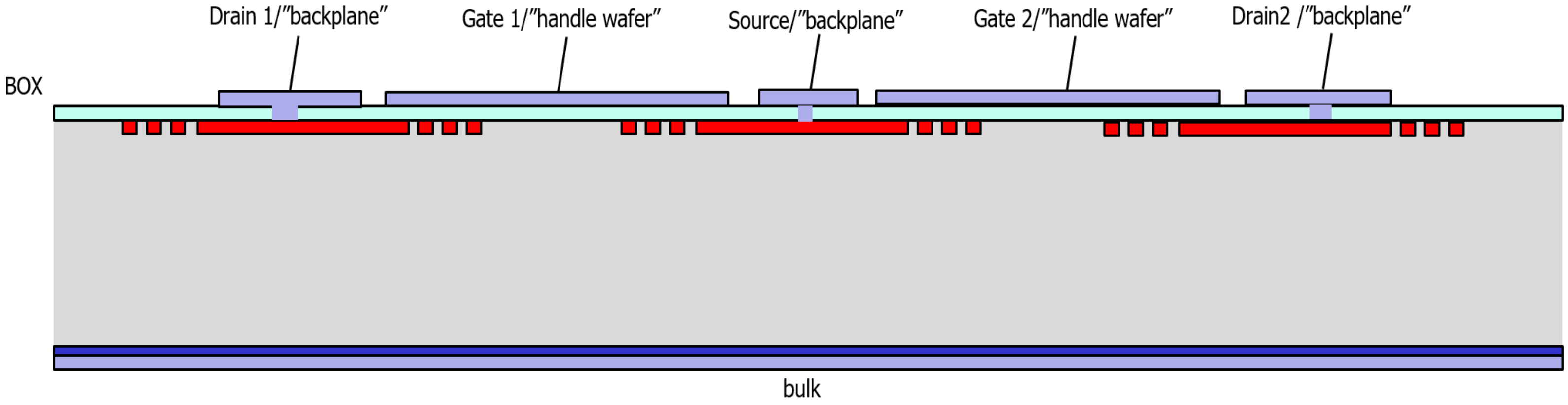
No n-doping, no space charge, no pot. barrier



some n-doping, some charge, weak pot. barrier

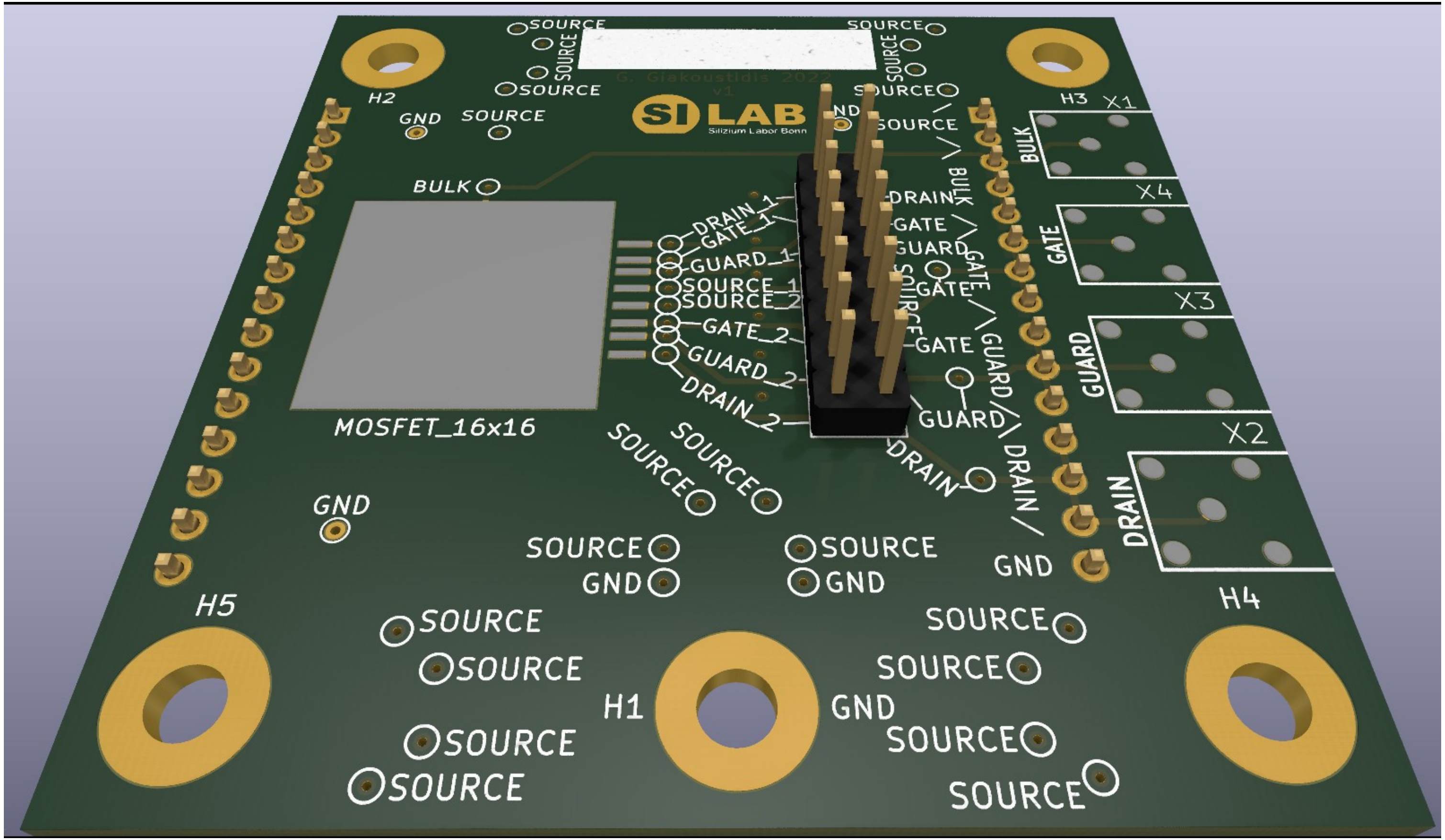
- *Secondary Ion Mass Spectroscopy (SIMS) + Simulation:* Extract dopant profile
- *Shorted guard rings*
  - The effect is worse in IceMOS than Shin-Etsu bonded wafers
- *Current understanding*: High electric fields at guard-ring structures → avalanche current multiplication → increased currents
- Structure to verify the mechanism?

MOSFET TEST STRUCTURES



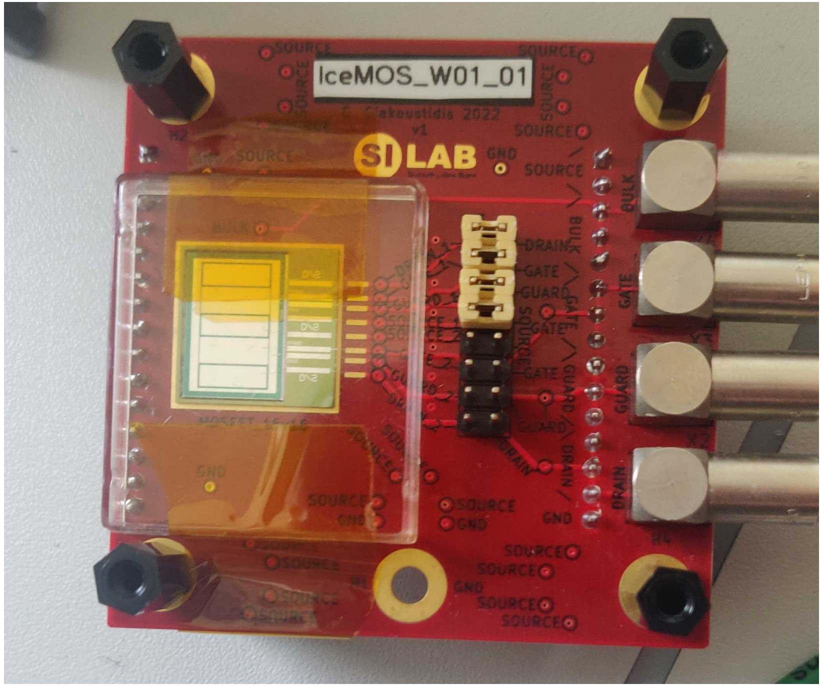
- Processing similar to DePFET
- Use p+ backside implantation of matrices as source and drain to create MOSFETs
- Less complicated than DePFET → easier to verify the mechanism
- Interface?

PCB FRONT SIDE



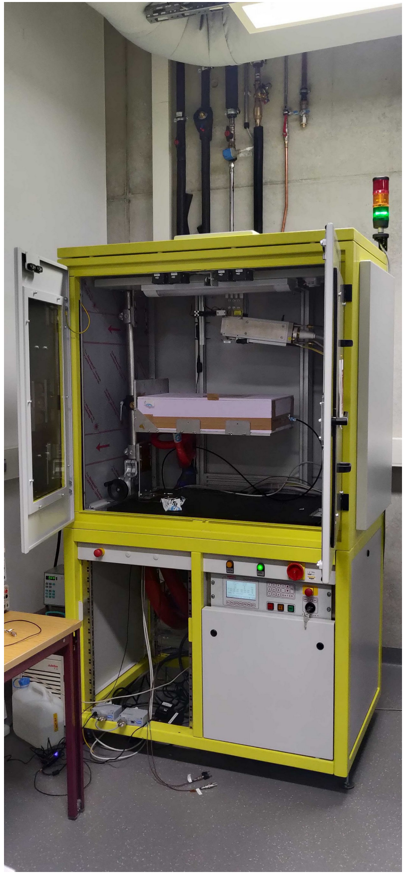
PCB IN ACTION

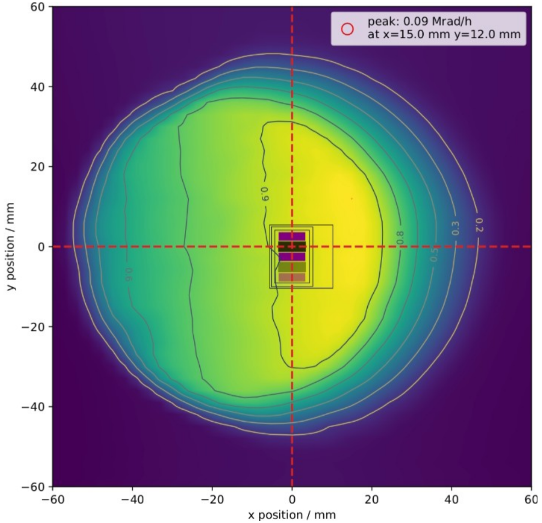
- 8 MOSFET test structures glued and wire-bonded on PCBs
  - 4 **IceMOS** bonded SOI
  - 4 **Shin-Etsu** bonded SOI
- Electrical tests and inspection done
  - 7 working
  - 1 non-working (not good bulk contact, not enough glue)
- Fully characterized and X-ray irradiated
  - 1 **IceMOS** bonded SOI
  - 1 **Shin-Etsu** bonded SOI

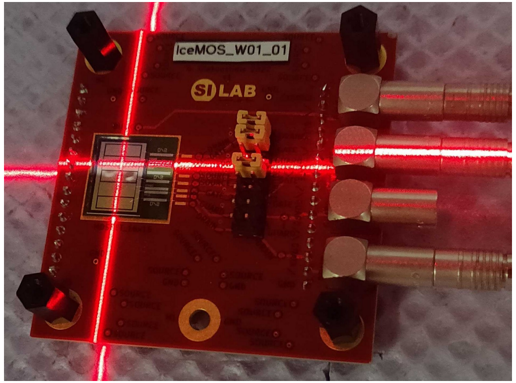


X-RAY CHAMBER AND BEAM PROFILE

- X-ray setup in Bonn
- Tungsten target
- 150 µm Al filter
- V_{tube} = 40 kV
- I_{anode} = 40-50 mA
- X-ray beam profile gradient → anode heel effect
- Quite some effort to make the irradiation campaign 100% remote
  - 3-week long

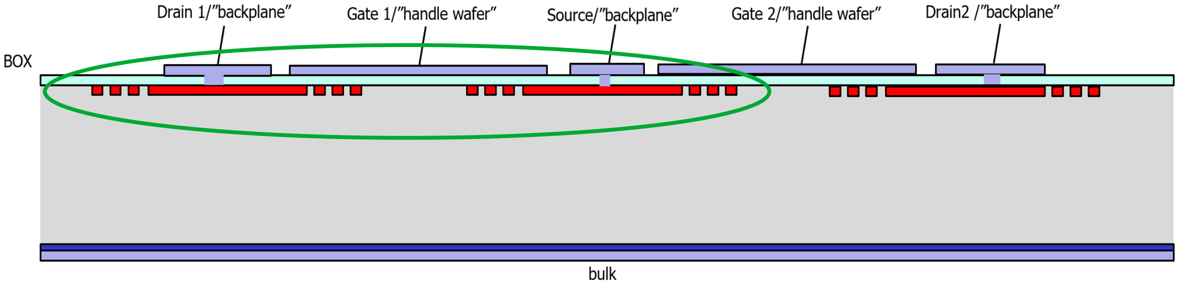






MEASUREMENT GOALS

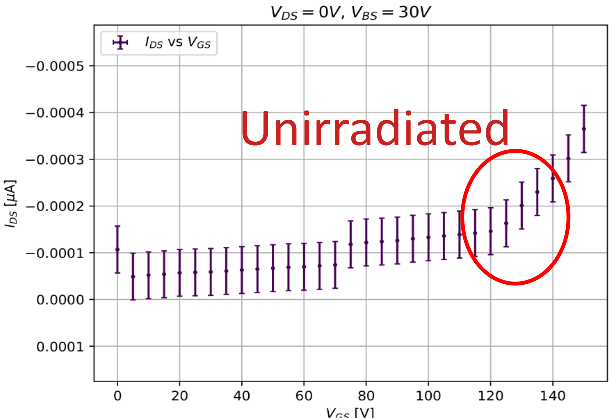
- *Irradiation up to ~10 Mrad & same dose rate:*
  - Burried SiO_2 dose in full-scale and prototype modules from previous campaigns

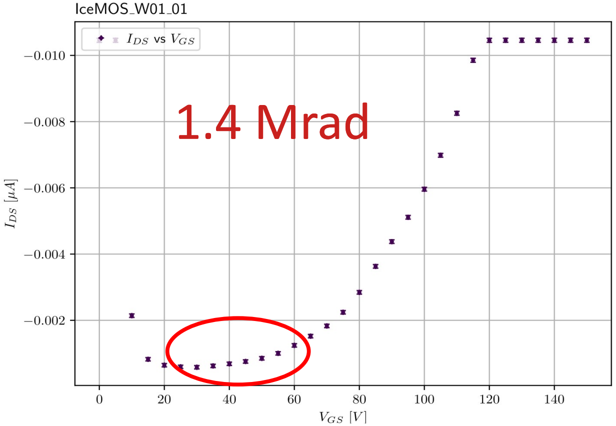


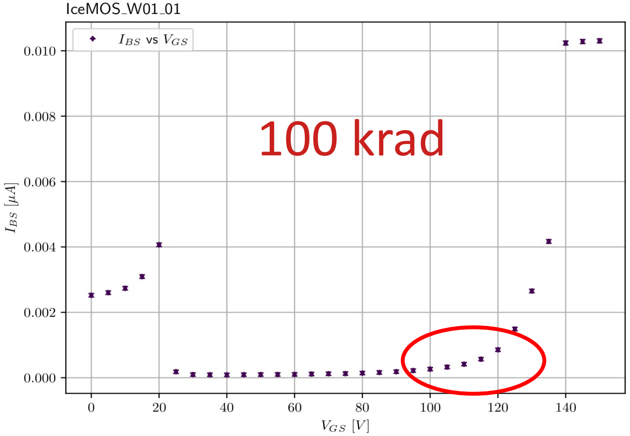
- *Biasing:*
  - **Zero-biasing** → comparison to literature
  - **DePFET-like biasing** → comparison to previous irradiation campaigns with DePFET
- *Main measurements:*
  - Create avalanche currents by scanning over highly positive V_{GS}
    - Verify that onset starts earlier with higher radiation levels
  - Measure threshold voltage
    - Calculate oxide charge density
- *Secondary measurements:*
  - Study other MOSFET characteristics (e.g. sub-threshold swing)

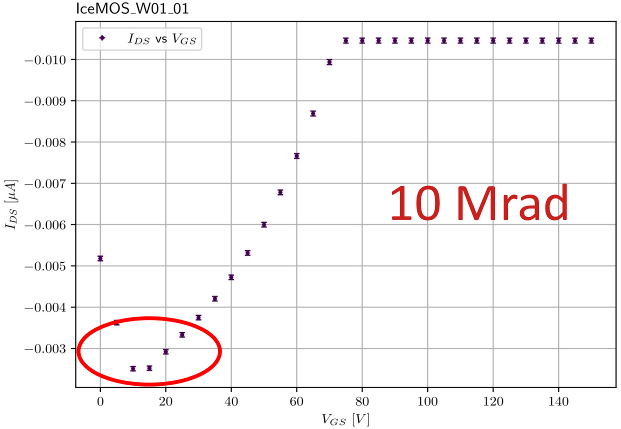
AVALANCHE CURRENT MEASUREMENT (I_avalanche) ICEMOS

- V_{DS} = 0 V, V_{BS} = 30 V
- Onset indeed **shifts to lower voltages** with irradiation
- From onset the oxide charge can be calculated

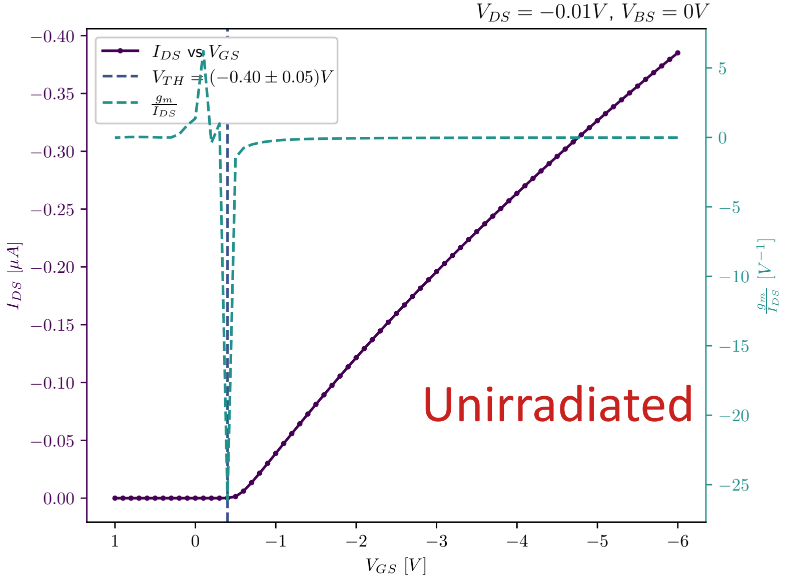

Unirradiated

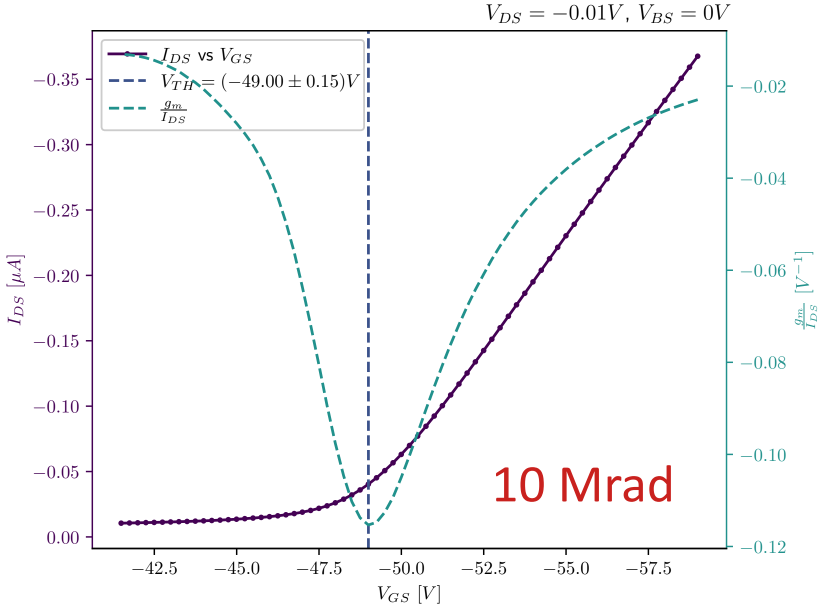

1.4 Mrad


100 krad


10 Mrad

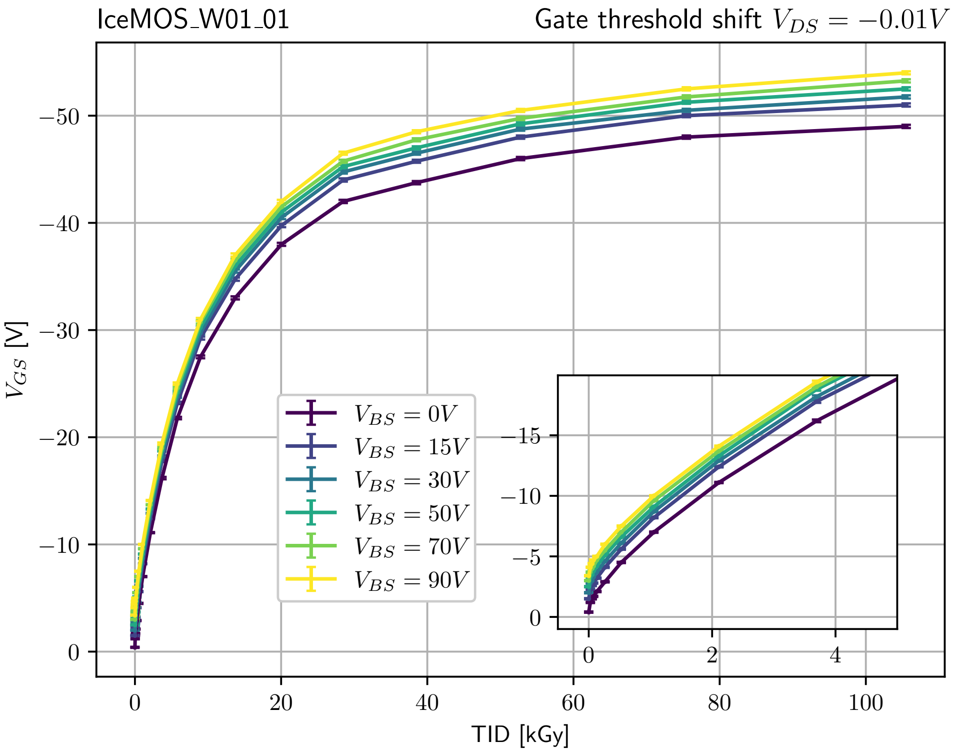
GATE THRESHOLD VOLTAGE MEASUREMENT (I_{DS} vs V_{GS} (thr)) ICEMOS

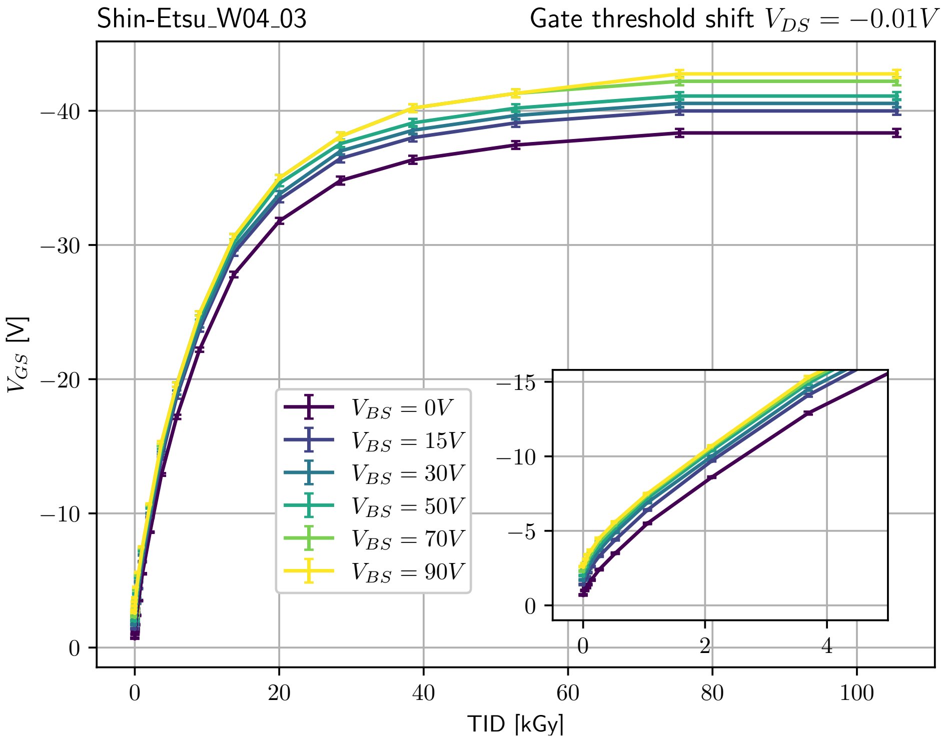




- Use minimum of g_m/I_{DS} to determine the threshold
- Noise can affect the measurement (especially the baseline)

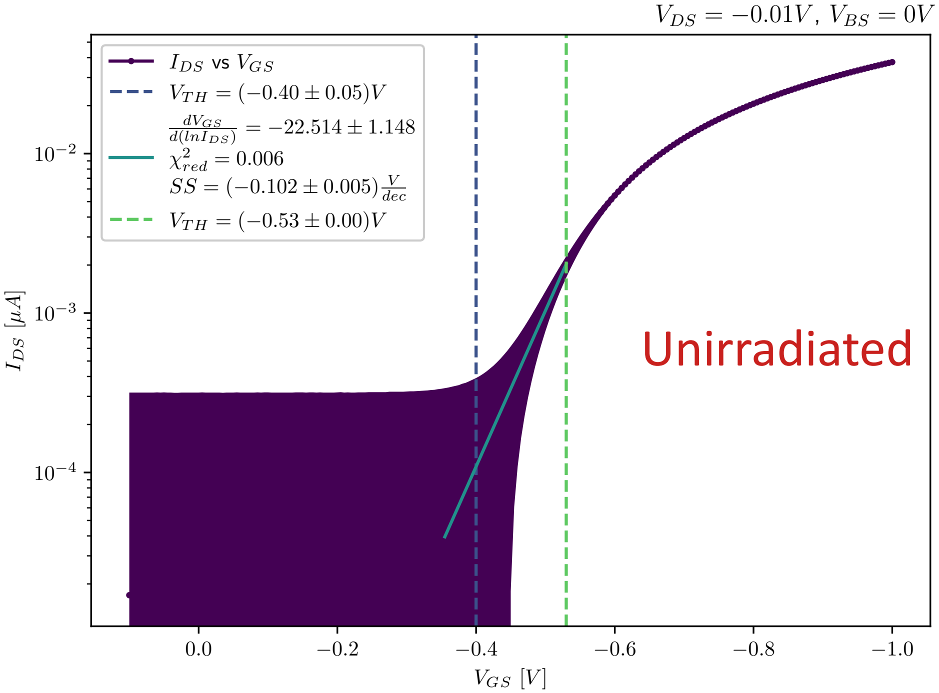
GATE THRESHOLD VOLTAGE MEASUREMENT (I_{DS} vs V_{GS} (thr)) SHIFT

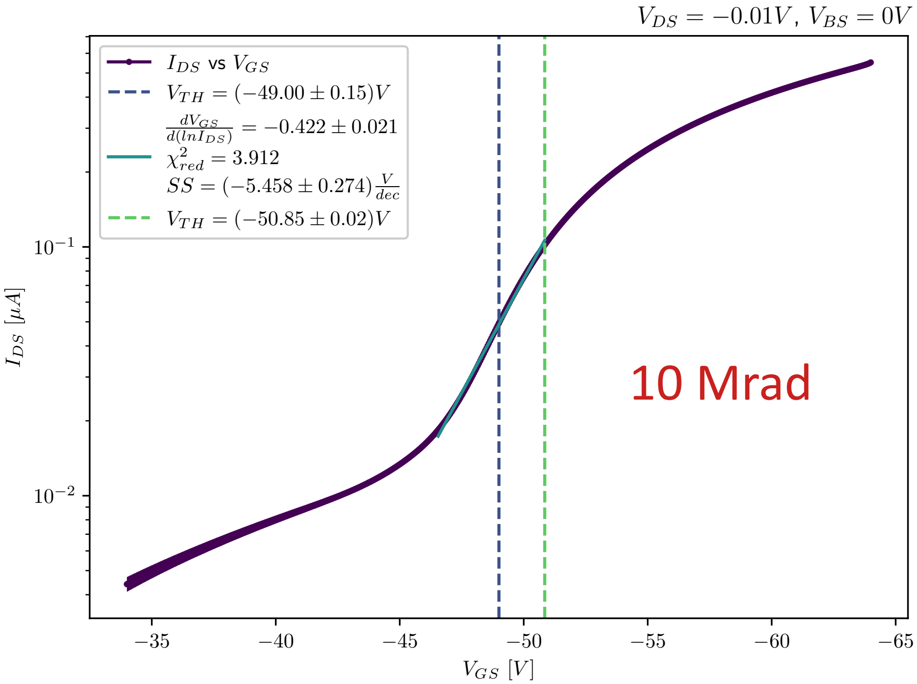




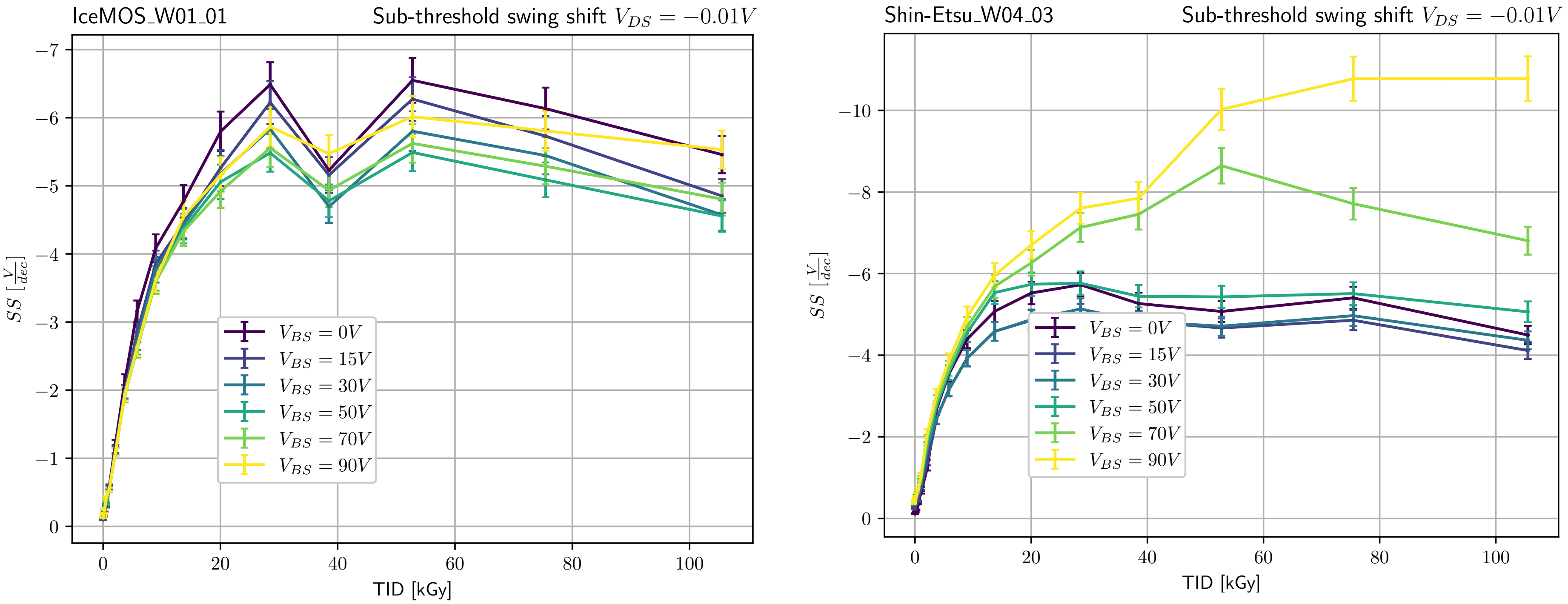
- **Higher** gate threshold shift for **IceMOS** (thicker oxide)

GATE SUB-THRESHOLD SWING MEASUREMENT (I_{DS} vs V_{GS} (sub)) ICEMOS

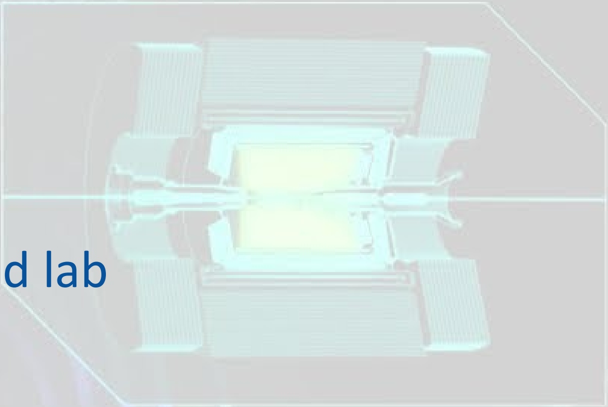




GATE SUB-THRESHOLD SWING MEASUREMENT (I_{DS} vs V_{GS} (sub)) SHIFT



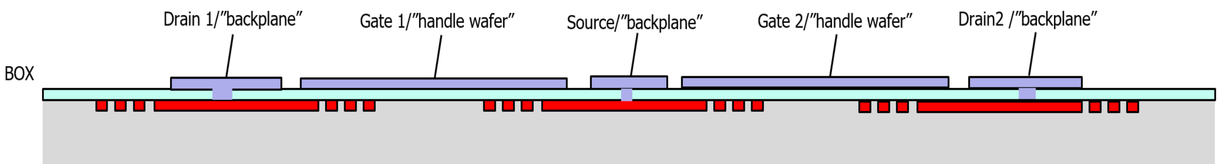
SUMMARY

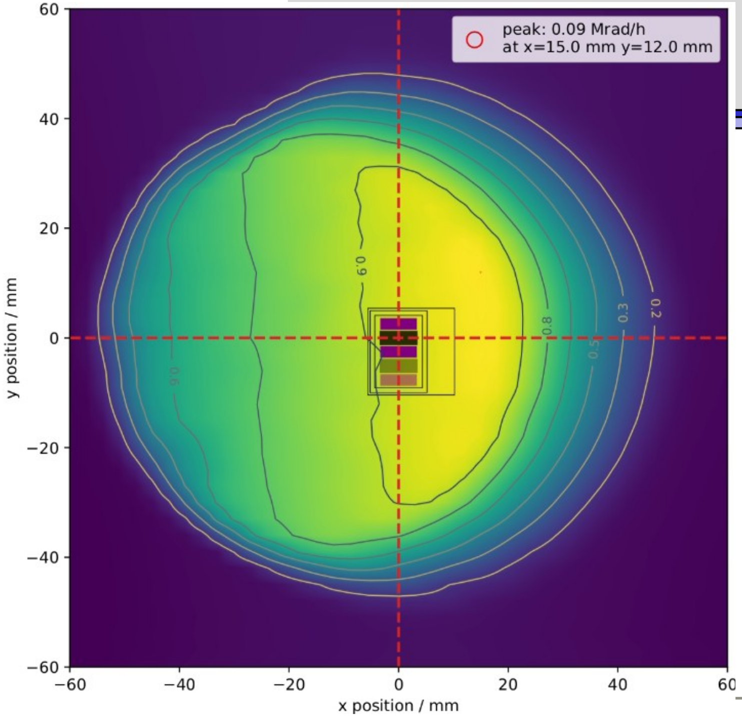


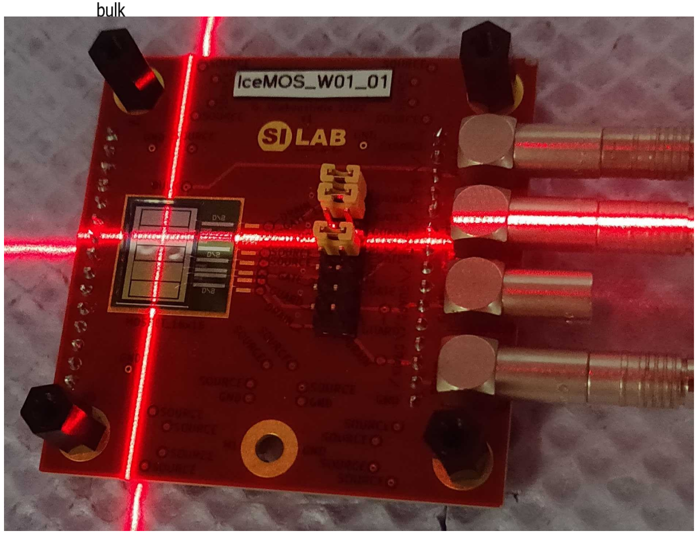
- Observed discrepancies between modules at KEK and lab
  - Under investigation
- High backside current mechanism is understood
  - (Partially) shorted guard-rings at the backside
  - Avalanche current multiplication
- Investigation with irradiation of test structures
  - Further analysis and interpretation is needed

BACKUP

TEST-STRUCTURES FOR HV CURRENT INVESTIGATION

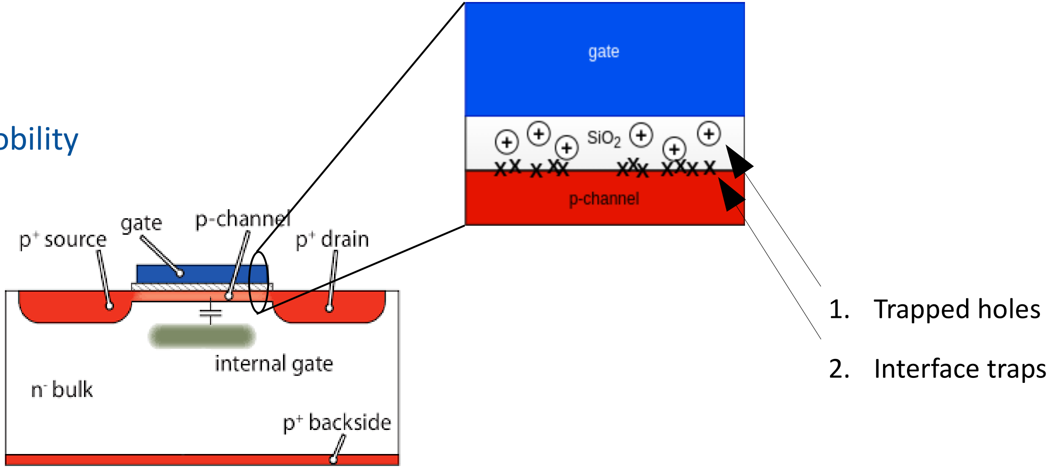




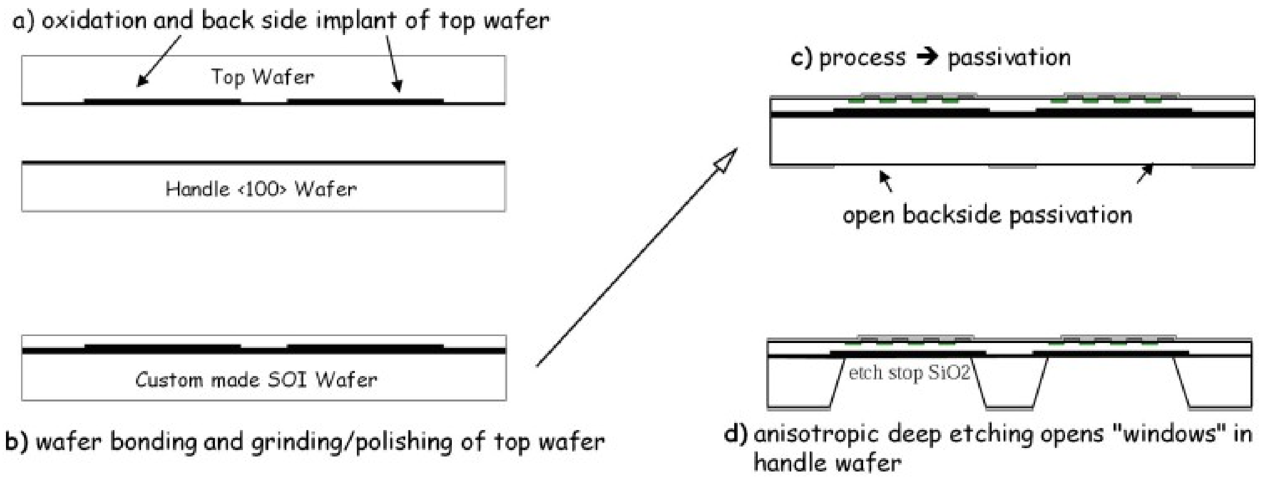


SURFACE RADIATION DAMAGE IN DEPFET

- X-ray irradiation → e-h pairs → Oxide damage
  1. Trapped holes at SiO_2 / Si border due to their low mobility
  2. Interface traps
     - Moving holes in the lattice release protons
     - Protons drift towards the SiO_2 / Si interface
     - Reaction with hydrogen-passivated defects → H_2 molecules
     - H_2 molecules diffuse out and charge defect is left behind
- Effect on V_{th} of a FET
  - Negative threshold shift for p-channel MOSFET
  - **DEPFET gate (V_G)** and **Common Clear Gate (V_{CCG})**



DEPFET PROCESSING

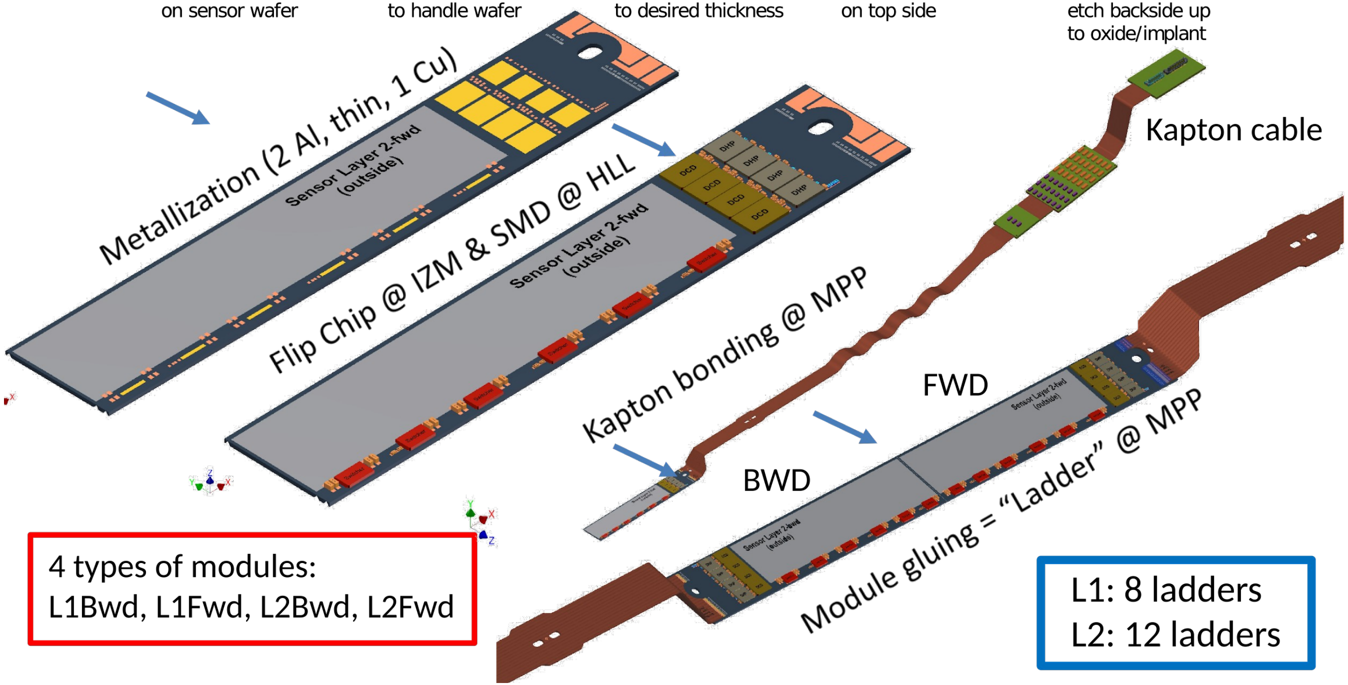


- Processing similar to DEPFET
  - Backside implantation of the Top Wafer
  - Oxidization of the Top and Handle Wafer
  - SOI bonding of the two Wafers (Shin-Etsu and IceMOS)
  - Passivation
  - Unstractured n-type substrate on the topside of the Top Wafer
  - Etching

DEPFET PROCESSING

DEPFET Production

1. implant backside on sensor wafer
2. bond sensor wafer to handle wafer
3. thin sensor side to desired thickness
4. process DEPFETs on top side
5. structure resist, etch backside up to oxide/implant

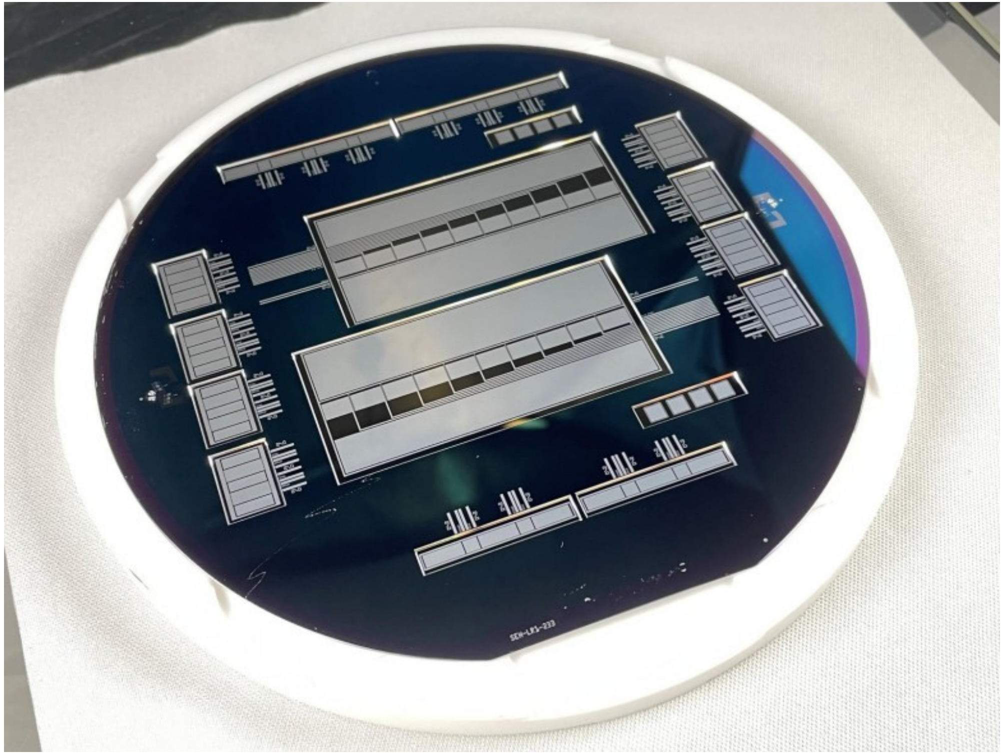


4 types of modules:
L1Bwd, L1Fwd, L2Bwd, L2Fwd

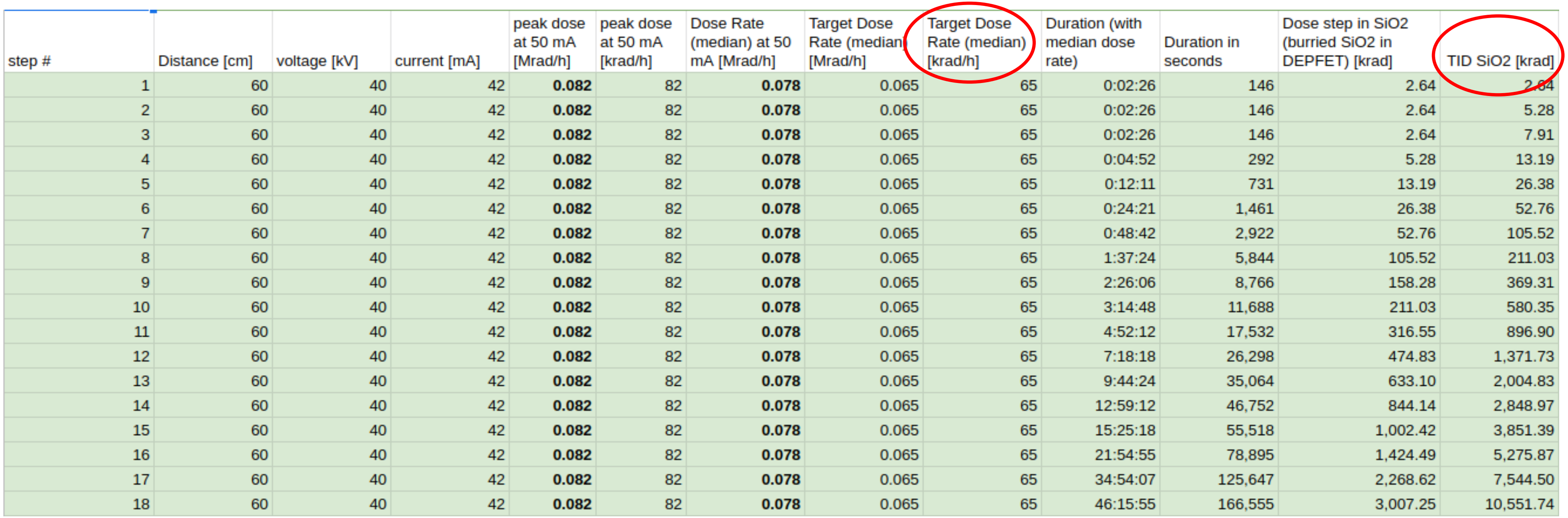
L1: 8 ladders
L2: 12 ladders

TEST STRUCTURES ON WAFER LEVEL

- Six (6) wafers in total
  - Three (3) IceMOS bonded SOI
  - Three (3) Shin-Etsu bonded SOI
- Five (5) different structures
  - Four (4) MOSFET
  - One (1) MOS CAP
- Structures have been cut, tested and sent to Bonn

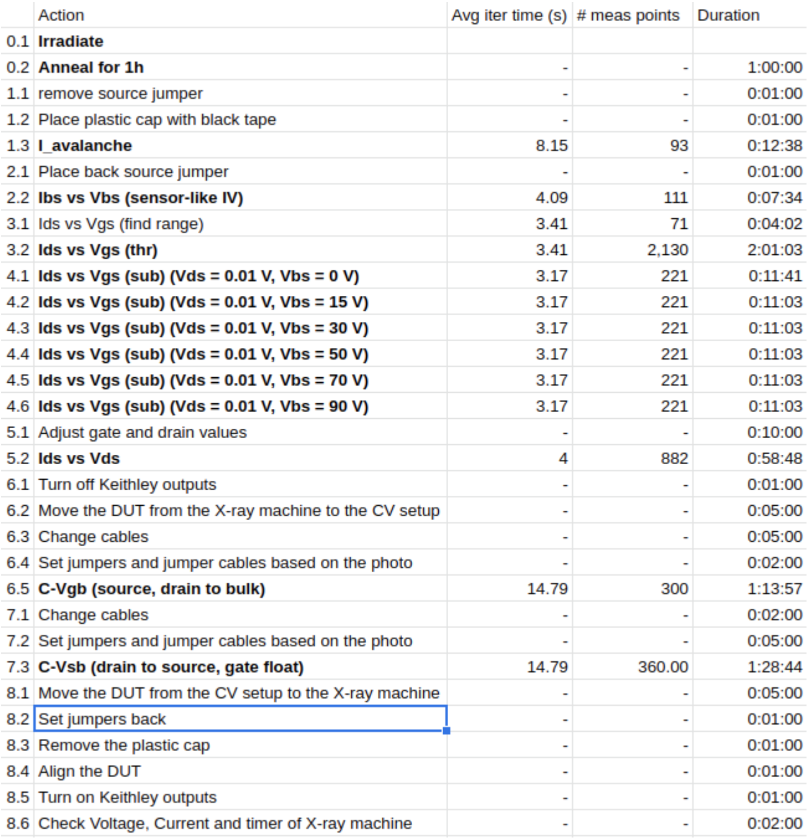


IRRADIATION PLAN

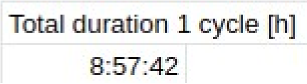


step #	Distance [cm]	voltage [kV]	current [mA]	peak dose at 50 mA [Mrad/h]	peak dose at 50 mA [krad/h]	Dose Rate (median) at 50 mA [Mrad/h]	Target Dose Rate (median) [Mrad/h]	Target Dose Rate (median) [krad/h]	Duration (with median dose rate)	Duration in seconds	Dose step in SiO2 (burried SiO2 in DEPFET) [krad]	TID SiO2 [krad]
1	60	40	42	**0.082**	82	**0.078**	0.065	65	0:02:26	146	2.64	2.64
2	60	40	42	**0.082**	82	**0.078**	0.065	65	0:02:26	146	2.64	5.28
3	60	40	42	**0.082**	82	**0.078**	0.065	65	0:02:26	146	2.64	7.91
4	60	40	42	**0.082**	82	**0.078**	0.065	65	0:04:52	292	5.28	13.19
5	60	40	42	**0.082**	82	**0.078**	0.065	65	0:12:11	731	13.19	26.38
6	60	40	42	**0.082**	82	**0.078**	0.065	65	0:24:21	1,461	26.38	52.76
7	60	40	42	**0.082**	82	**0.078**	0.065	65	0:48:42	2,922	52.76	105.52
8	60	40	42	**0.082**	82	**0.078**	0.065	65	1:37:24	5,844	105.52	211.03
9	60	40	42	**0.082**	82	**0.078**	0.065	65	2:26:06	8,766	158.28	369.31
10	60	40	42	**0.082**	82	**0.078**	0.065	65	3:14:48	11,688	211.03	580.35
11	60	40	42	**0.082**	82	**0.078**	0.065	65	4:52:12	17,532	316.55	896.90
12	60	40	42	**0.082**	82	**0.078**	0.065	65	7:18:18	26,298	474.83	1,371.73
13	60	40	42	**0.082**	82	**0.078**	0.065	65	9:44:24	35,064	633.10	2,004.83
14	60	40	42	**0.082**	82	**0.078**	0.065	65	12:59:12	46,752	844.14	2,848.97
15	60	40	42	**0.082**	82	**0.078**	0.065	65	15:25:18	55,518	1,002.42	3,851.39
16	60	40	42	**0.082**	82	**0.078**	0.065	65	21:54:55	78,895	1,424.49	5,275.87
17	60	40	42	**0.082**	82	**0.078**	0.065	65	34:54:07	125,647	2,268.62	7,544.50
18	60	40	42	**0.082**	82	**0.078**	0.065	65	46:15:55	166,555	3,007.25	10,551.74

MEASUREMENT PROTOCOL 08.2022-09.2022 IRRAD ICEMOS

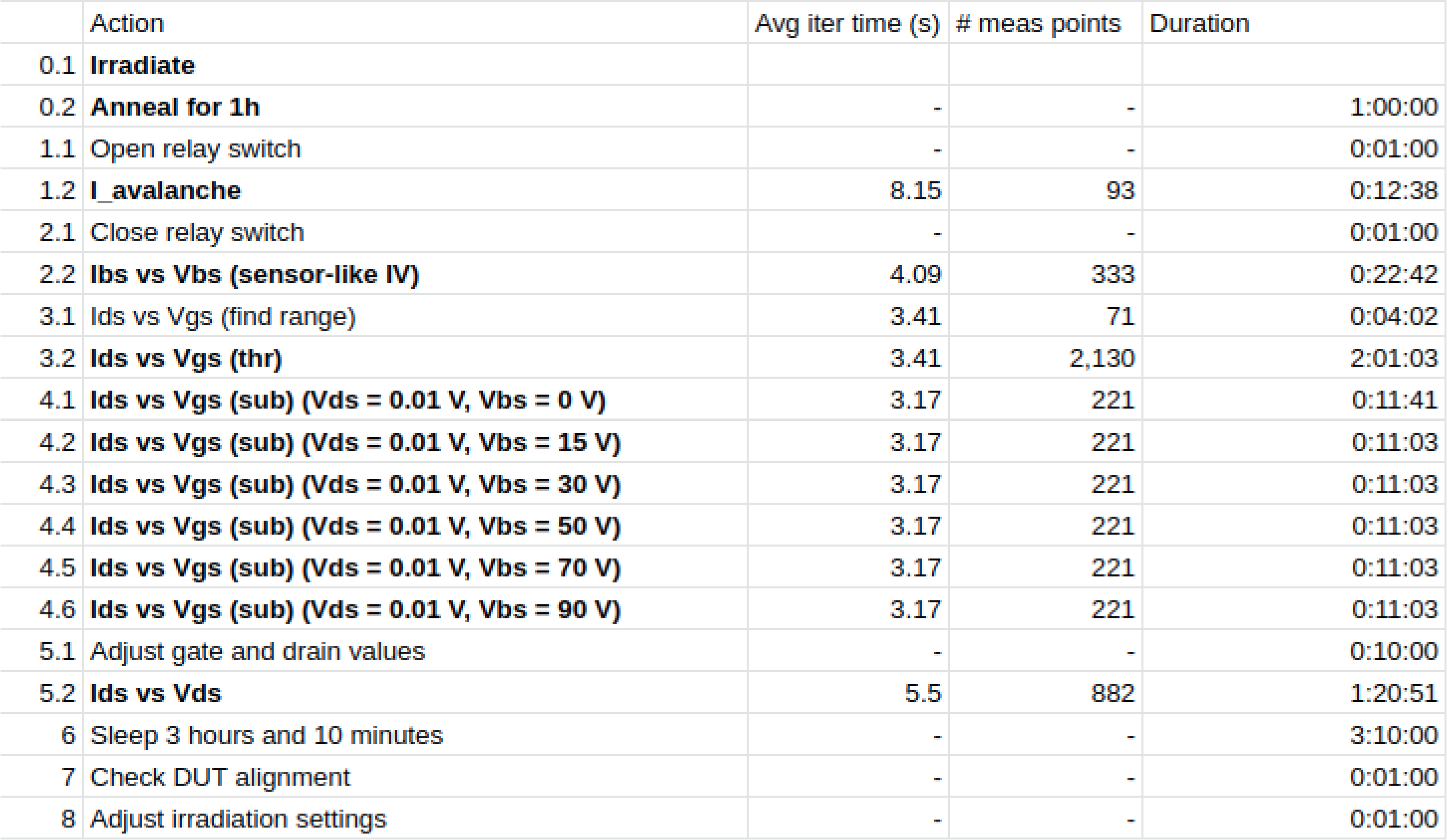


	Action	Avg iter time (s)	# meas points	Duration
0.1	**Irradiate**			
0.2	**Anneal for 1h**	-	-	1:00:00
1.1	remove source jumper	-	-	0:01:00
1.2	Place plastic cap with black tape	-	-	0:01:00
1.3	**I_avalanche**	8.15	93	0:12:38
2.1	Place back source jumper	-	-	0:01:00
2.2	**Ibs vs Vbs (sensor-like IV)**	4.09	111	0:07:34
3.1	Ids vs Vgs (find range)	3.41	71	0:04:02
3.2	**Ids vs Vgs (thr)**	3.41	2,130	2:01:03
4.1	**Ids vs Vgs (sub) (Vds = 0.01 V, Vbs = 0 V)**	3.17	221	0:11:41
4.2	**Ids vs Vgs (sub) (Vds = 0.01 V, Vbs = 15 V)**	3.17	221	0:11:03
4.3	**Ids vs Vgs (sub) (Vds = 0.01 V, Vbs = 30 V)**	3.17	221	0:11:03
4.4	**Ids vs Vgs (sub) (Vds = 0.01 V, Vbs = 50 V)**	3.17	221	0:11:03
4.5	**Ids vs Vgs (sub) (Vds = 0.01 V, Vbs = 70 V)**	3.17	221	0:11:03
4.6	**Ids vs Vgs (sub) (Vds = 0.01 V, Vbs = 90 V)**	3.17	221	0:11:03
5.1	Adjust gate and drain values	-	-	0:10:00
5.2	**Ids vs Vds**	4	882	0:58:48
6.1	Turn off Keithley outputs	-	-	0:01:00
6.2	Move the DUT from the X-ray machine to the CV setup	-	-	0:05:00
6.3	Change cables	-	-	0:05:00
6.4	Set jumpers and jumper cables based on the photo	-	-	0:02:00
6.5	**C-Vgb (source, drain to bulk)**	14.79	300	1:13:57
7.1	Change cables	-	-	0:02:00
7.2	Set jumpers and jumper cables based on the photo	-	-	0:05:00
7.3	**C-Vsb (drain to source, gate float)**	14.79	360.00	1:28:44
8.1	Move the DUT from the CV setup to the X-ray machine	-	-	0:05:00
8.2	Set jumpers back	-	-	0:01:00
8.3	Remove the plastic cap	-	-	0:01:00
8.4	Align the DUT	-	-	0:01:00
8.5	Turn on Keithley outputs	-	-	0:01:00
8.6	Check Voltage, Current and timer of X-ray machine	-	-	0:02:00



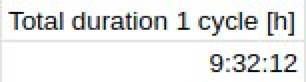
Total duration 1 cycle [h]
8:57:42

MEASUREMENT PROTOCOL 11.2022-12.2022 IRRAD SHIN-ETSU



	Action	Avg iter time (s)	# meas points	Duration
0.1	**Irradiate**			
0.2	**Anneal for 1h**	-	-	1:00:00
1.1	Open relay switch	-	-	0:01:00
1.2	**I_avalanche**	8.15	93	0:12:38
2.1	Close relay switch	-	-	0:01:00
2.2	**Ibs vs Vbs (sensor-like IV)**	4.09	333	0:22:42
3.1	Ids vs Vgs (find range)	3.41	71	0:04:02
3.2	**Ids vs Vgs (thr)**	3.41	2,130	2:01:03
4.1	**Ids vs Vgs (sub) (Vds = 0.01 V, Vbs = 0 V)**	3.17	221	0:11:41
4.2	**Ids vs Vgs (sub) (Vds = 0.01 V, Vbs = 15 V)**	3.17	221	0:11:03
4.3	**Ids vs Vgs (sub) (Vds = 0.01 V, Vbs = 30 V)**	3.17	221	0:11:03
4.4	**Ids vs Vgs (sub) (Vds = 0.01 V, Vbs = 50 V)**	3.17	221	0:11:03
4.5	**Ids vs Vgs (sub) (Vds = 0.01 V, Vbs = 70 V)**	3.17	221	0:11:03
4.6	**Ids vs Vgs (sub) (Vds = 0.01 V, Vbs = 90 V)**	3.17	221	0:11:03
5.1	Adjust gate and drain values	-	-	0:10:00
5.2	**Ids vs Vds**	5.5	882	1:20:51
6	Sleep 3 hours and 10 minutes	-	-	3:10:00
7	Check DUT alignment	-	-	0:01:00
8	Adjust irradiation settings	-	-	0:01:00

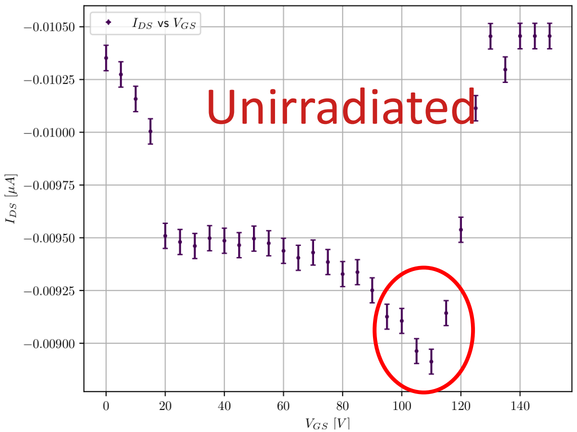
To keep the same annealing time as in the previous campaign



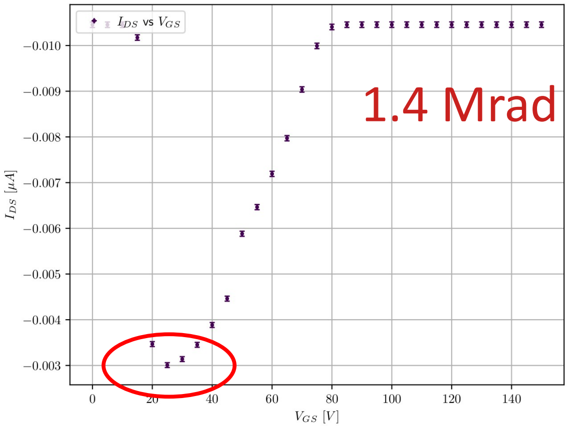
Total duration 1 cycle [h]
9:32:12

AVALANCHE CURRENT MEASUREMENT (I_avalanche) SHIN-ETSU

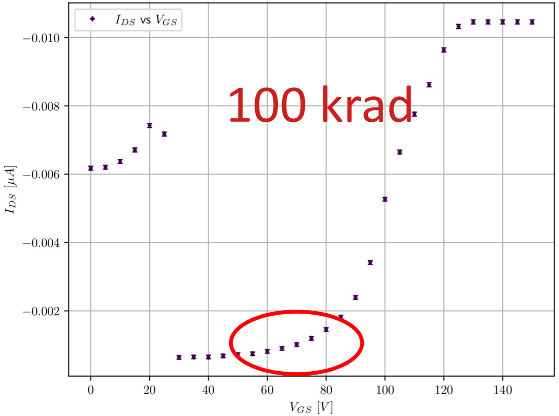
- Shin-Etsu
- V_{DS} = 0 V, V_{BS} = 30 V
- Measurement before irradiation
- Onset indeed **shifts to lower voltages** with irradiation
- From onset the oxide charge can be calculated
- Measurements also for V_{BS} = 35 V and V_{BS} = 40 V (see backup)



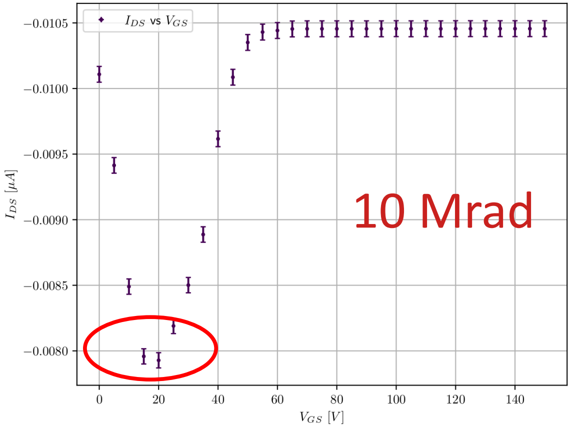
Unirradiated



1.4 Mrad

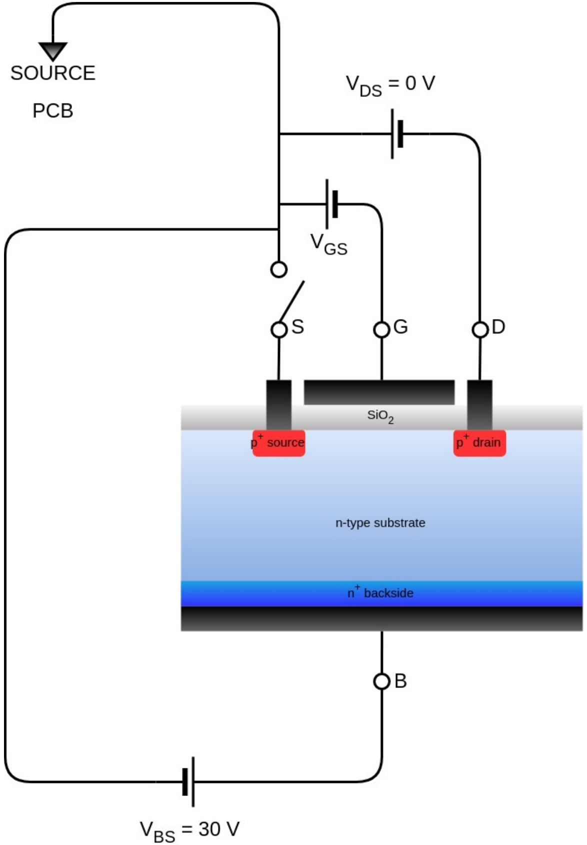


100 krad



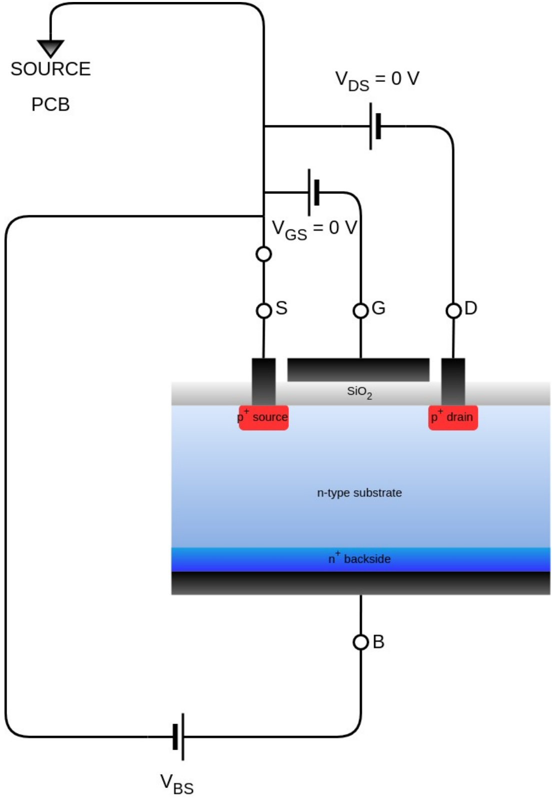
10 Mrad

AVALANCHE CURRENT MEASUREMENT (I_avalanche) SETUP



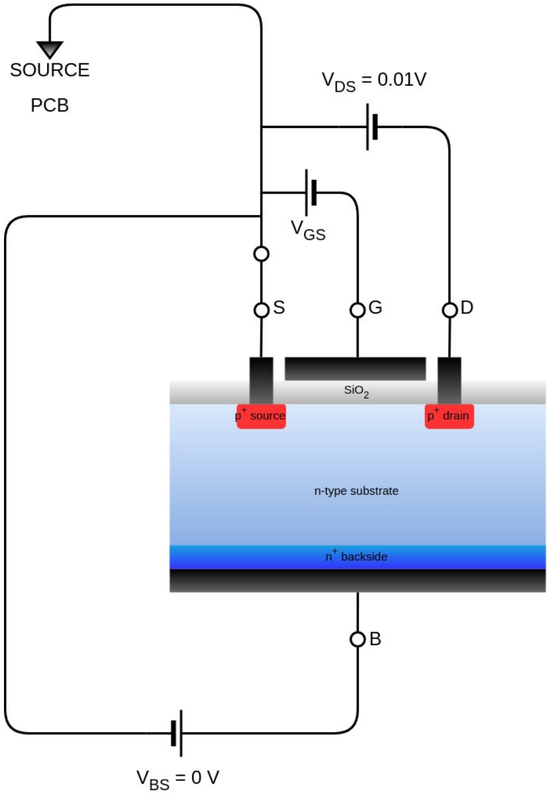
- Source implant floating
- V_{DS} = 0 V, V_{BS} = 30 V, scan over positive V_{GS}

BULK IV (I_{BS} vs V_{BS}) SETUP



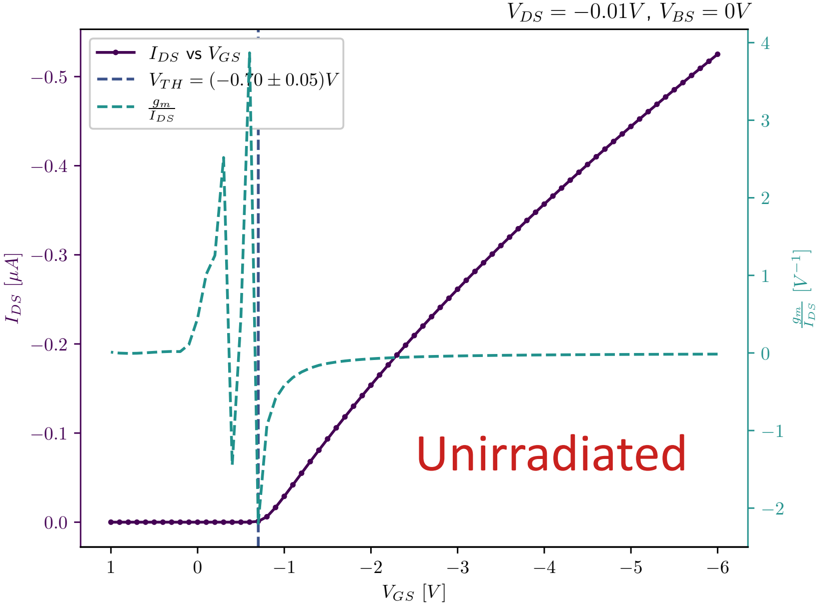
- V_{DS} = 0 V, V_{GS} = 0 V, scan over positive V_{BS}
- Measurements for V_{GS} = -5 V, 5 V as well

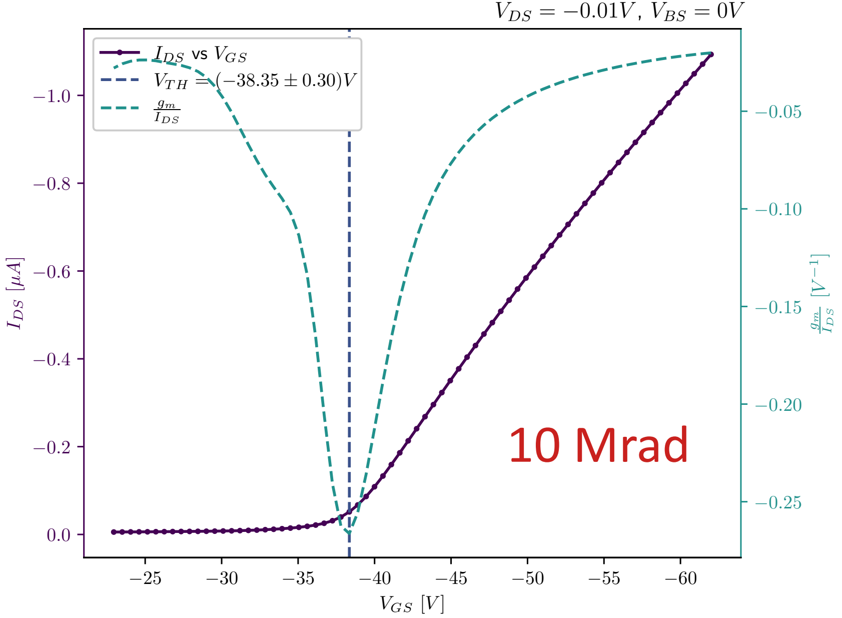
GATE THRESHOLD VOLTAGE MEASUREMENT (I_{DS} vs V_{GS} (thr)) SETUP



- V_{DS} = 0.01 V, V_{BS} = 0 V, scan over negative V_{GS}
- IVs also for different V_{BS} values

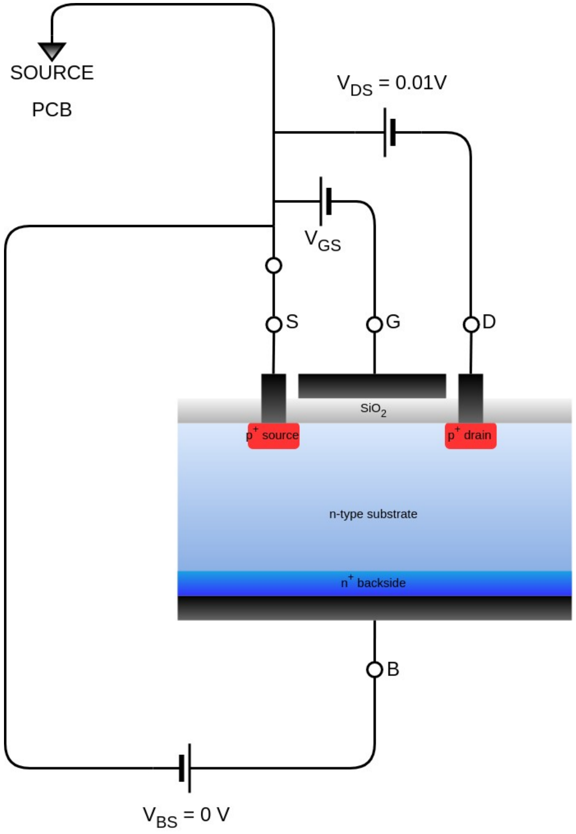
GATE THRESHOLD VOLTAGE MEASUREMENT (I_{DS} vs V_{GS} (thr))
SHIN-ETSU





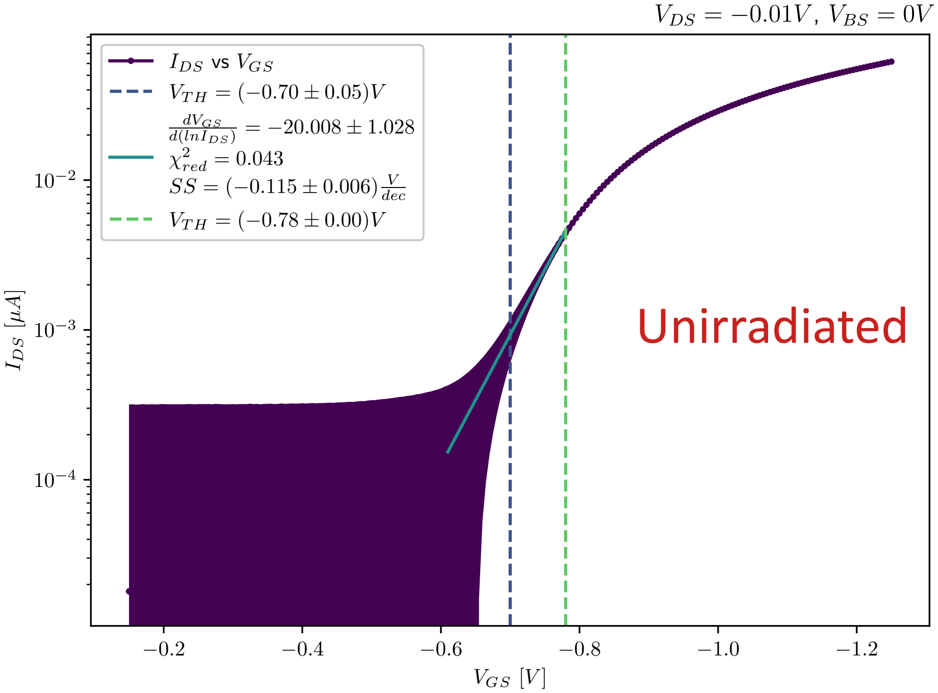
- Use minimum of g_m/I_{DS} to determine the threshold
- Noise can affect the measurement (especially the baseline)
- Hardware will be further improved with TRIAX cables and a special DUT box (Faraday cage)

GATE SUB-THRESHOLD SWING MEASUREMENT (I_{DS} vs V_{GS} (sub)) SETUP

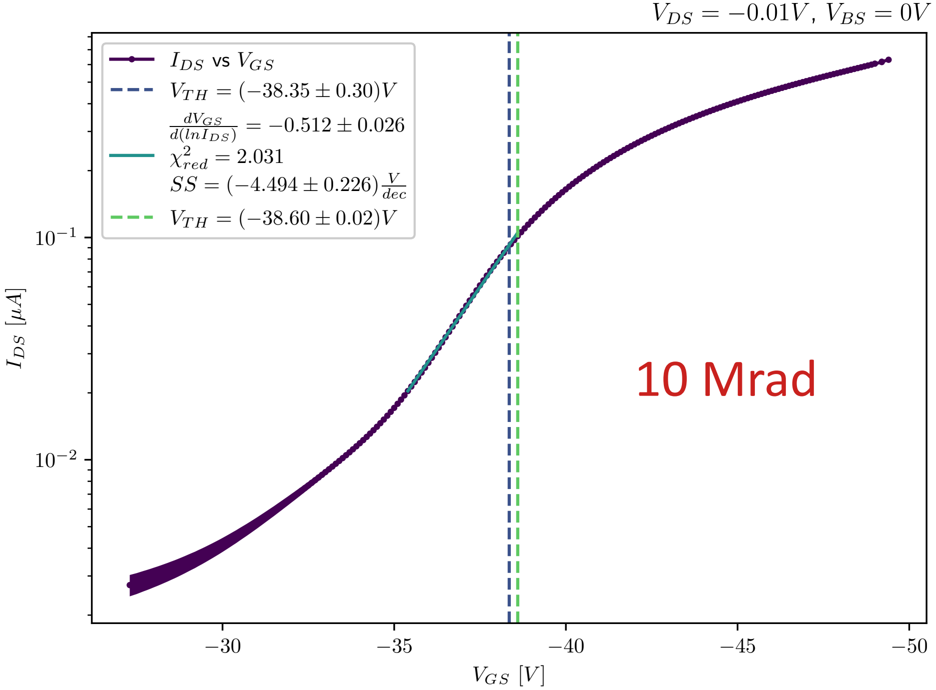


- V_{DS} = 0.01 V, V_{BS} = 0 V, fine scan over negative V_{GS}
- IVs also for different V_{BS} values

GATE SUB-THRESHOLD SWING MEASUREMENT (I_{DS} vs V_{GS} (sub)) SHIN-ETSU

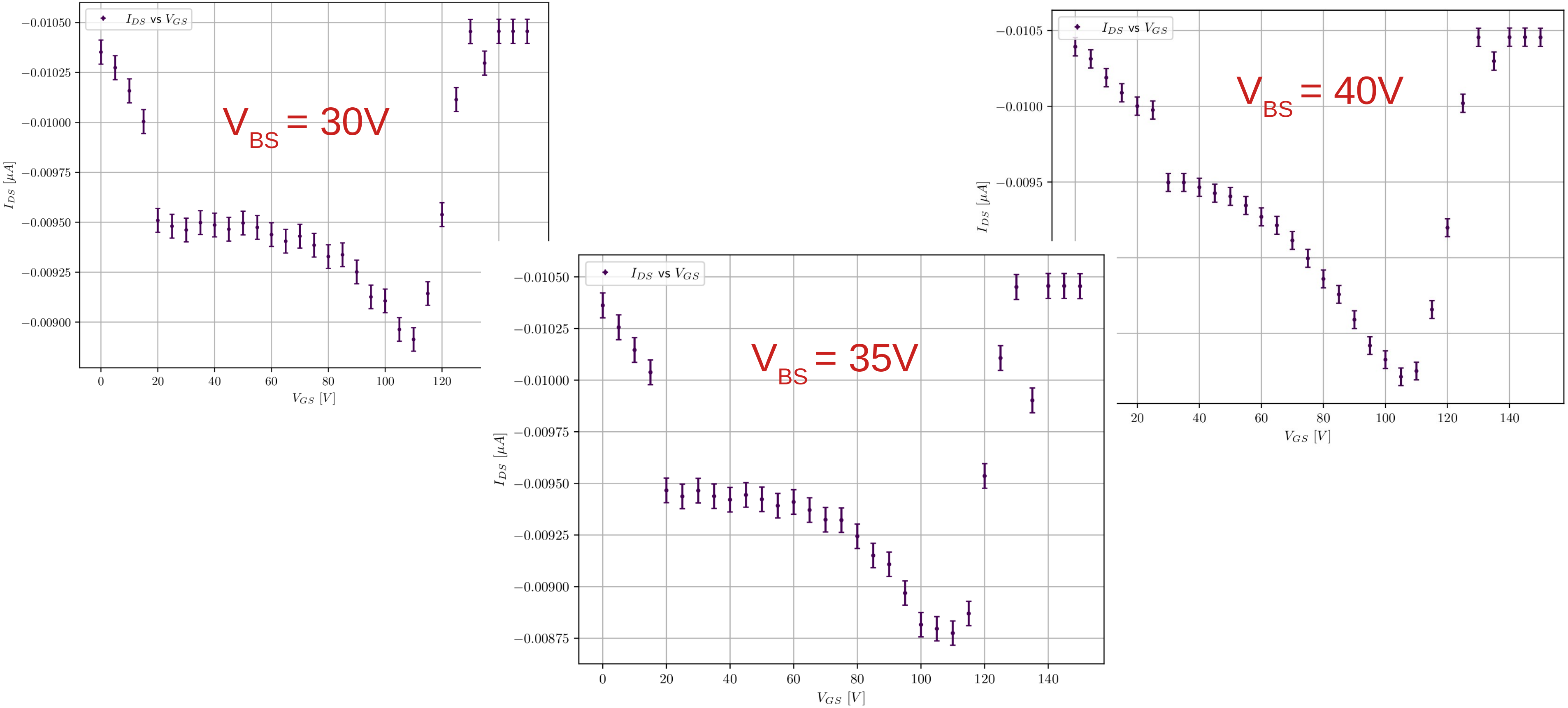


Unirradiated

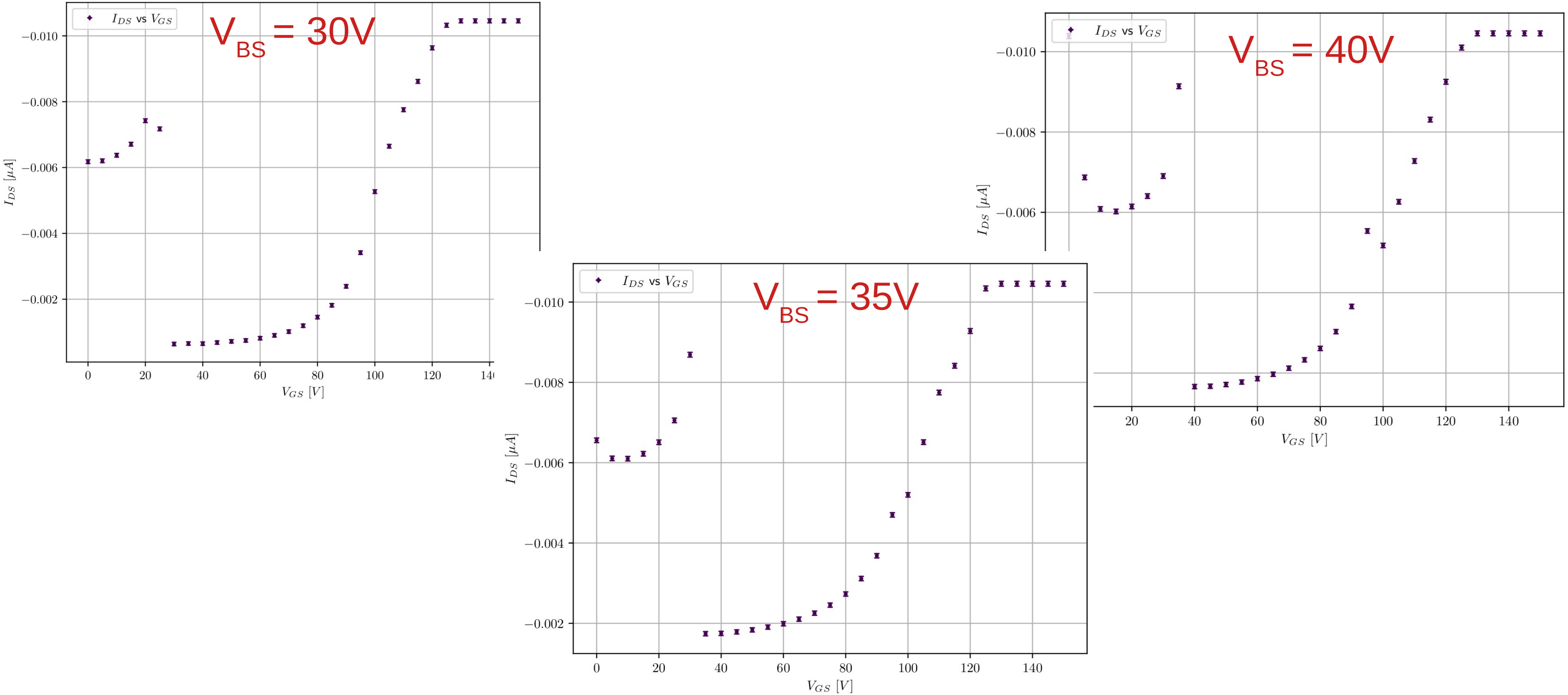


10 Mrad

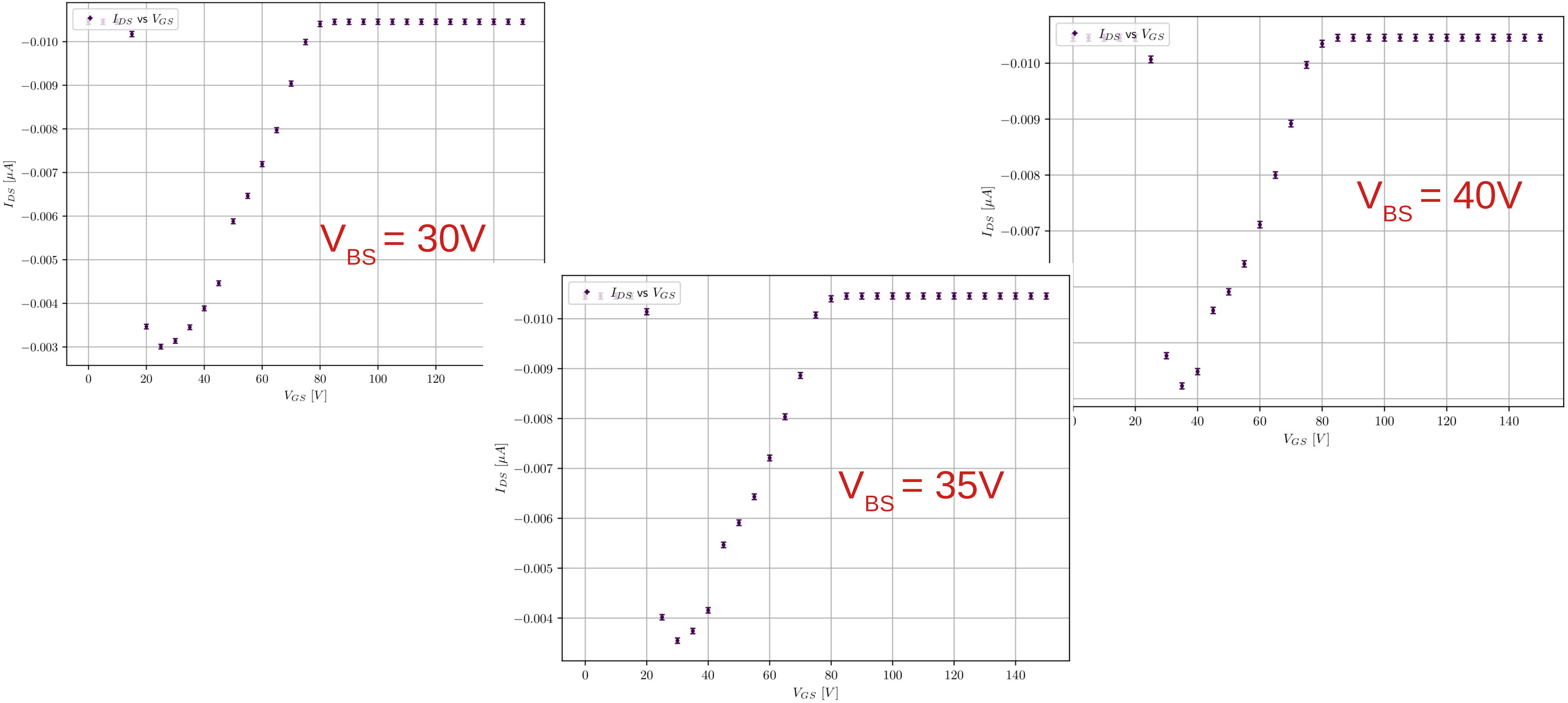
AVALANCHE CURRENTS SHIN-ETSU UNIRRADIATED



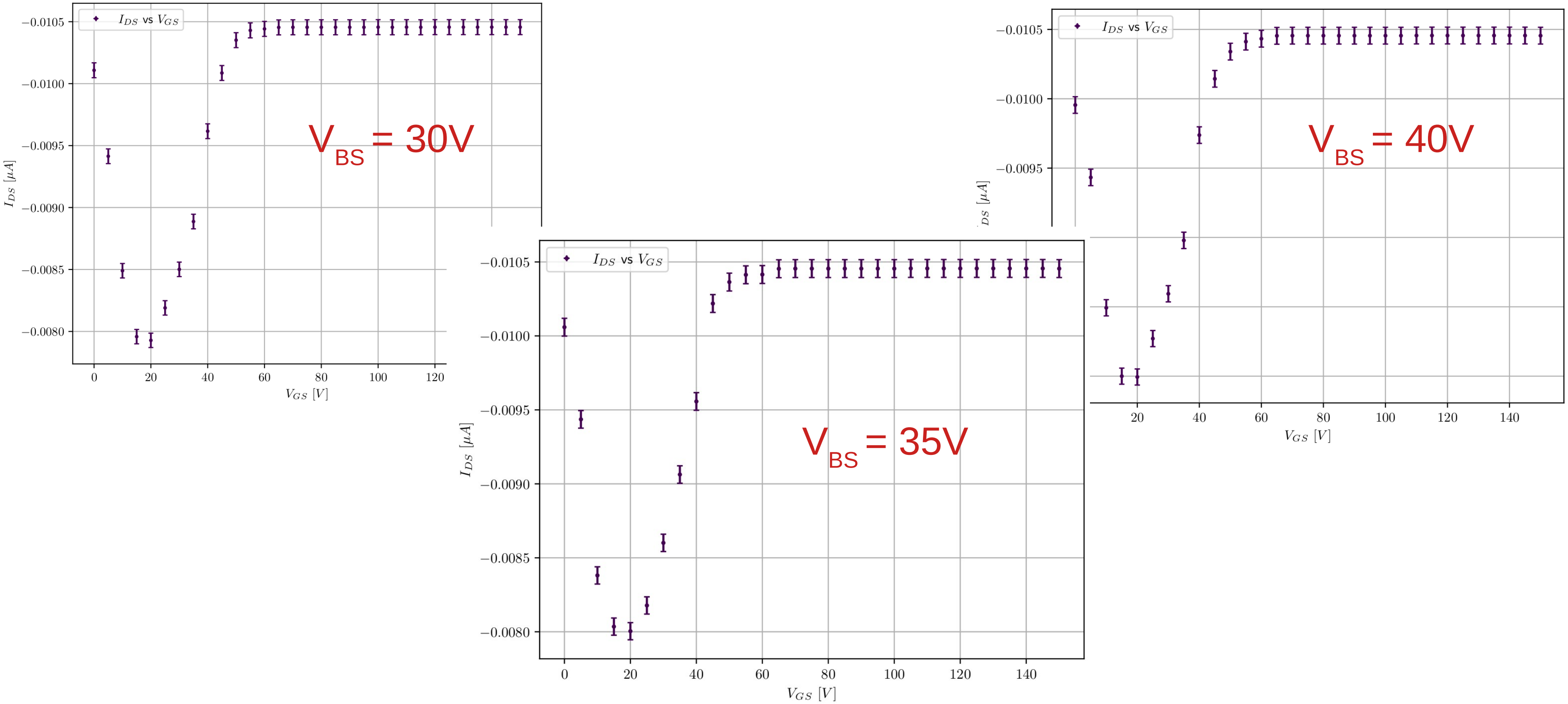
AVALANCHE CURRENTS SHIN-ETSU
100 krad



AVALANCHE CURRENTS SHIN-ETSU
1.4 Mrad



AVALANCHE CURRENTS SHIN-ETSU
10 Mrad



AVALANCHE CURRENTS SHIN-ETSU 10 Mrad

- Look at the area around the threshold and measure in small steps
- Plot with logarithmic y-axis
- Analysis steps
- Smooth log(y) using spline interpolation (4th order).
- Data is slightly smoothed while shape is completely preserved
- This step is needed to achieve smooth df(x)/dx and d2f(x)/dx2
- Calculate df(x)/dx and d2f(x)/dx2
- Locate point of inflection
- df(x)/dx is minimum
- d2f(x)/dx2 = 0 (cross-check)
- Locate minimum and maximum of d2f(x)/dx2 around the inflection point
- Beyond these points the curve is not linear anymore and the curve should not be fitted
- Smoothing factor needs to be tuned or the optimum factor needs to be found for every curve individually

- If smoothing factor too large -> interpolated linear region is altered -> fitting range gets larger -> not the best fit to the actual data

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