GDL
Payloads
ECLBkgOverlay
Server
VME

H. Nakazawa (NTU)
20230208@B2GM

GDL Transition to UT4

- vu160 version

- ETM-GDL connection
  - With GDL==vu080, delivered timing was unstable, often after deadline.
    Planned to change protocol to 12Gbps (available only on UT4) to reduce latency.
  - But Unno-san allowed to use hidden latency budget (~100ns) on UT3ETM.
    => Tried to adjust timing using the budget with UT4GDL(vu160) and ETM(UT3).
    => Latency is same as UT3-UT3 and stable.

- Will move GDL to UT4 with 5Gbps GDL-ETM link after B2L readout test.
  - Need to change LVDS cable between GDL and GRL

- TOPTRG-GDL connection
  - 12Gbps on UT4
    UT3; 32 bit * 4lanes
    topt9: lane1(17 downto 0)
    topcc: lane0(31 downto 21)
    topvd: lane0(20)
    UT4; 96 bit * 4lanes
    topt9: lane0(49 downto 32)
    topcc: lane0(31 downto 21)
    topvd: lane0(20)
  - YunTsung modification necessary as GDL-ETM link ?

Automation of GDL payload production

- Scripts finalized https://stash.desy.de/projects/B2/repos/basf2/pull-requests/1447/overview
- Applied to entire exp region, exp 7 - exp 26

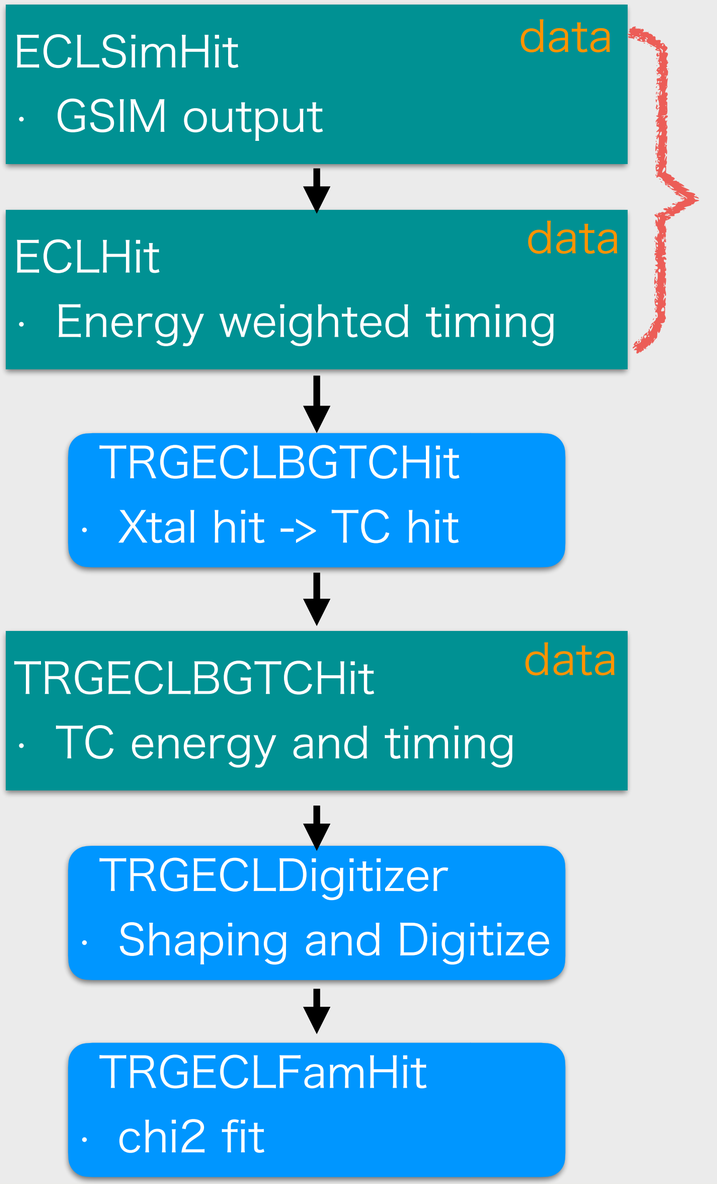
Wrong/Missing values

e7r3219 - e7r4025	5 largest output bits, 133 - 137 are missing	Monitor bits.
e7r3219 - e7r3238	PS of bit 32 (c4) is 1, but should be 0.	9 runs.
e7r4026 - e8r1199	9 largest output bits, 133 - 141 are missing	Monitor bits.
e8r1200 - e8r1201	11 largest output bits, 133 - 143 are missing	Monitor bits.
e8r1202 - e8r2044	2 largest output bits, 142 - 143 are missing	bit 142 (fffo) with PS=1, but logically included in fff.
e8r2045 - e8r2778	5 largest output bits, 142 - 146 are missing	
e8r2779 - e10r134	11 largest output bits, 142 - 153 are missing	
e10r5729 - e10r5902	PS of bit 135 (hiev) is 1, but should be 2000	30 runs
e12r5379 - end of e12	Input bits 42 - 45 are bha_type_10 - bha_type_13, must be tx_0 - 3	No one uses
	Output bits 153 - 156 are bhabrl, bhamtc1, bhamtc2, bhaf, which should be bhamtc1, y2, y3, y4.	All PS=0
e18r2640	PS of stt4, stt5, stt6 are 1, but should be 0.	Short run.

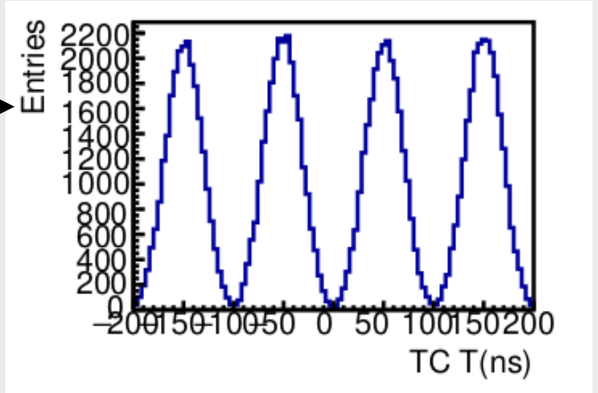
Algorithm changes which are not properly recorded in payloads

	Exp	bit		
fso	12	18	Angle requirement, cdc_open90 -> s2fo	PS=0
fsb	12	23	Angle requirement, cdc_b2b5 -> s2f5	
sso	12	19	Angle requirement, cdc_open90 -> s2so	
ssb	12	24	Angle requirement, cdc_b2b5 -> s2s5	
mu_b2b	12	67	klmb2b (3bit) > 0 -> klmb2b (1bit). t2>0 requirement removed.	PS=0,1
ggsel	14	158	Missing !veto -> added.	PS=0,1,10

ECL background study



- Goals
  - Data and MC Validity check
    - Bug fix if any
      - TRGECLBGTCHit data looks strange
      - TRGECLDigitizer output looks strange
    - Adjustment of timing window size
      - The narrower the better to reduce data size
    - Adjustment of mixing parameter (?)
    - Make tools
  - Estimate future trigger rate with higher background
  - No idea of time scale an urgency



Status and Summary

- New VME board
  - Present one no longer available in market. No more spares.
  - New ones, ~10, already purchased.
  - Collecting information
  - Asked Nakao-san who purchased same board.

- Move to btrgsrv2/3 in Ehut
  - Need to complete slow control

- Stuck incomplete/almost-complete tasks
  - Server (2w) > UT4 (2w) > PR of Payload (2w) > ECLBg (2m) > VME (?)

Nakao-san's New board

"FAIL" is on

Connected to daqnet