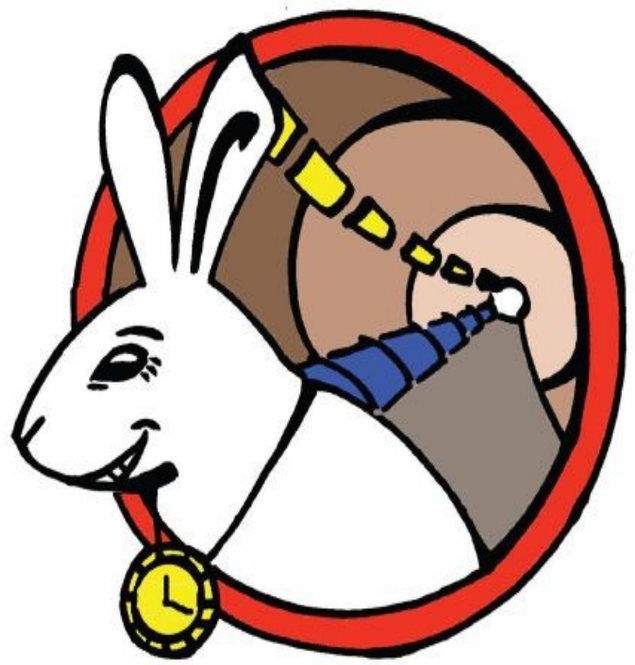
Laboratoire de Physique des 2 infinis Irène Joliot-Curie

l'Observatoire de Paris | SYRTE

Systèmes de Référence Temps-Espace



WhiteRabbit
Time dissemination

B2GM FEB-13-2023
D.Charlet, C.Viou, PE.Pottie

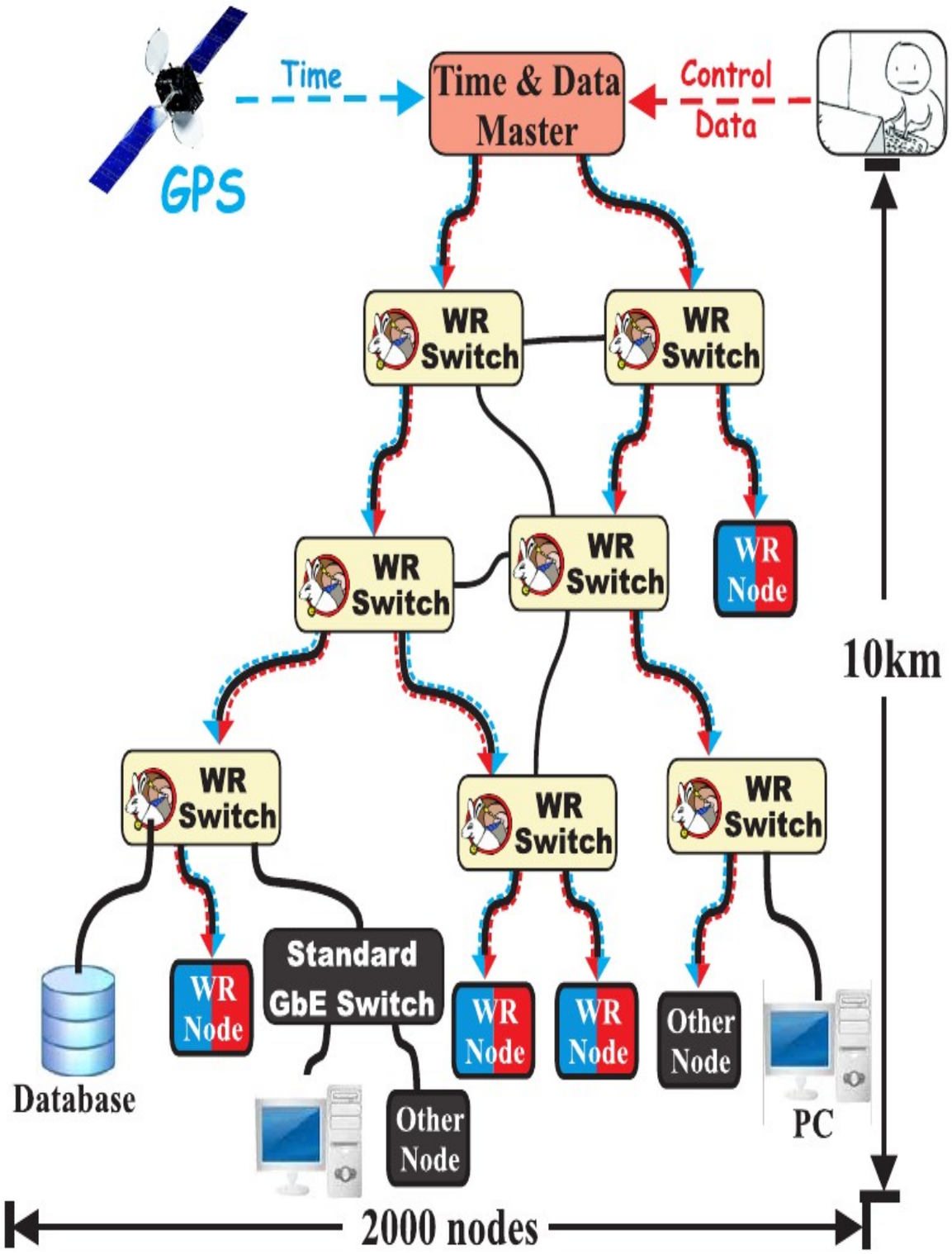
cnrs

Station de Radioastronomie de Nançay

Outline

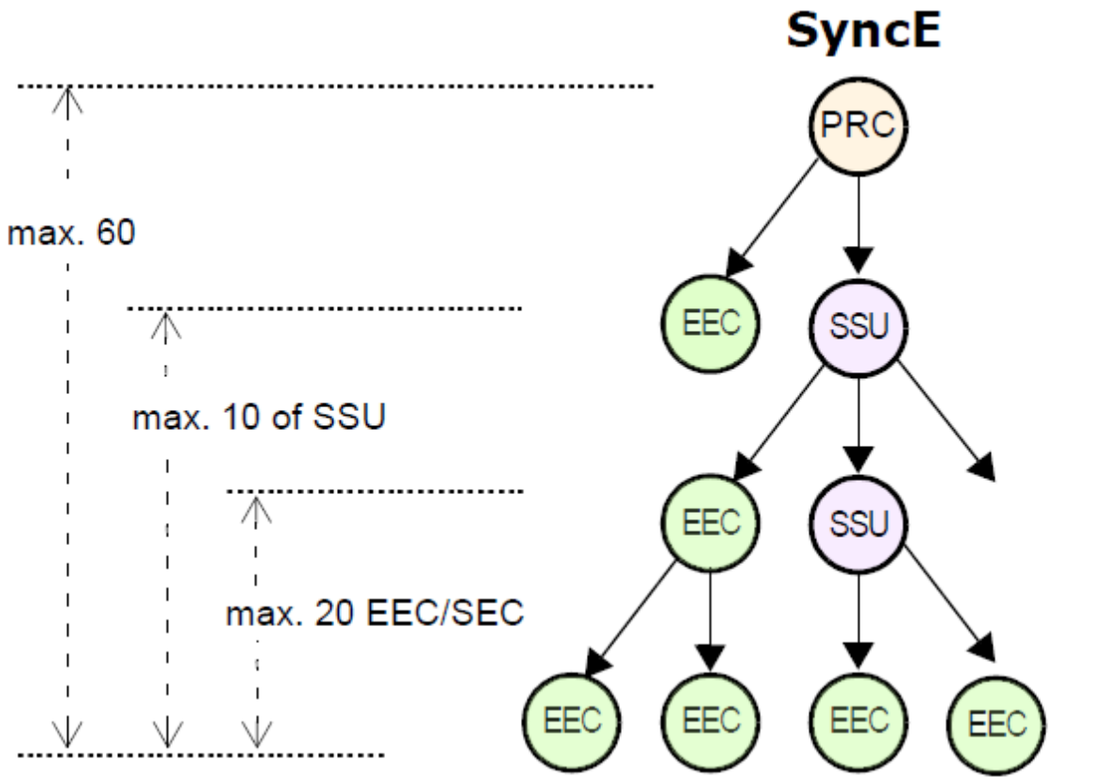
- WhiteRabbit overview
- IDROGEN board
- Research &Technology project : TIMED
- T+R’EFIMEVE infrastruture
- PCIe400
- PAON IV detector

White Rabbit principle : Enhanced Ethernet

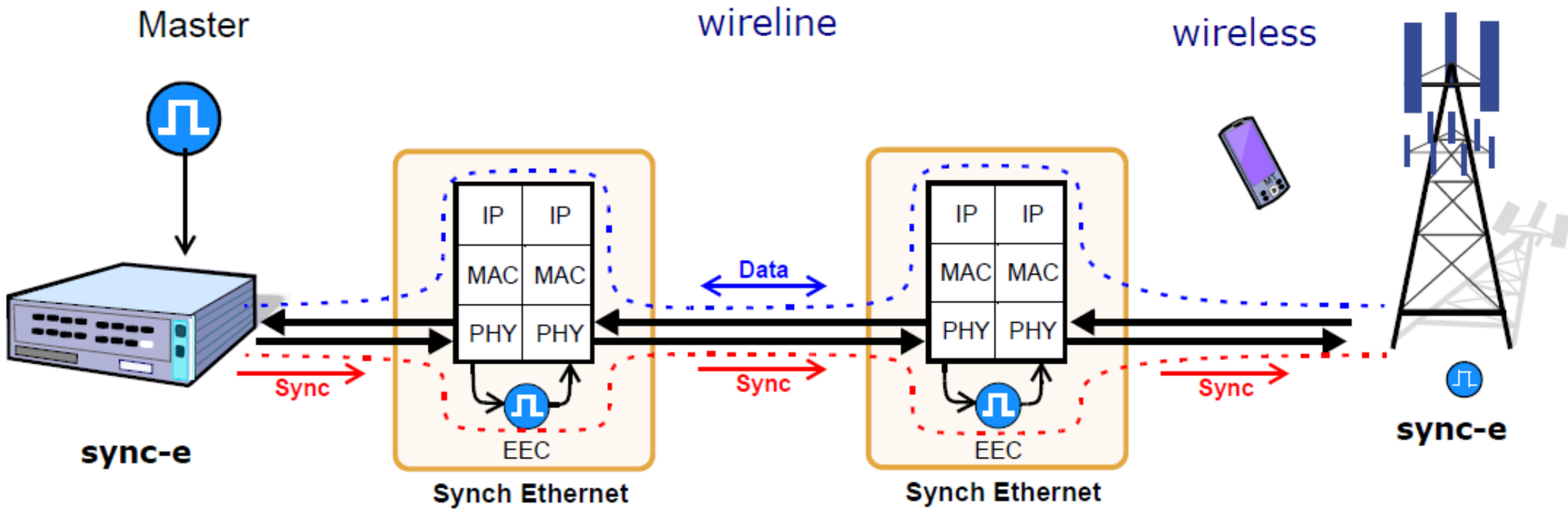


- An extension of Ethernet which provides :
  - Synchronous mode (Syn-E) – common clock for physical layer in entire network, allowing for precise time and frequency transfer
  - Deterministic routing latency – a guarantee that packet transmission delay between two stations will never exceed a certain boundary.
- Technology overview
  - Precision Time Protocole (IEEE1588)
  - Synchronous Ethernet
  - DDMTD Phase tracking (Digital Dual Mixer Domain) …

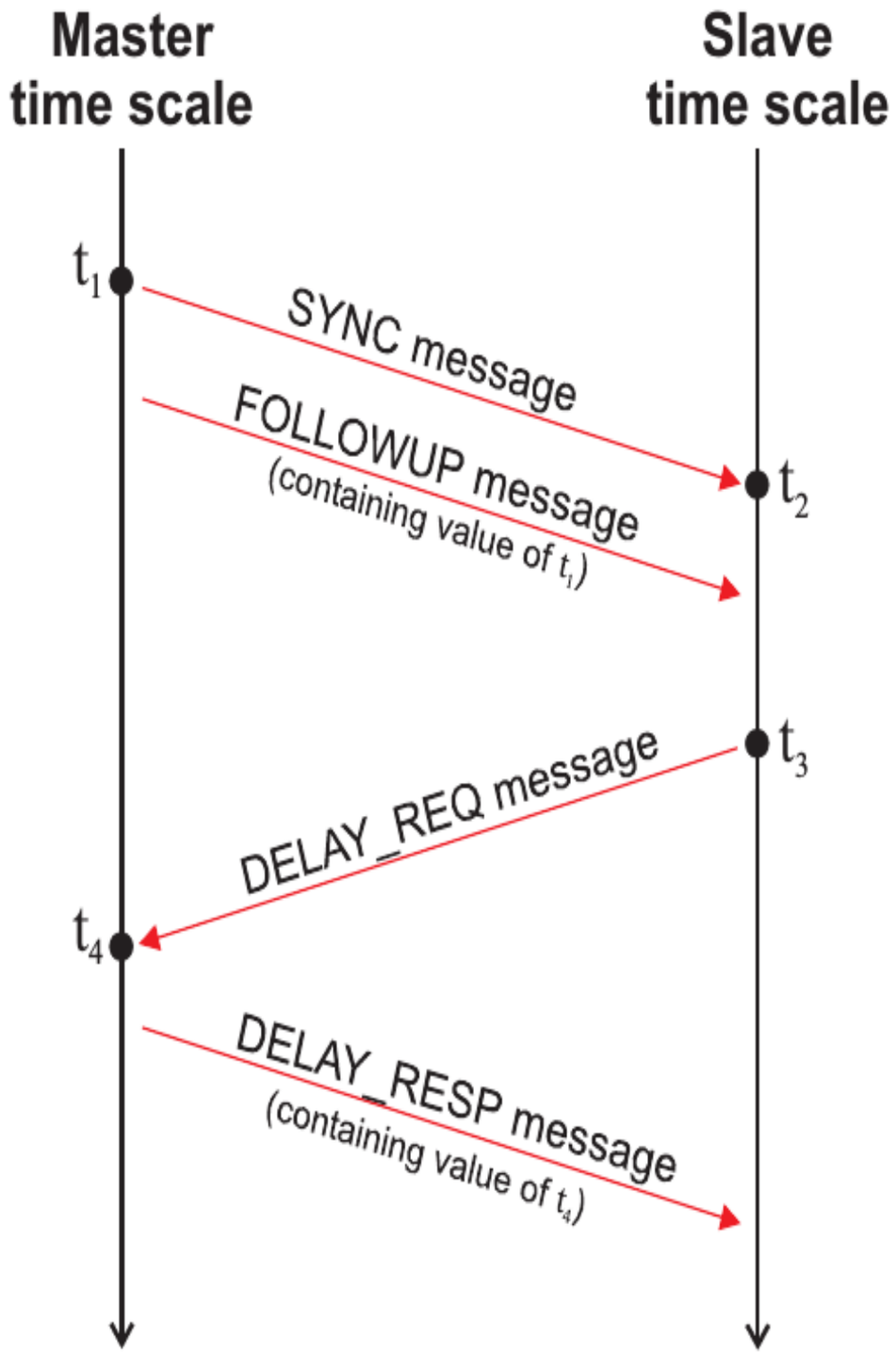
Synchronous Ethernet (Sync-E)



- All network nodes use the same physical layer clock,
- Clock is encode in the Ethernet carrier and recovered by the receiver chip(PHY)
- A master and unique clock for the whole network
- Synchronous digital hierarchy
- High precision clock definition, 20 better than standard Ethernet clock



Precision Time Protocol (IEEE1588)



- Packet-based synchronization protocol
- Synchronizes local clock with the master clock by measuring and compensating the delay introduced by the link.
- Link delay evaluated by measuring and exchanging packets tx/rx timestamps
- PTP is used only for compensation of the clock offset

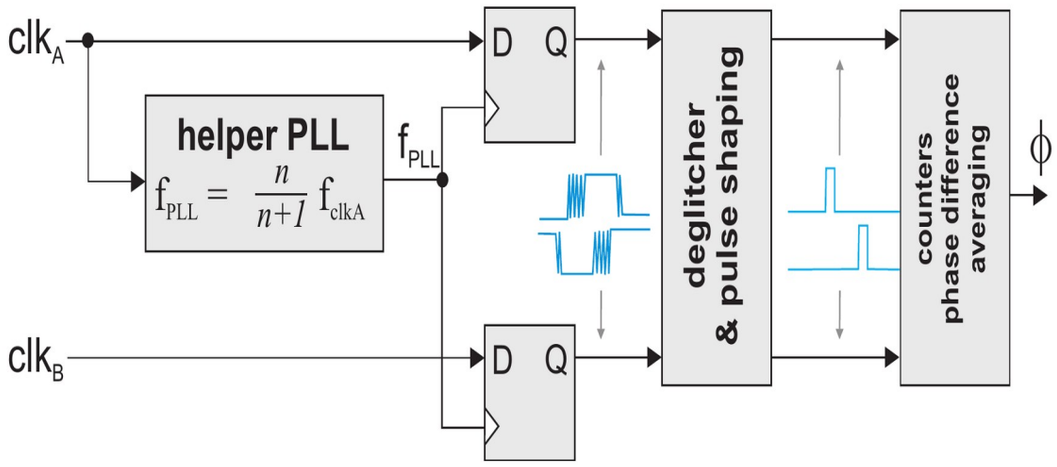
Having values of t1 ...t4 , slave can:

- calculate one-way link delay:

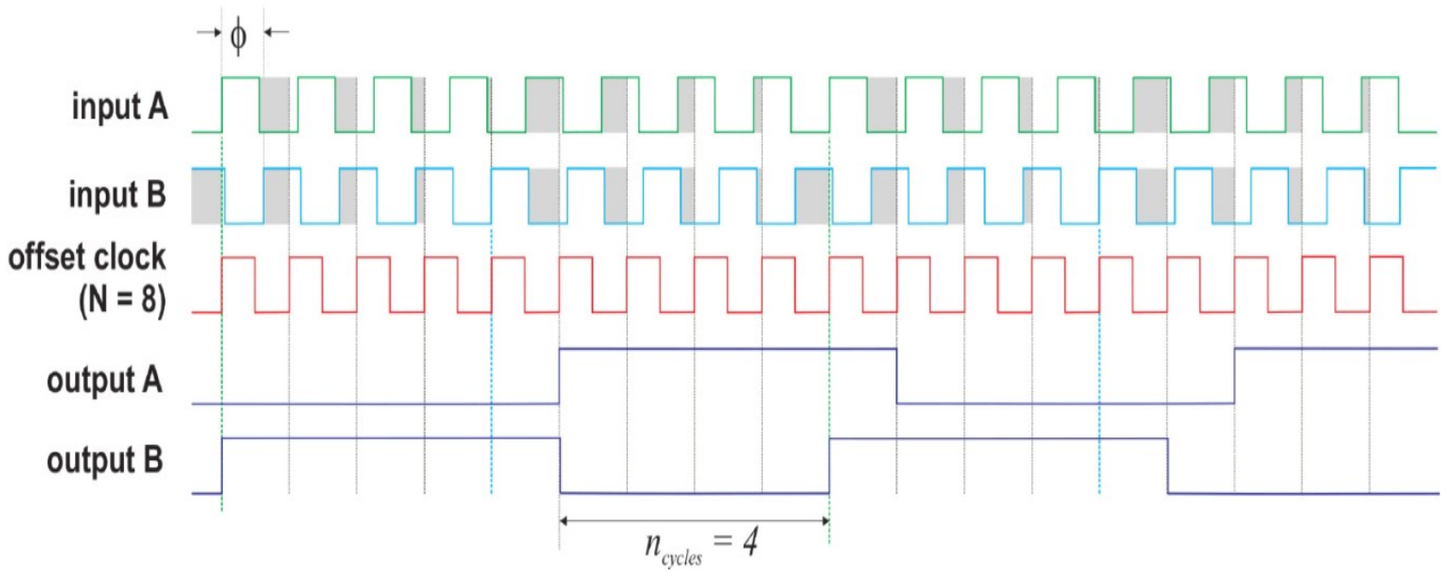
$$\delta ms = ((t4 - t1) - (t3 - t2))/2$$

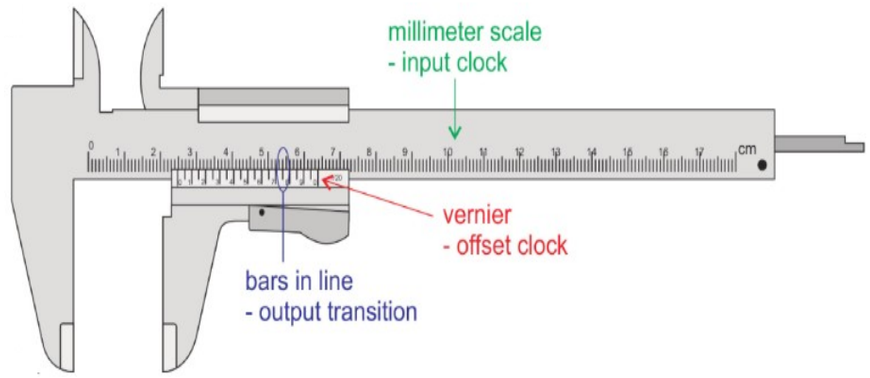
- syntonize its clock rate with the master by tracking the value of
  t2 − t1
- compute clock offset:
  offset = t2 − t1 + δms

Digital Dual Mixer Time Domaine phase detector (DDMTD)



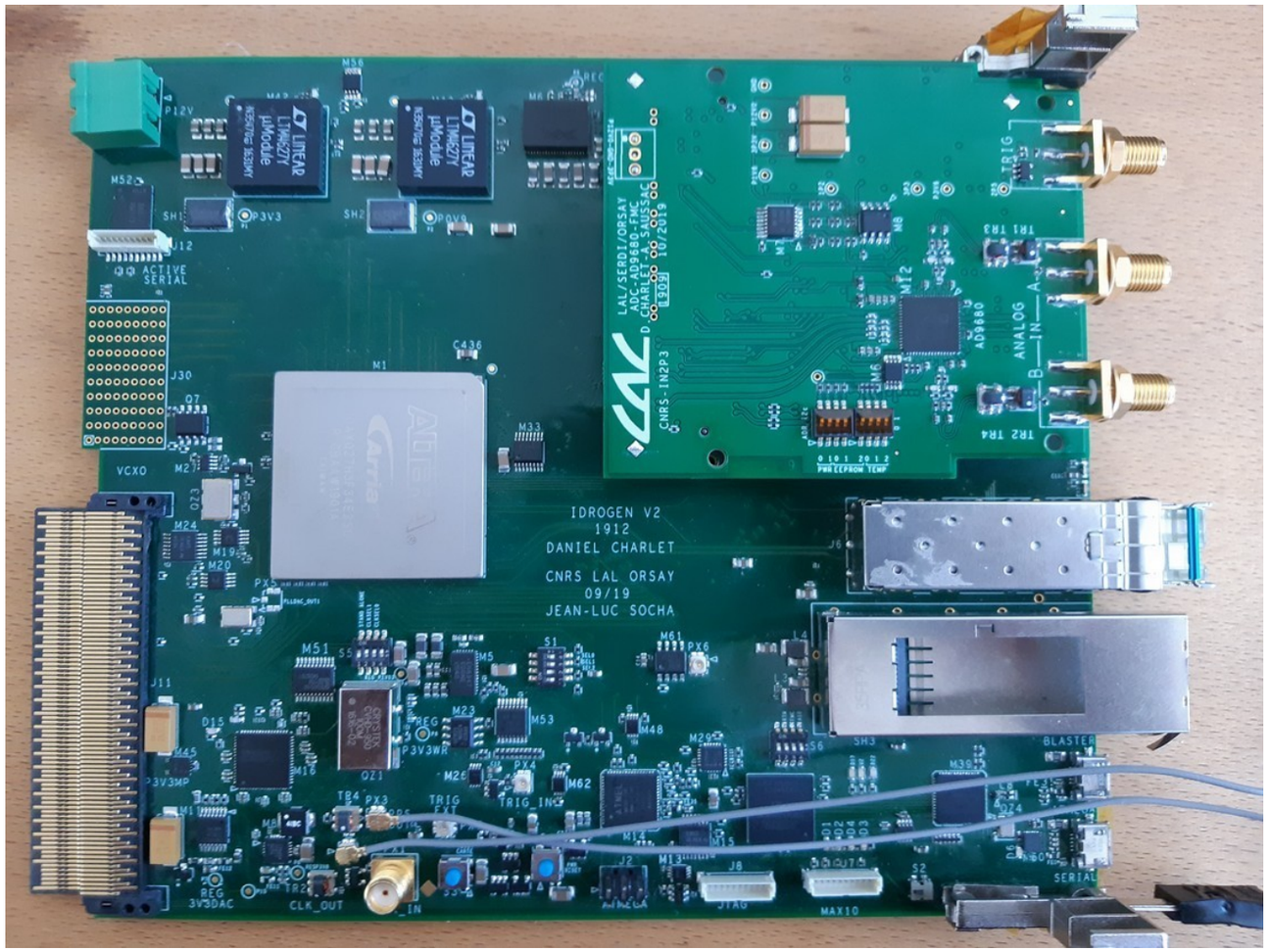
- Measure the phase shift between transmit and receive clock on
- the master side, taking the advantage of Synchronous Ethernet.
- Monitor phase of bounced-back clock continuously.
- Phase-locked loop in the slave follows the phase changes measured by the master.





IDROGEN board

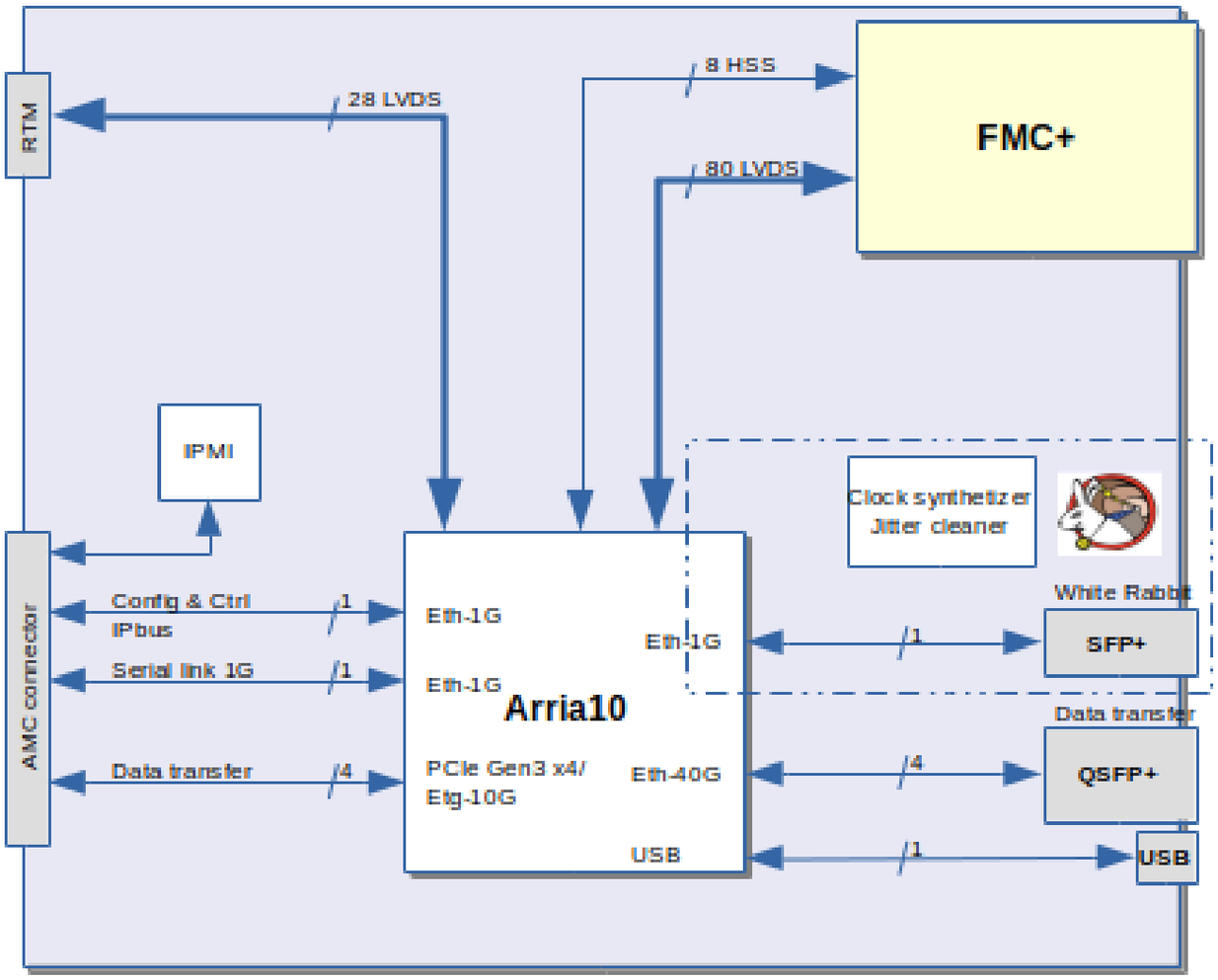
Low phase noise WR -PTP : IDROGEN



- High performance WR low jitter
  - Expertise from SYRTE for clock & qualification
- Design & realization by IJCLAB
- Firmware by Nancay Observatory
- Measures at SYRTE and IJCLAB

http://www.ohwr.org/projects/white-rabbit/wiki/WRReferenceDesign

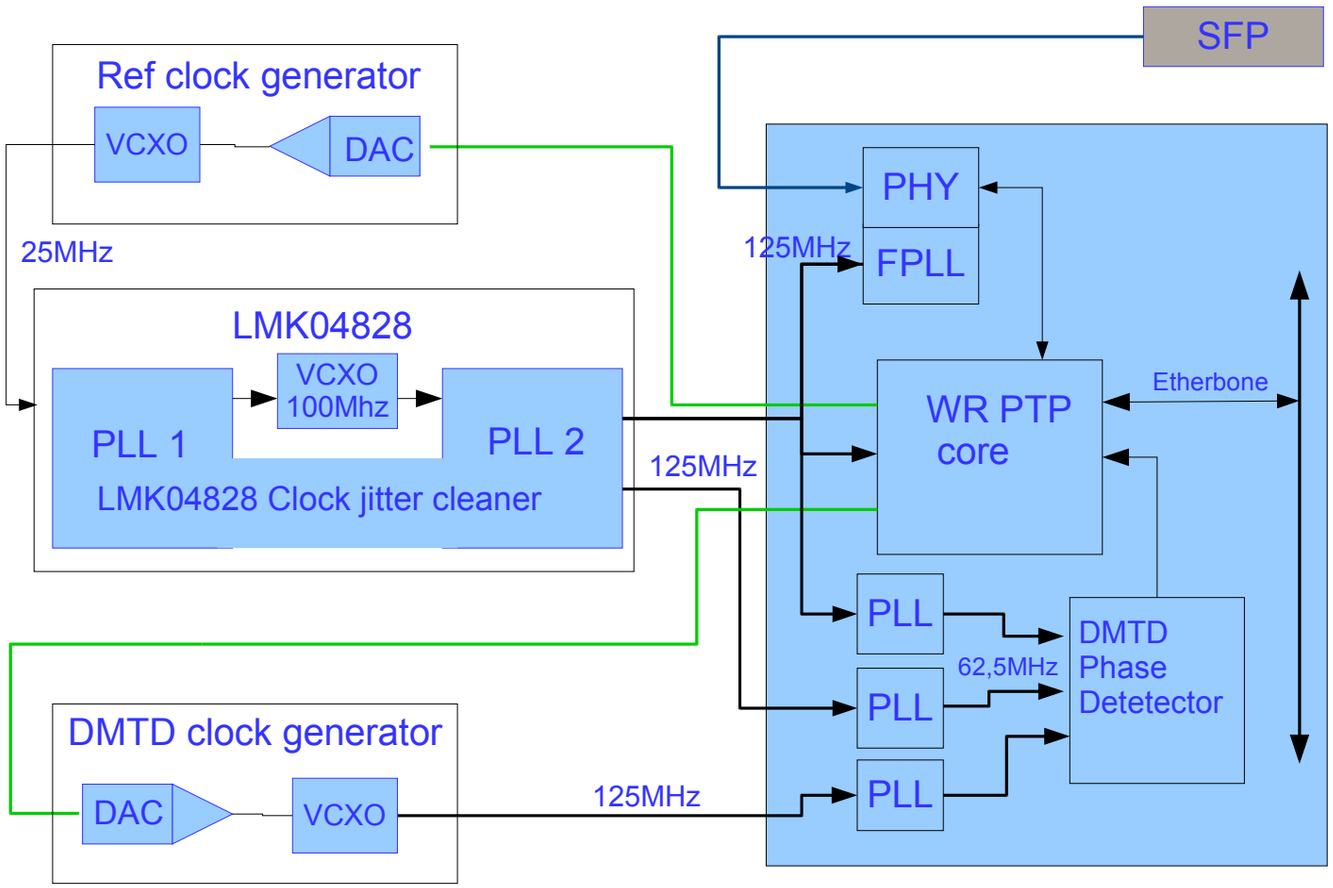
IDROGEN main features



- MTCA 4.0 standard, double width full-size
- Stand-alone mode
- VITA57.1 (FMC slot)
  - 160 single-ended I/Os (80 LVDS) and/or up to 10 serial transceivers in a 40 x 10 configuration
- Full WhiteRabbit compliant.
- Front panel conectivity
  - WR SFP+
  - QSFP+ 40G, USB
- Backplane connectivity
  - 1Gbe IPbus,PCI 4x Gen3,
  - IPMB, CLK & trigger lane.
  - RTM connector : J30

http://www.ohwr.org/projects/white-rabbit/wiki/WRReferenceDesign

WhiteRabbit : DAQGEN implementation

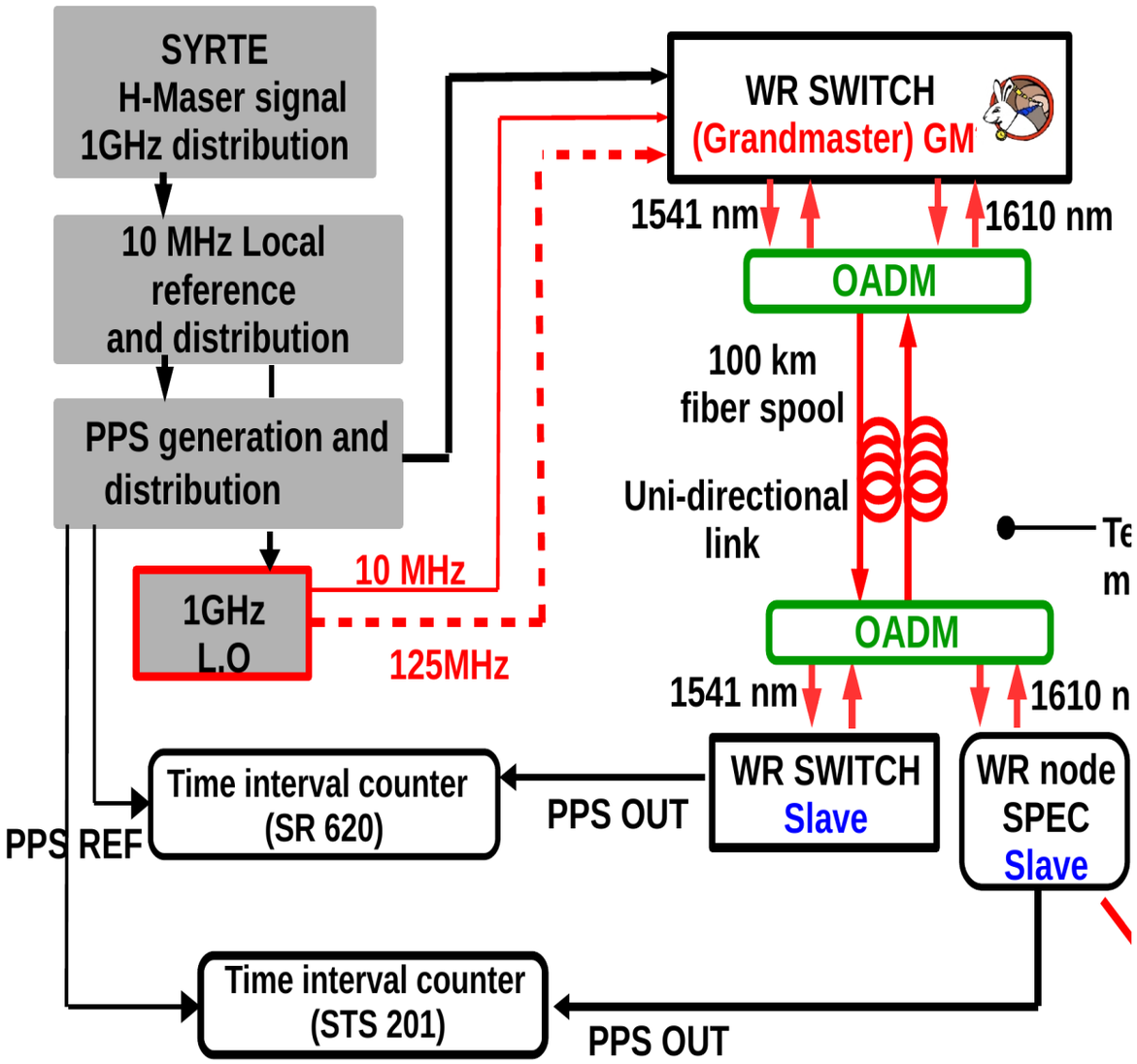


The WhiteRabbit IDROGEN hardware is based on CERN open hardware with Enhancements

- Based on LMK4828 synthetiser
  - Ultra low noise clock jitter Cleaner with Dual Loop PLL
  - 90fs RMS jitter.
- DDMTD internal of FPGA (placement with constraint)
- Two generated local clocks :
  - DDMTD source (comparison between WR master clock from SFP)
  - PLL source with phase adjustment
- **IDROGEN Enhancements**
  - PLL selection
  - VCXO Frequency
  - Input frequency for DDMTD)
  - Tx/Rx routing equalisation

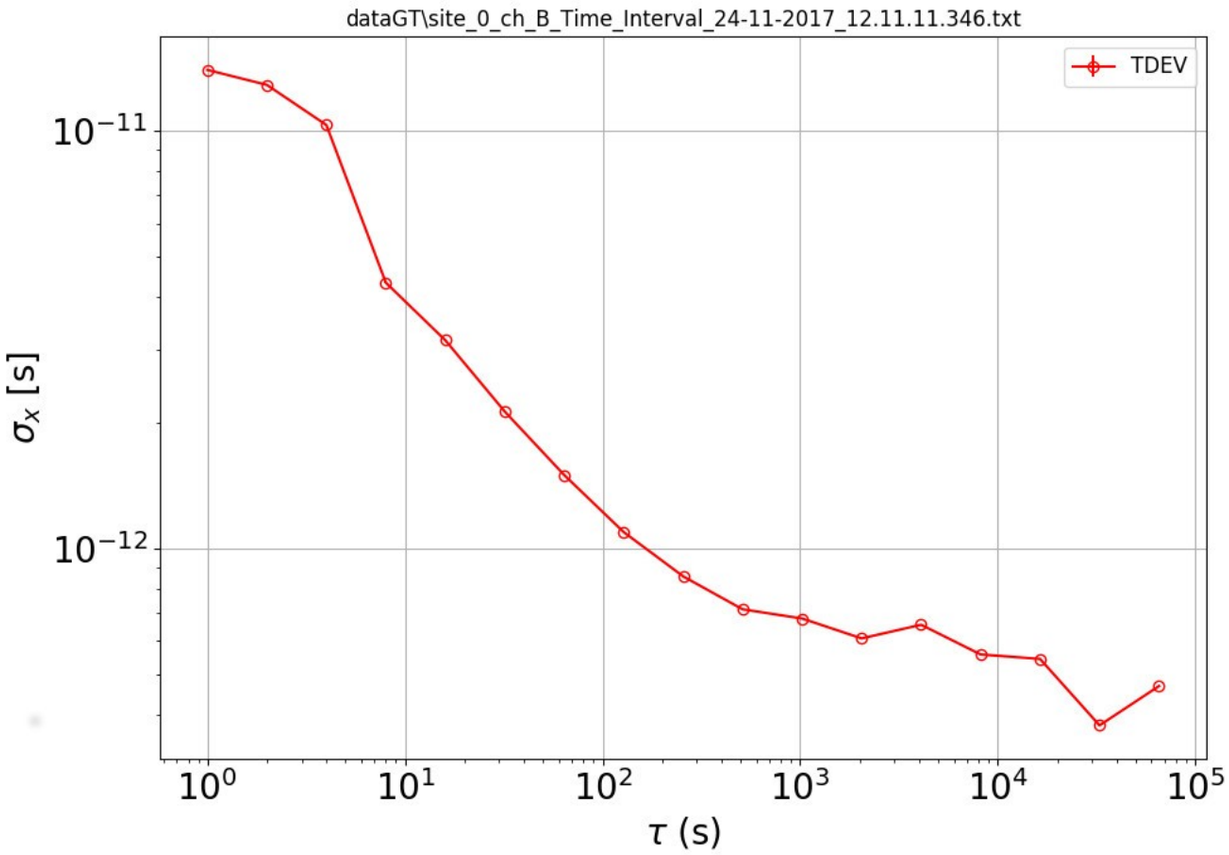
http://www.ohwr.org/projects/white-rabbit/wiki/WRReferenceDesign

WhiteRabbit, SYRTE test system



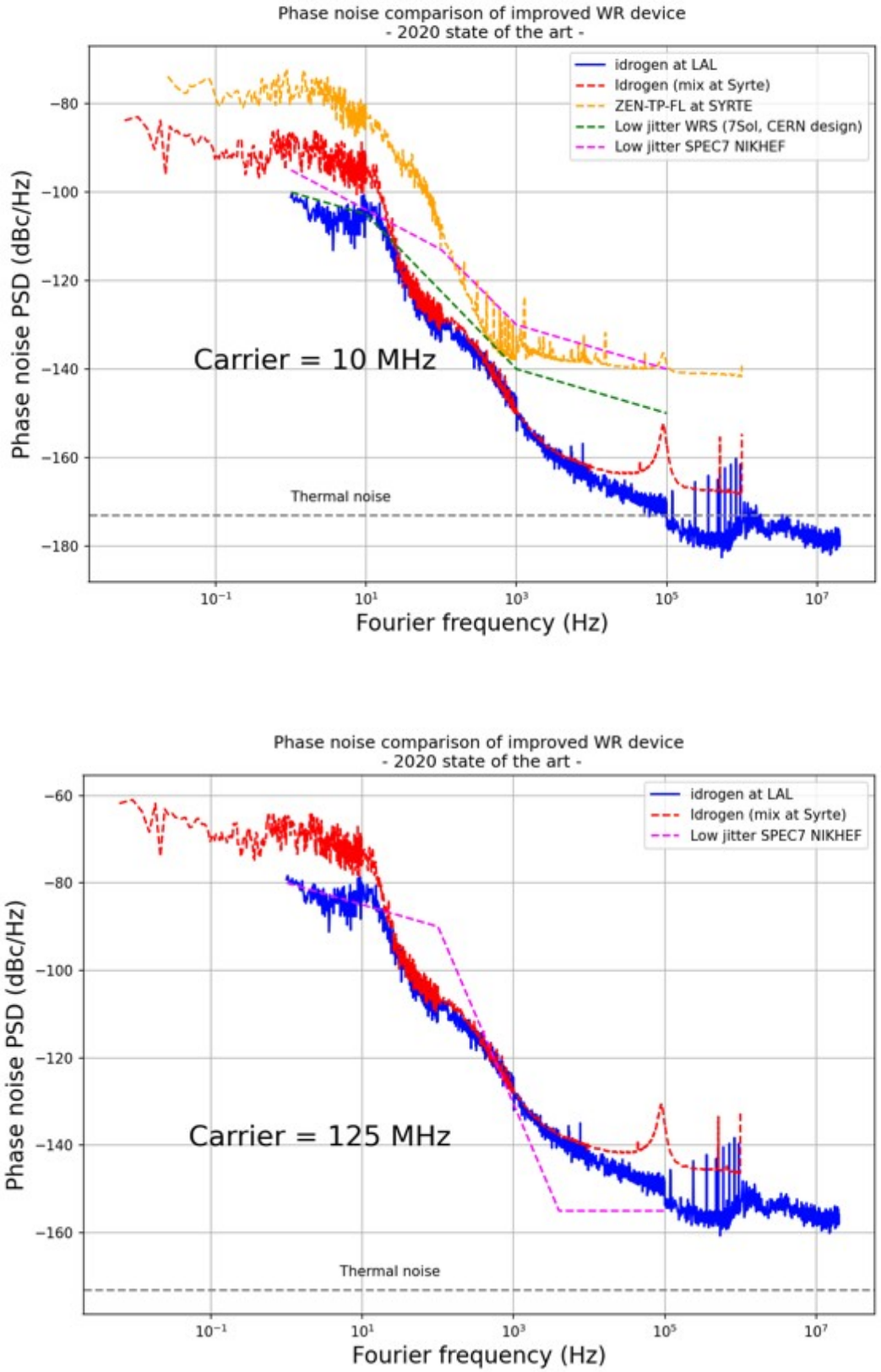
- For the test we use the test system developed by the SYRTE for timing distribution measurement.
  - fs measurement capability
  - Very high timing stability 10e-16
  - WR switch improvement.
    - Remove of local PLL
  - Conditioned room.
  - Dedicated measuring apparatus
  - Selection of fiber length
  - Selection of transceivers

NEBULA performance



- IDROGEN version -1
  - 400fs after 1000s & 1km of fibers
  - Same design as IDROGEN
  - IDROGEN system qualificationTest
    - With SYRTE test setup

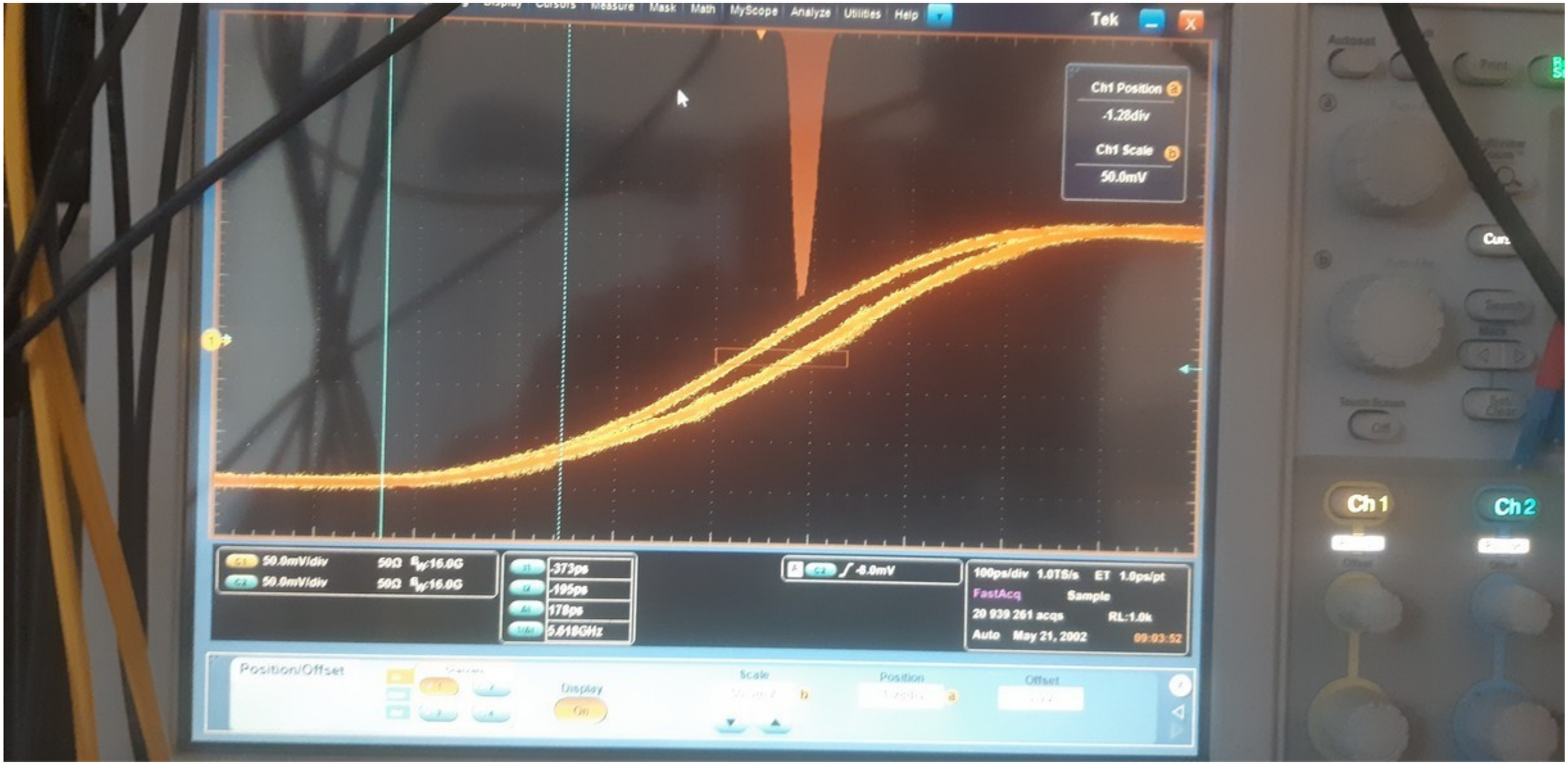
NEBULA performance



- Transfer from one WR switch to two IDROGEN with a short link (few meter)
- For the test we measure the phase difference between 2 nodes (IDROGEN board)
  - Best result, one order of magnitude than the « challenger »
  - Clock phase jitter
  - PPS time precision 1ps RMS

Pulse Per Second : IDROGEN

- PPS 2 IDROGEN board
- 25m & 125m of fiber
  - ~50ps of dispersion des PPS with calibration



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Firmware improvements

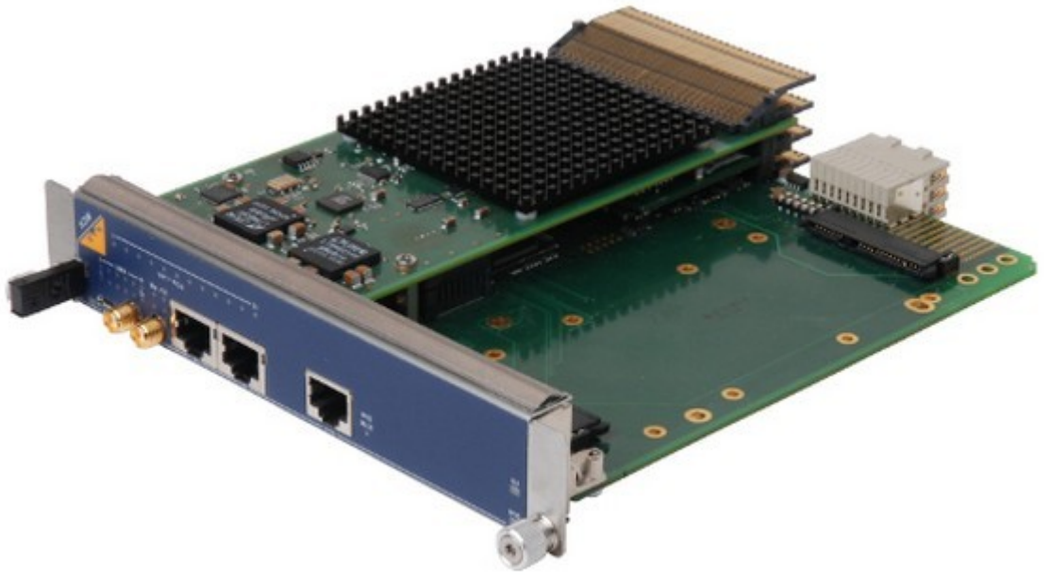
- Integration of IPBus and UDP streamer on WR link
  - One fiber : Synchro, configuration, data readout
- WR node status on integrated IPbus

Resarch and technology : TIMED

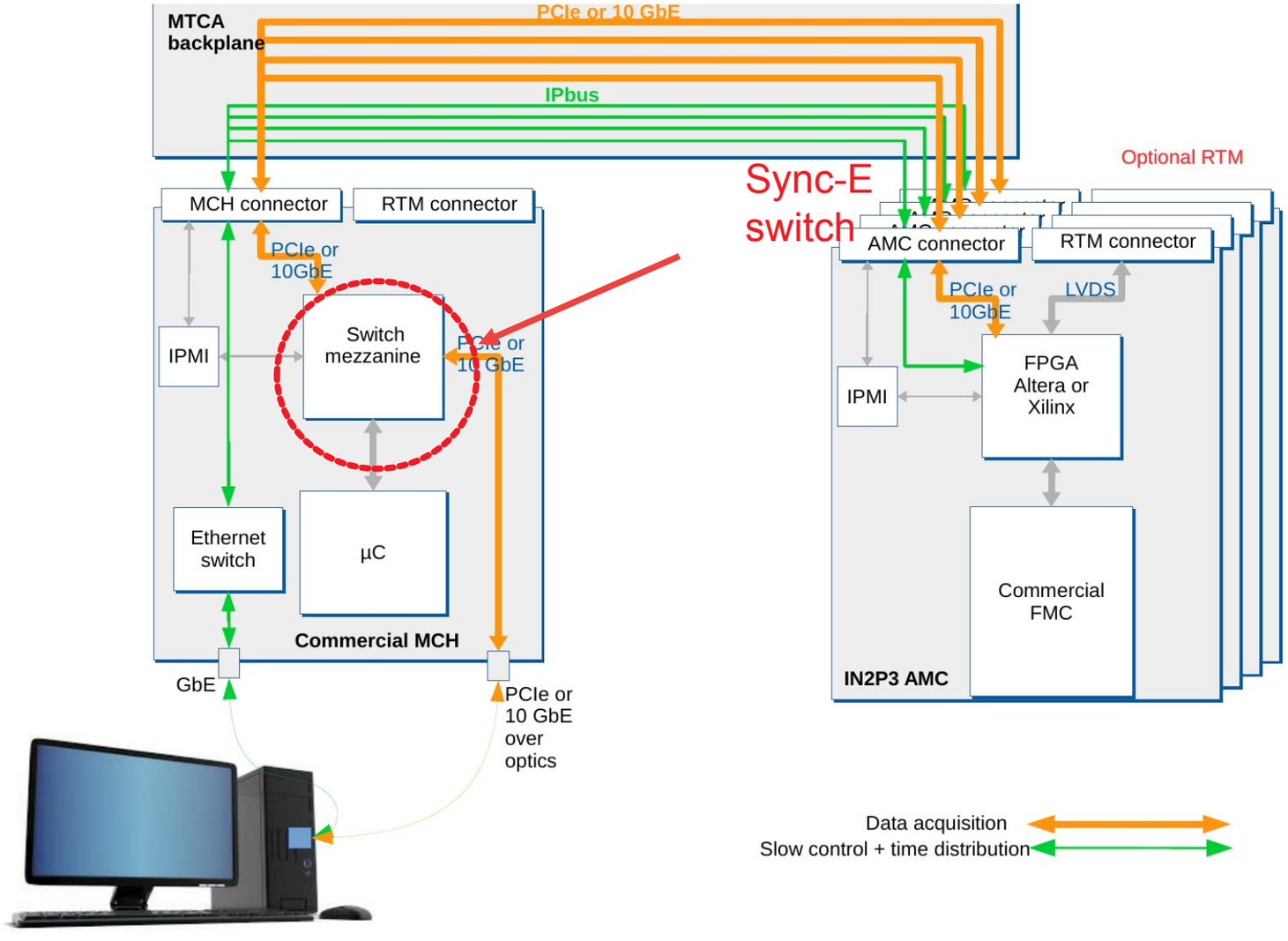
Rsearch & Technology : TIMED

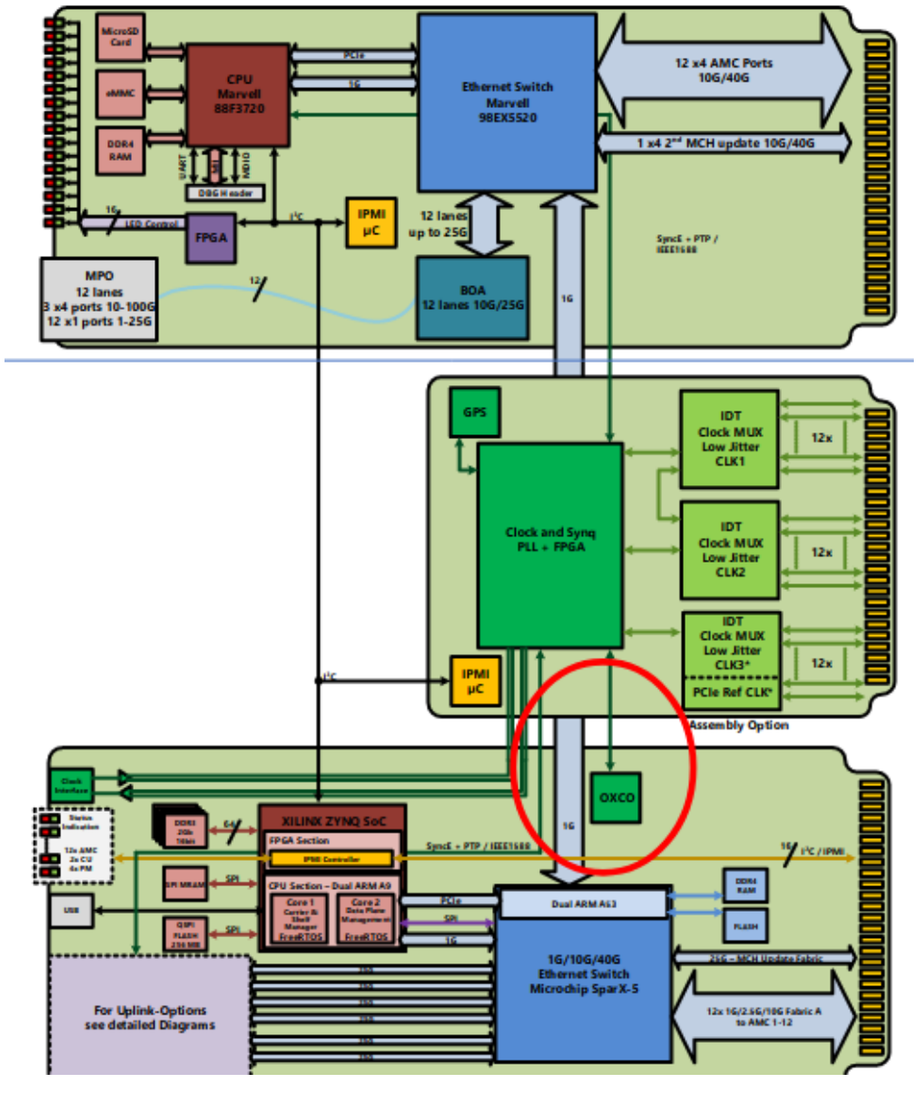
- Observatory of Paris & IN2P3 laboratories collaboration
- Extend domain of WhiteRabbit
- WhiteRabbit node simplification of technical integration
- Improvement of WR performance
- Integration of external components by firmware function
- High stability frequencies distribution

R & T TIMED 1 : WR Crate integration



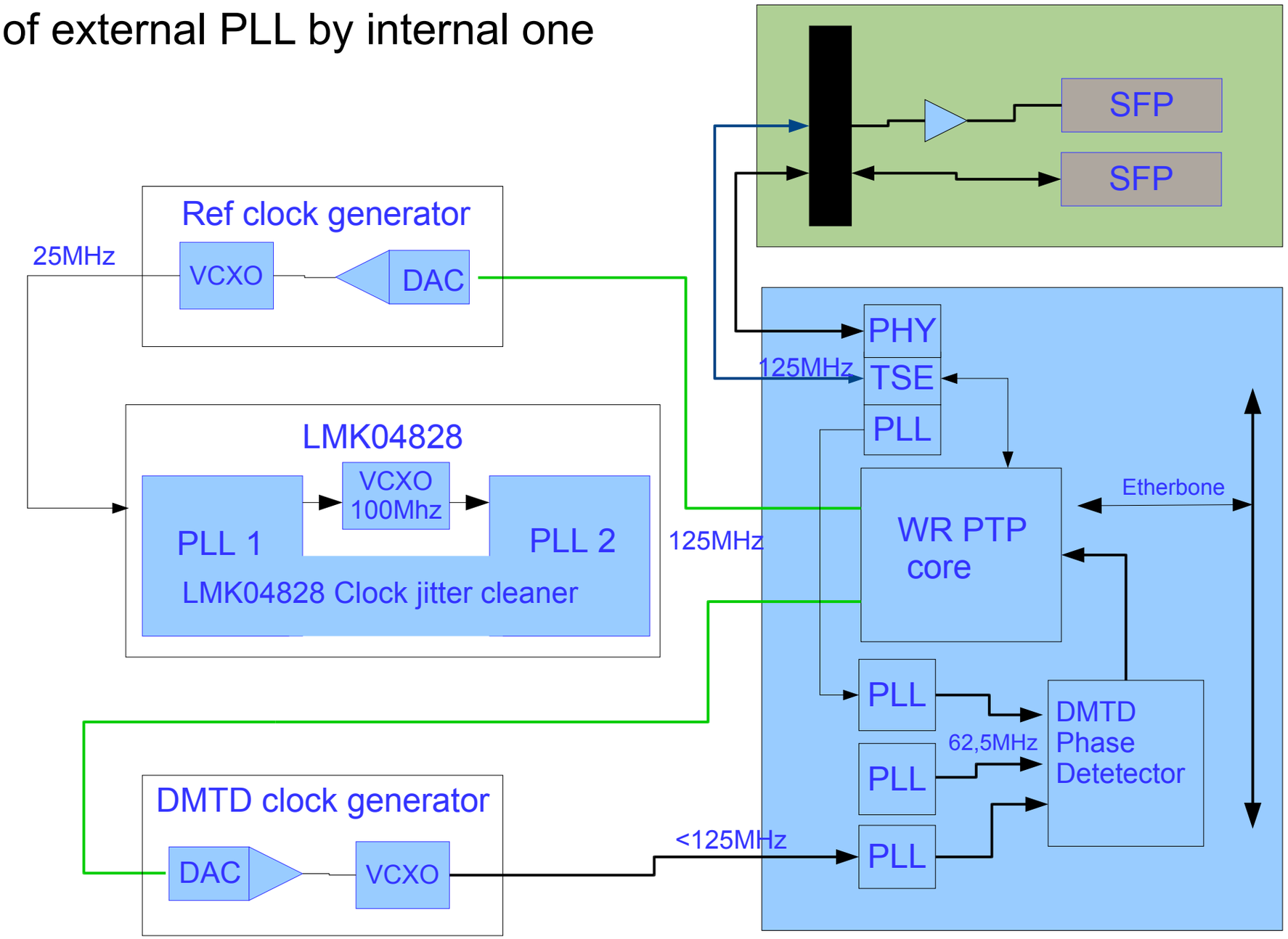
- WhiteRabbit on µTCA
  - Only switch functionality (no master)
  - WhiteRabbit on copper link
  - Sync-E function on MCH board
  - NAT-MCH-4
    - IEEE1588V2 compliant switch



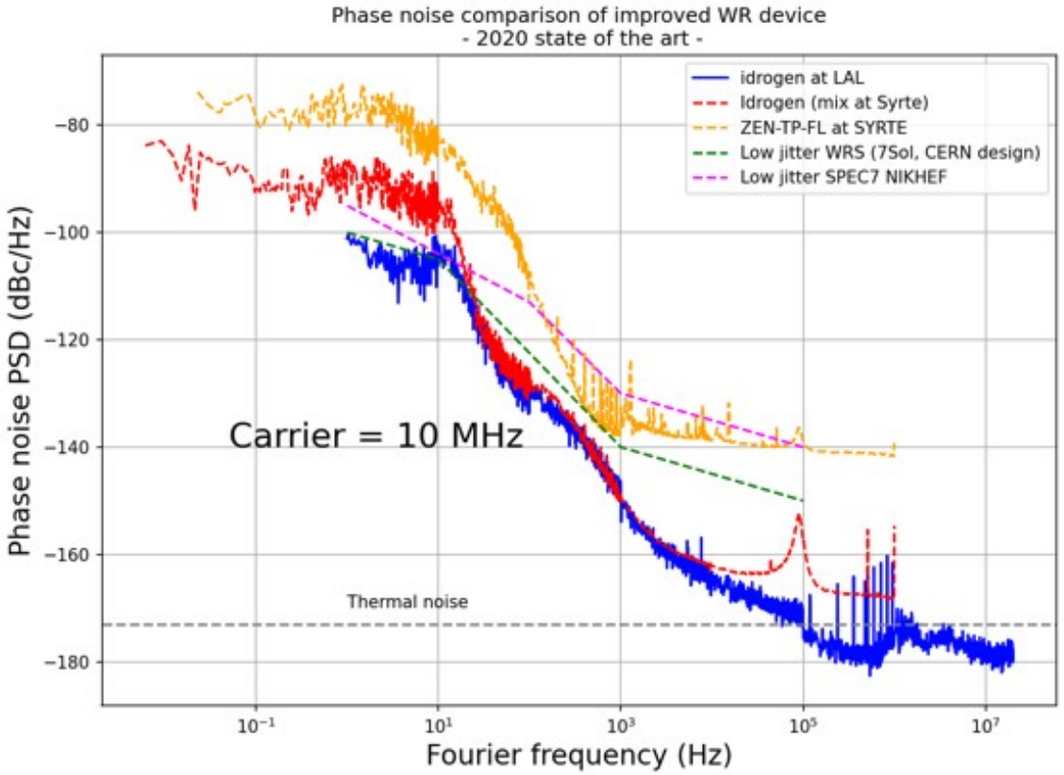


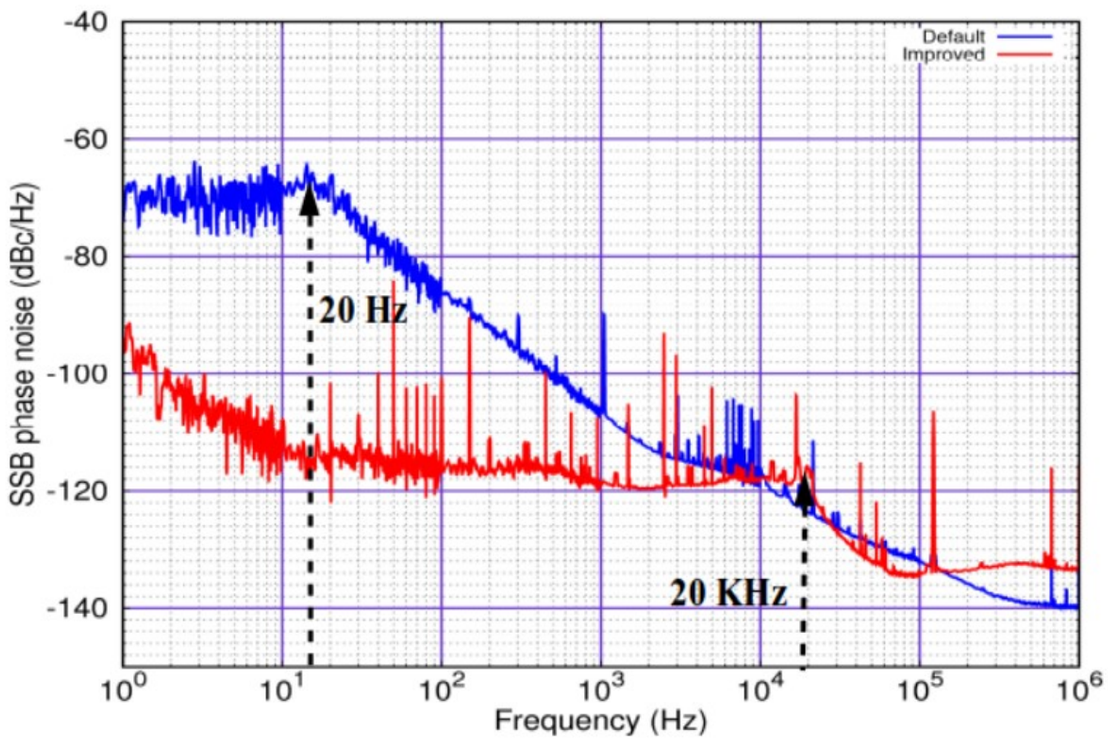
R & T IMED 2 : Simplification of WR integration

- Replacement of GXB by DDR I/O (up to 800MHz capability)
  - IP Native-PHY by IP TSE Pcs only
  - Integrated PHY functionality replaced by RTL code
- Integration of external PLL by internal one



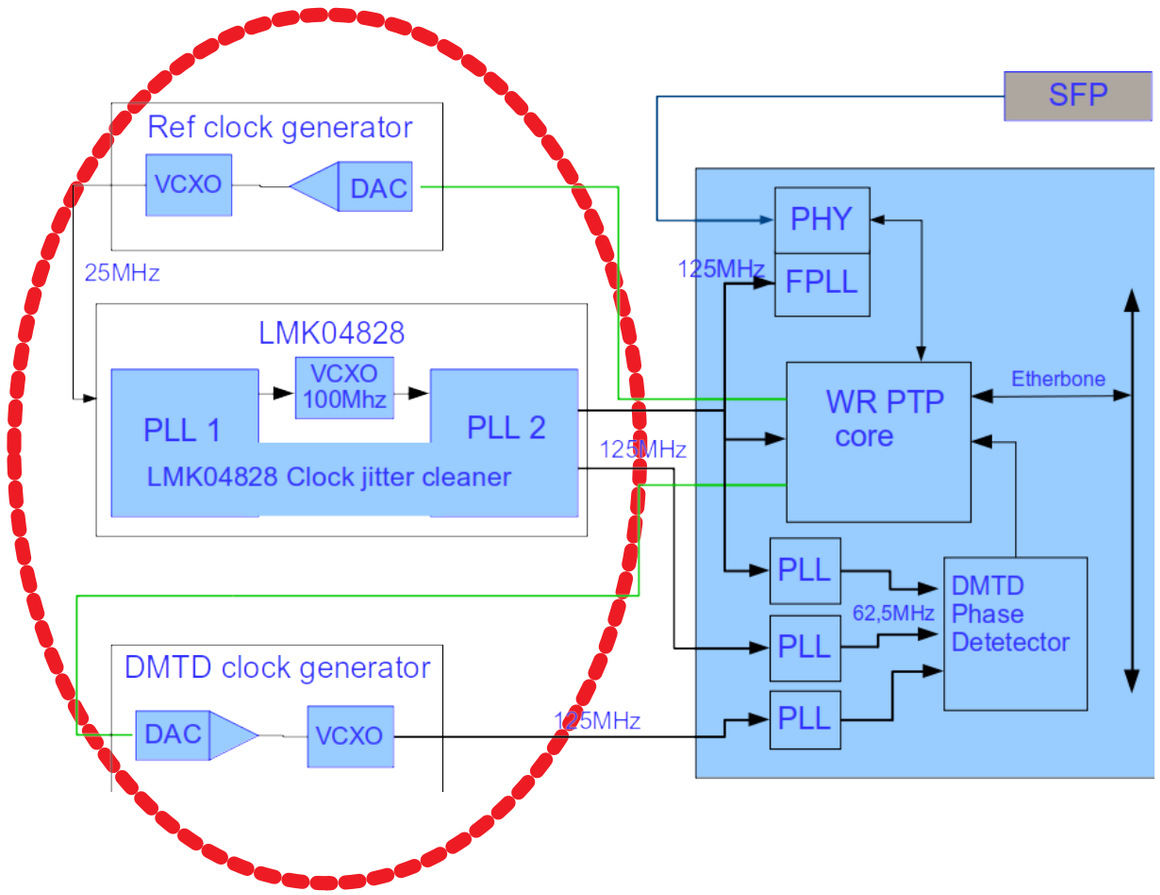
R & T TIMED 3 : Increasing performances





- Collaboration with Paris Observatory Laboratory
- Soft PLL modification
  - Decrease the response time of software PLL
  - µP upgrading :Replacement of the universal µP based on logic bloc by dedicated µP (NIOS) or hardware µP (SOC)
  - Gain integrator optimization
- Increased PLL bandwith of the GM Local oscillator
- Components upgrading
  - VCXO selection
  - Increase Frequency (reduce PLL number)

R & T TIMED 4 : Firmware integration



- External PLL integration
  - Internal reconfiguration
  - µP Software upgrade
- VCXO intégration
  - Derived from video IP
- FPGA manufacturer dependent

Application Note: 7 Series FPGAs and Zynq-7000 AP SoCs

XILINX
ALL PROGRAMMABLE

XAPP589 (v2.3) April 29, 2015

All Digital VCXO Replacement for Gigabit Transceiver Applications (7 Series/Zynq-7000)

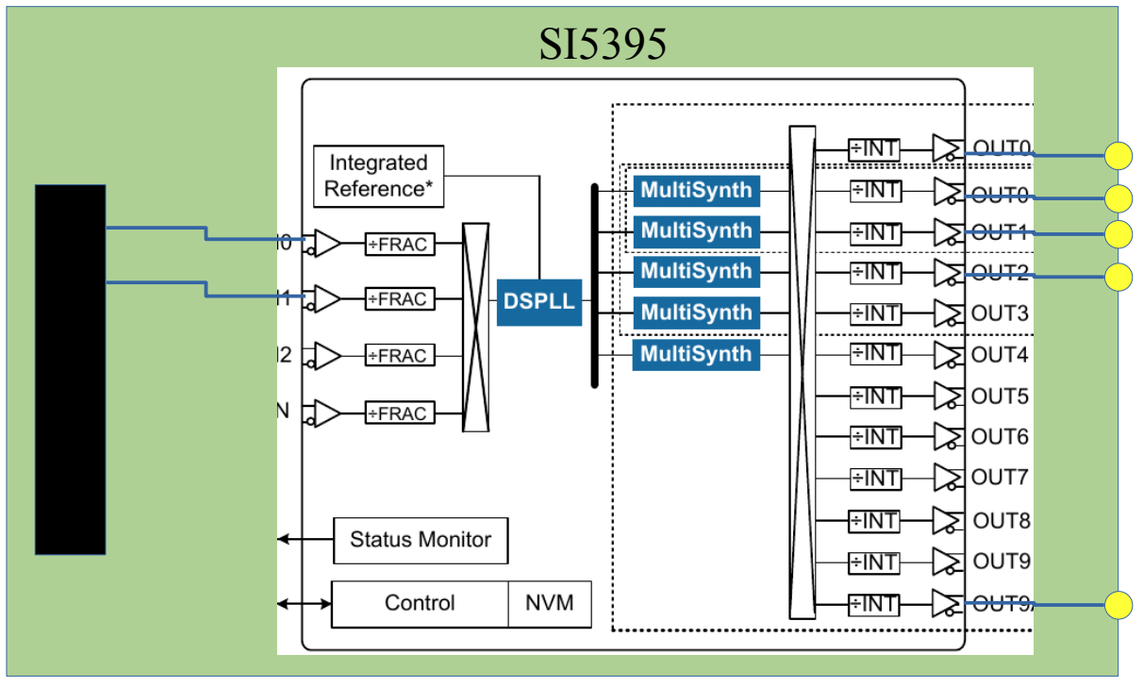
Authors: David Taylor, Matt Klein, and Vincent Vendramini

Summary

This application note delivers a system that is designed to replace external voltage-controlled crystal oscillator (VCXO) circuits by utilizing functionality within each serial gigabit transceiver.

Note: In this application note, *transceiver* refers to these types of transceivers:

R & T TIMED 5 : High stability frequency distribution

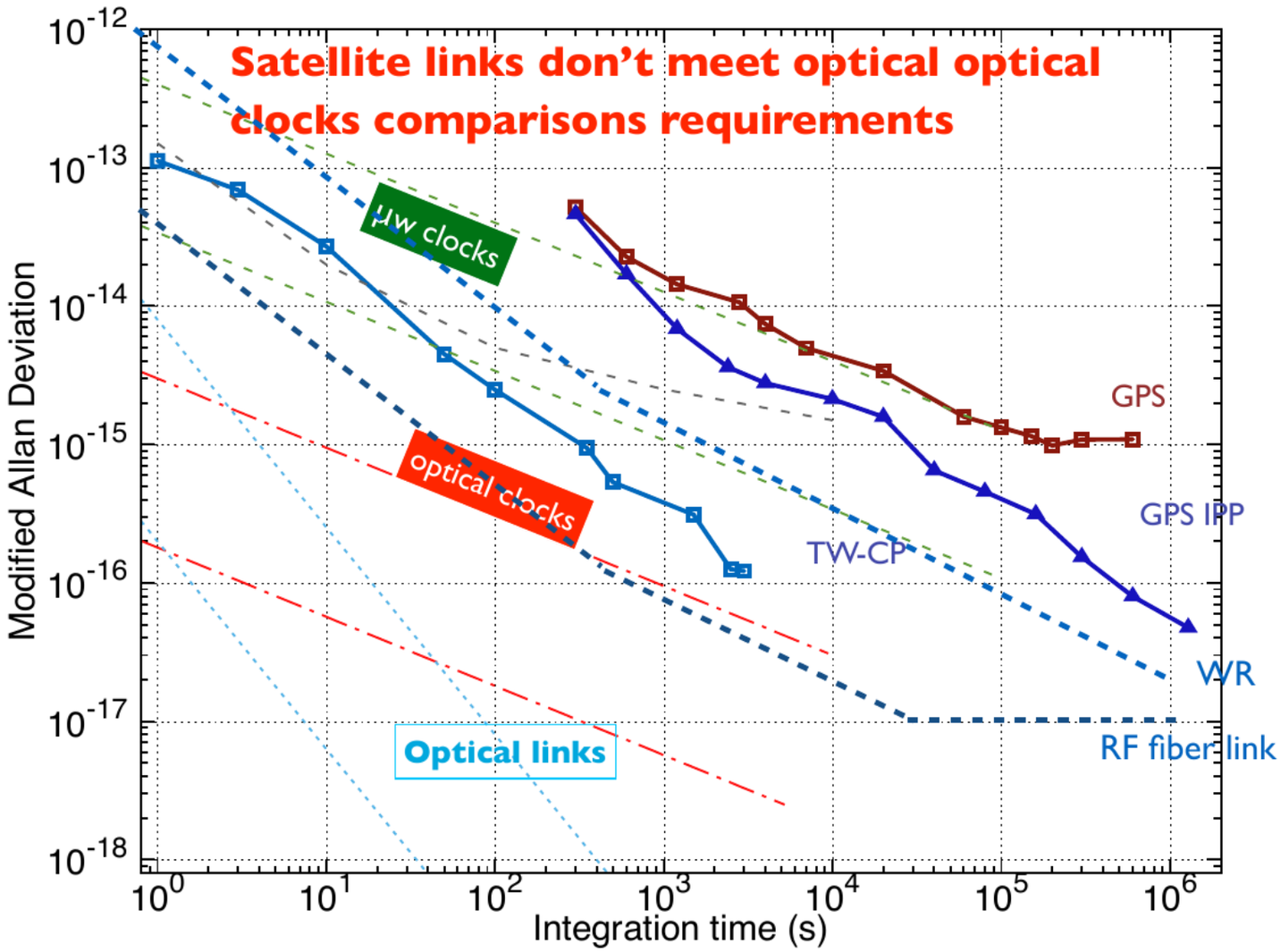


- Implementation of a synthesizer on mezzanine FMC : SI5395
- Collaboration with accelerator department
- Design mid 2023
  - Phase jitter 90 fs
  - Frequency : 1kHz < F < 1GHz
  - RF filter : outside

Systèmes de Référence Temps-Espace

T+RFIMEVE

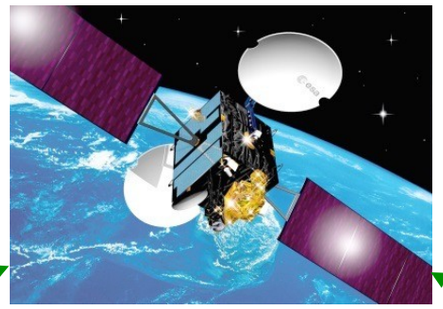
Overview of comparison methods



WitteRabbit	Stabilité 1s	Stabilité 1j
LAN with commercial hardware	1e-11	1e-13
National network RENATER	1e-12	1e-15
Development IJCLAB	1e-13	1e-16

Problematic : comparison method/ dissemination

Satellite Link
10^{-11}(1s)
$2x10^{-16}$(1d)



Optical Fiber Link

NMI A

Atomic clock 1

in Europe
800< distance <1500 km

NMI B

Atomic clock 2

Stability(1s) <10^{-13}
Accuracy <10^{-16}

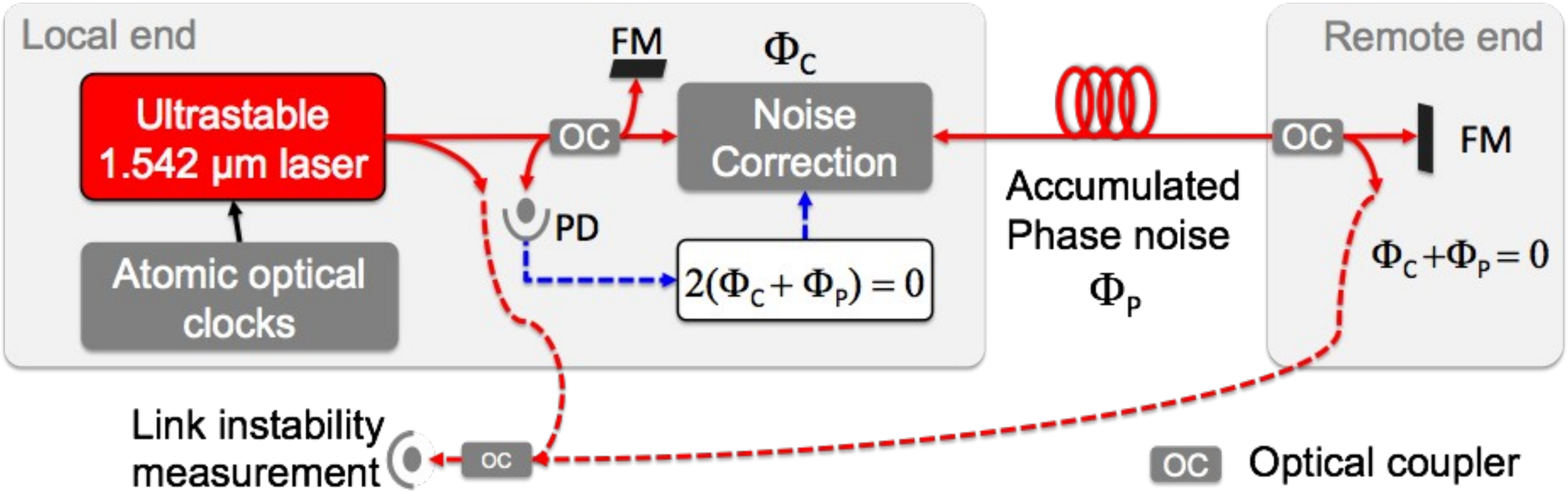
Transportable clock (FOM)
10^{-13}(1s)
$4x10^{-16}$(1d)

l'Observatoire de Paris — SYRTE
Systèmes de Référence Temps-Espace

Station de Radioastronomie de Nançay

Optical fibers links : global concept

- Seminal works: Primas et al, Proc 20th PTTI, 1988, Ma et al., OL 1994
- Active noise compensation after one round-trip
- Strong hypothesis : noises forth and back are the same
- 2 ends at the same place (for link stability measurement)



Example method for « all optic system »

The requirements of the dissemination of T/F by fiber

Laboratoire de Physique des 2 infinis Irène Joliot-Curie

Frequency metrology:

Access to ultra precise reference frequencies for remote user.

Spectroscopy, photonics, quantum sensors, quantum telecom., …

Applied dimensional measurements:

Traceability of the unit of length for interferometric measurements.

Astronomy:

Phase traceable signals for the synchronization of radio telescopes

VLBI, NOEMA, SKA, LOFAR …

Broadband communication technology:

Provision of reference signals with low-jitter for synchronization

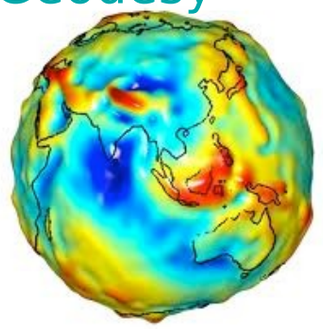
Large research infrastructures

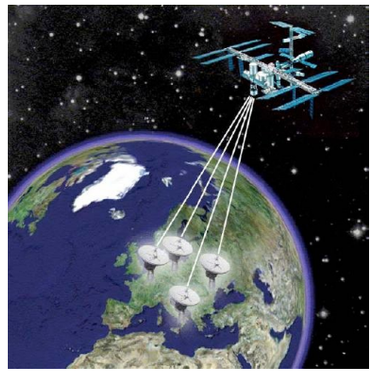
(ESA, DESY, CERN, GSI):

Time and frequency dissemination in ground stations

Industry : wireless, optical telecom. Galileo GNSS ground segment

Geodesy





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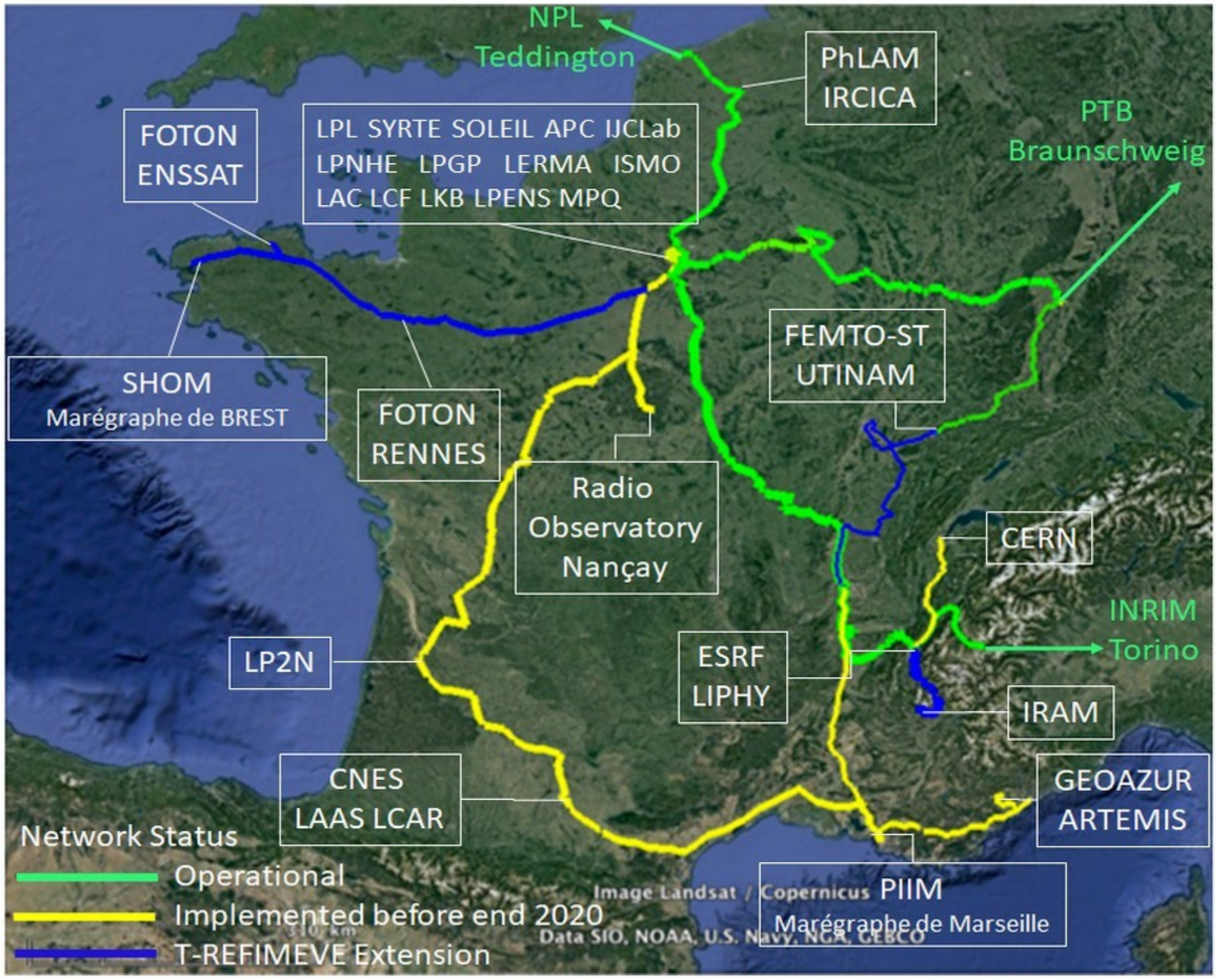
Systèmes de Référence Temps-Espace

Station de Radioastronomie de Nançay

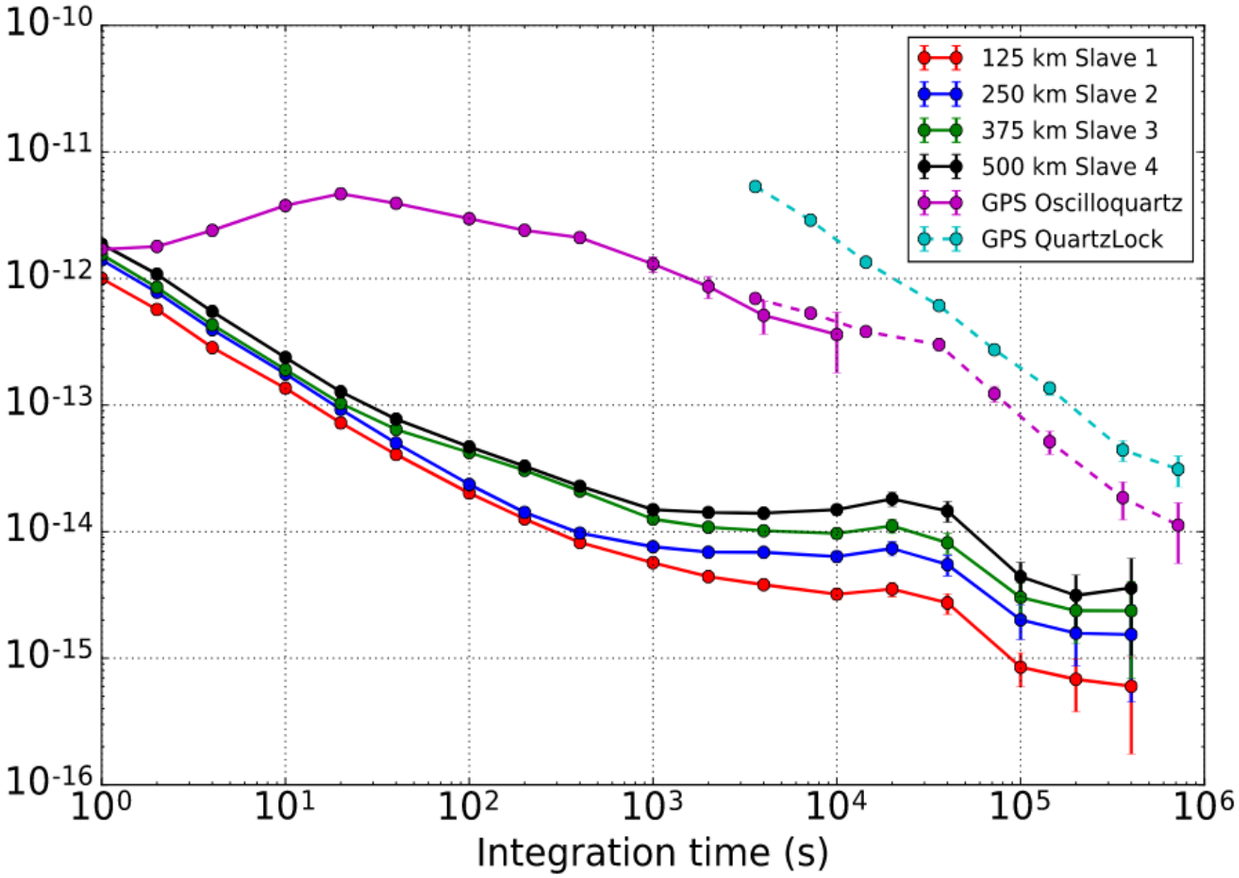
Map of REFIMEVE netwok



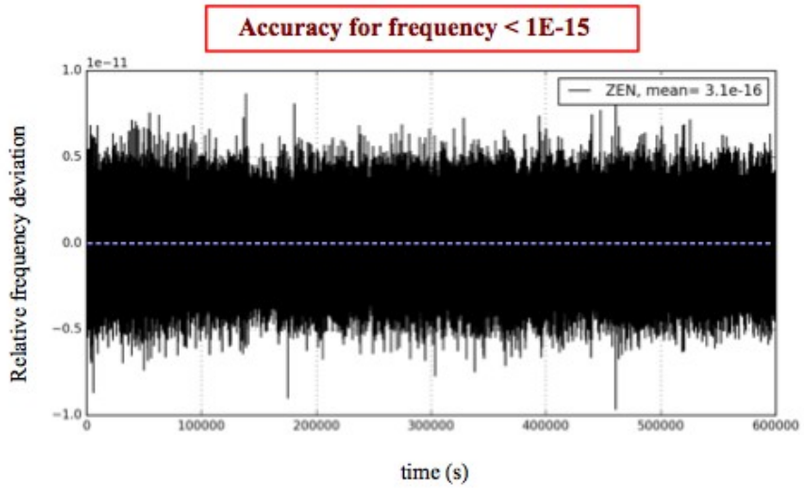
Distributed signals on REFIMEVE netwok

Signal provided by T-REFIMEVE		Stability @1s	Stability @1day	Uncertainty	
				routine	dedicated
Radiofrequency	1st pillar - 10 MHz (White Rabbit)	10^{-12}	10^{-15}	10^{-14}	10^{-15}
	2nd pillar - 1 GHz	10^{-13}	3×10^{-16}	10^{-14}	2×10^{-16}
Time	1st pillar (White Rabbit)	1 ns	1 ns	10 ns	10 ns
	2nd pillar	20-50 ps	500 ps	10 ns	2ns to 100ps
Optical frequency (194,5 THz - 1542 nm)	Today	10^{-15}	3×10^{-16}	10^{-14}	2×10^{-17}
	Expected progress in 5 years	10^{-16}	2×10^{-17}	10^{-14}	10^{-18}

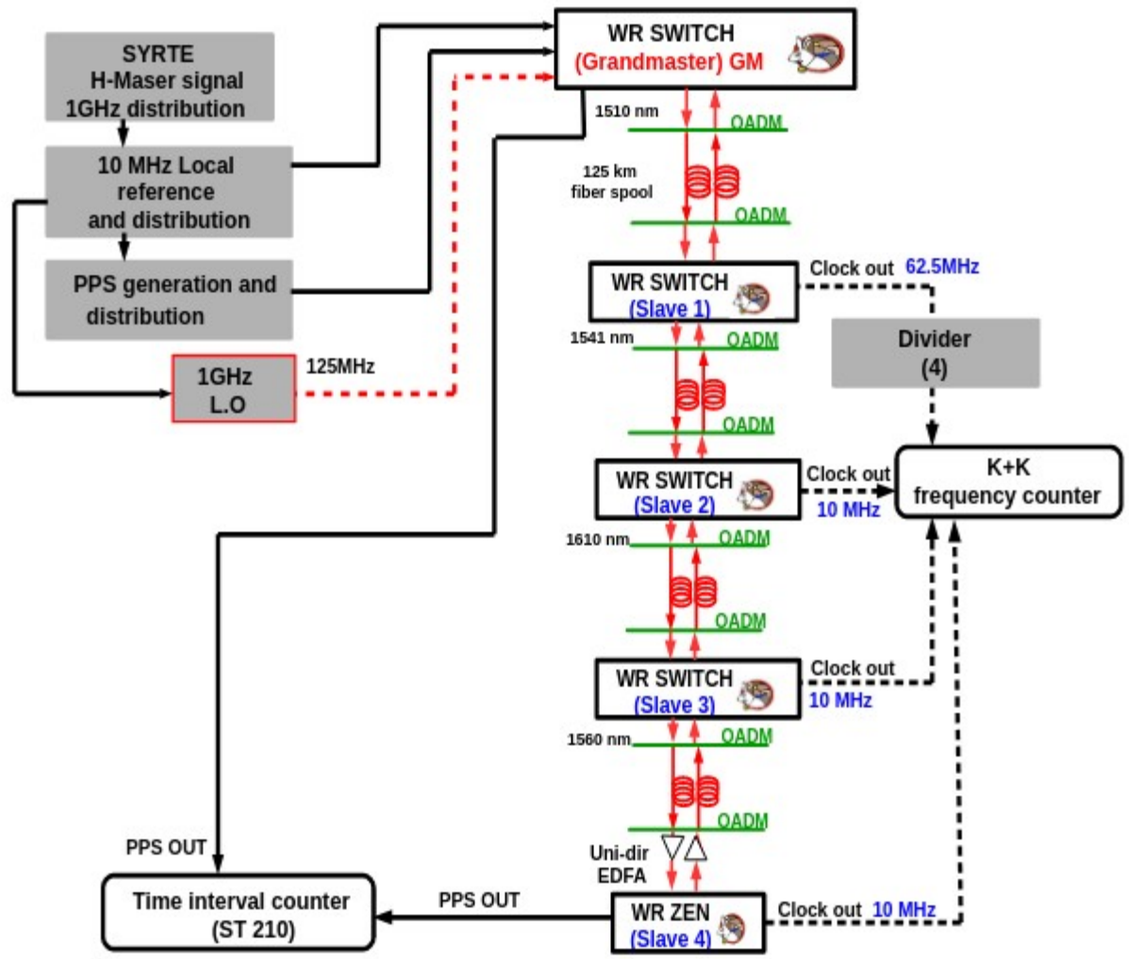
WR performance on long distance test



- 4 span Cascaded
- Better than Oscilloquartz GPS receiver
  - 500Km (4 x 125Km) of fiber
  - Uni-dir fiber
  - 2 OADM (multi wavelength)
- Fiber noise become dominant with the length
  - System disparity, reciprocity of the link



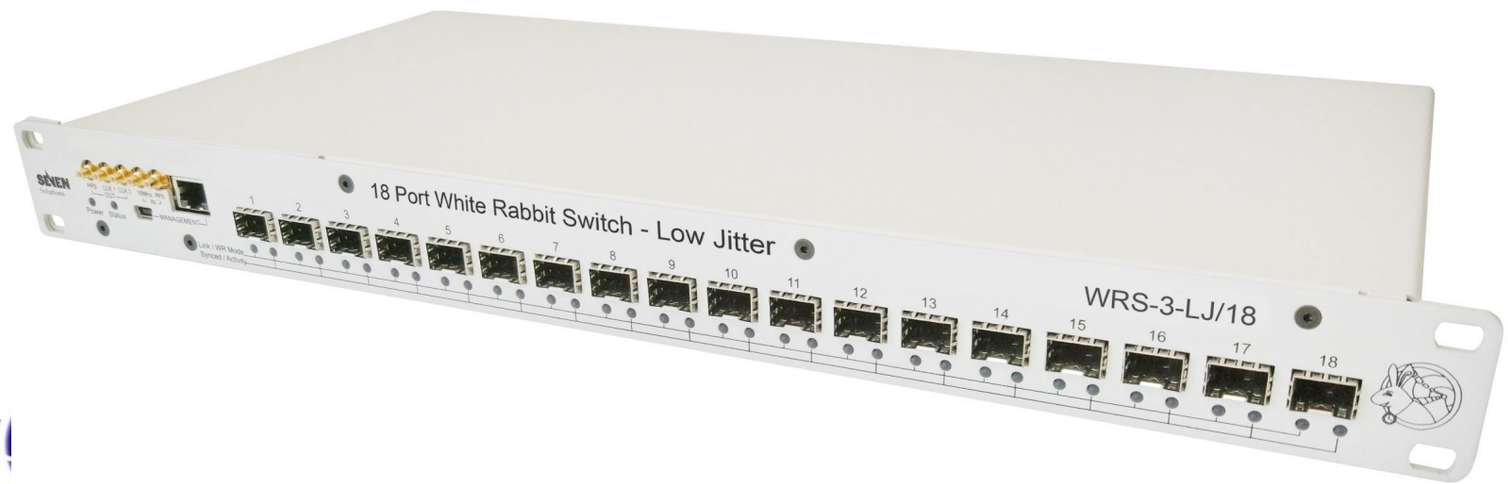
Λ gate time = 1s



Systèmes de Référence Temps-Espace

Tests facilities at IJCLab

- WR switch
  - Low jitter WRS-3-LJ/18
  - WRS-3/18
- Scope
  - 100G samples 17GHz of bandwith
- T+REFIMEVE node at the laboratory
- Phase meter
- IDROGEN board



WR Conclusion

- The WR is a very efficient system to distribute high stability frequency and very precise time stamping
- It is currently being standardized by IEEE (1588-V2)
- The WR allows to distribute very precise time on distance up to 1000km
  - Time stamping for long base line radio-telescope
  - Multi-messenger physics
- On the shelf system
- We will extend the area of use of the WR : R&T TIMED (implementation,stability,...)
- The WR allows the conception of new system architecture.
  - Ex : distributed high-frequency coding system for radio astronomy detector (PAON IV detector)
- The future of WR will be the upgrade to 10G
  - Ongoing development

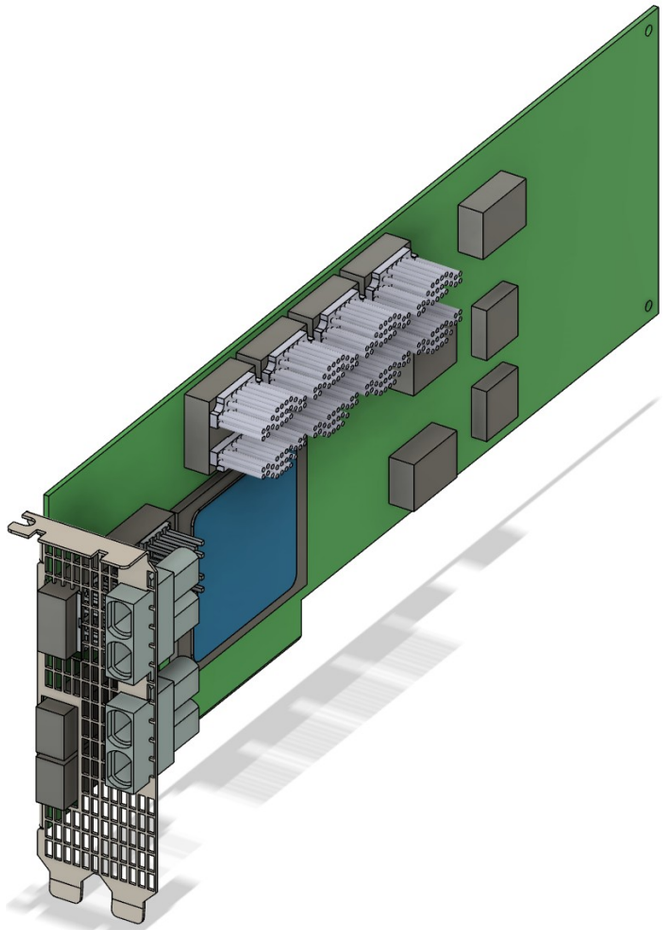
PCIe400 : Development status

Daniel Charlet on behalf of the R&T PCIe400 team
CPPM, IJClab, IP2I, LAPP, LPCC, CERN (LHCb Online)

PCIe400

Foreseen characteristics

- Agilex7 M-series AGMF039R47A1E2V
- No DDR memory
  Use of PC RAM or HBM2e instead
- Up to 48x26Gbps NRZ for FE
- PCIe Gen 5 / CXL or 400GbE
- Low jitter PLL < 100 fs RMS
- White Rabbit clock distribution (1ps) (SFP+)
- PON interface for fast control (SFP+)



Systèmes de Référence Temps-Espace

FPGA resource comparaison

Early Access program granted by Intel

New FPGA ressources

- Serial links up to 112Gb/s
- HBM / NoC (Network on Chip)
  - Facilitate high-bandwidth data movement between core logic and HBM
    - Deep learning acceleration
    - smartNIC to accelerate and offload certain functions from the server

Foreseen gain (compared to PCIe40)

- Processing : factor 8 to 12

	PCIe40	PCIe400
Family	Arria 10	Agilex7 M-series
Logic elements	1.2 M	3.9 M
DSP	1.5 K	12 K
Frequency (silicon max)	650MHz	1GHz
HBM2e	-	32GB
Hard co-processor	-	Arm Cortex A53 MPCore
Package	2000 pins	4500 pins

Planning

	2022				2023				2024			
Task	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Design												
Placing & Routing												
Manufacturing												
Definition unitary tests												
Implementation of unitary tests												
Prototype Debug												
Qualification & Characterization												

Prototype available July **2023**

Routing review internal and Intel **March 2023**

Schematics review internal and Intel **January 2023**

- Important design effort on power estimation and thermal simulations
- As of today, schematics are done

Synthesis

IN2P3 R&D

- Project set up to develop the prototype of PCIe40 next generation
- Design a generic readout DAQ for muti context use
- Interest from several collaborations (LHCb, Alice and CTA)
- Funded for 3 years from 2022 to end of 2024

Technical challenges to tackle

- Power distribution >100A for FPGA core in a 18 layers PCB
- Cooling solution for FPGA and optical transceivers
- High speed serial interface routing up to 112Gb/s
- Network interface on board through 400GbE (experimental)
- Use of on-Chip ressources to embed neural network for processing acceleration

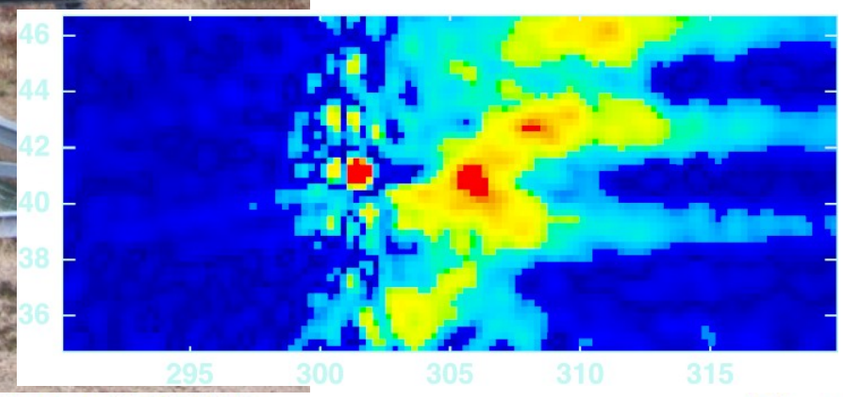
Project follow up

- Discussions with IN2P3 are on-going to envisage a production at the horizon of 2026-2028

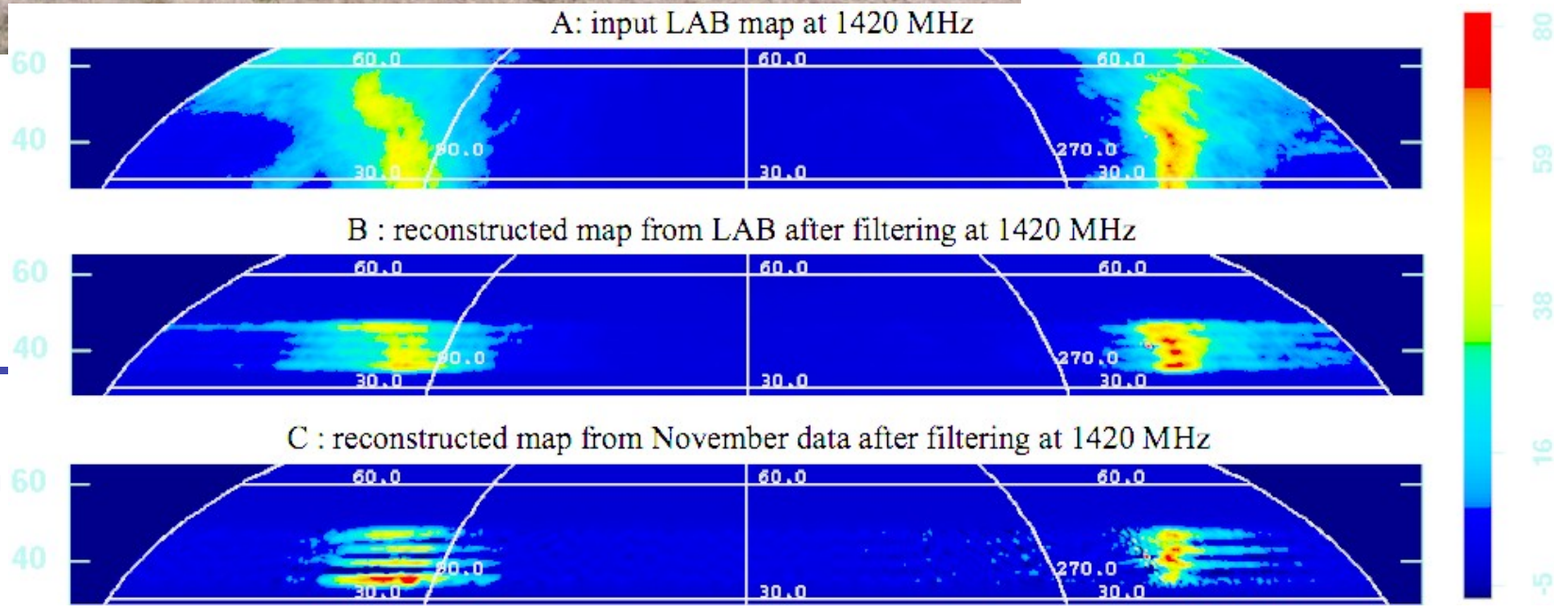
Backup

PAON IV

PAON IV



Reconstructed map at 1420.4 MHz
from PAON-4 Nov.2016 observations



Laboratoire de Physique des 2 infinis Irène Joliot-Curie

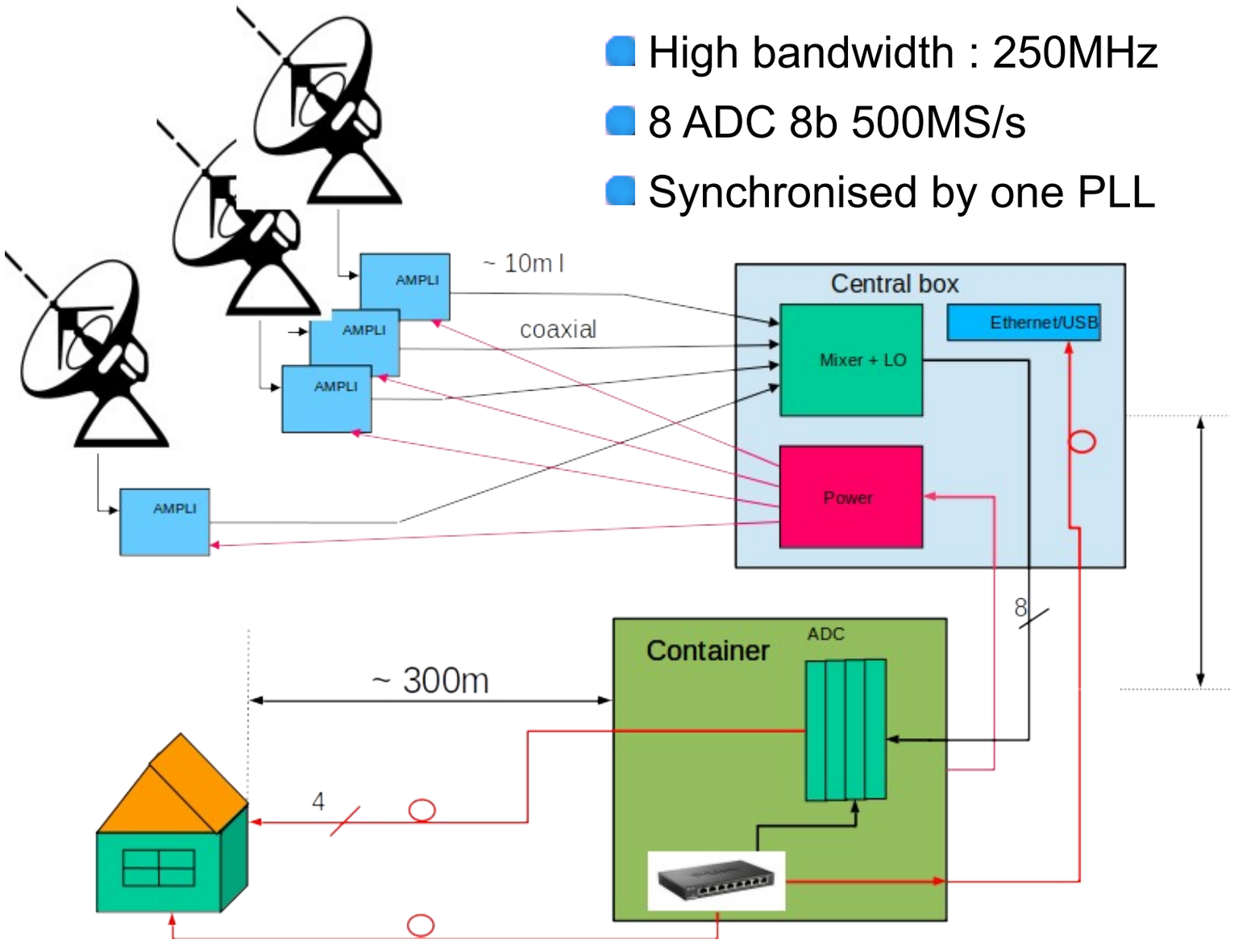
l'Observatoire de Paris — SYRTE

Systèmes de Référence Temps-Espace

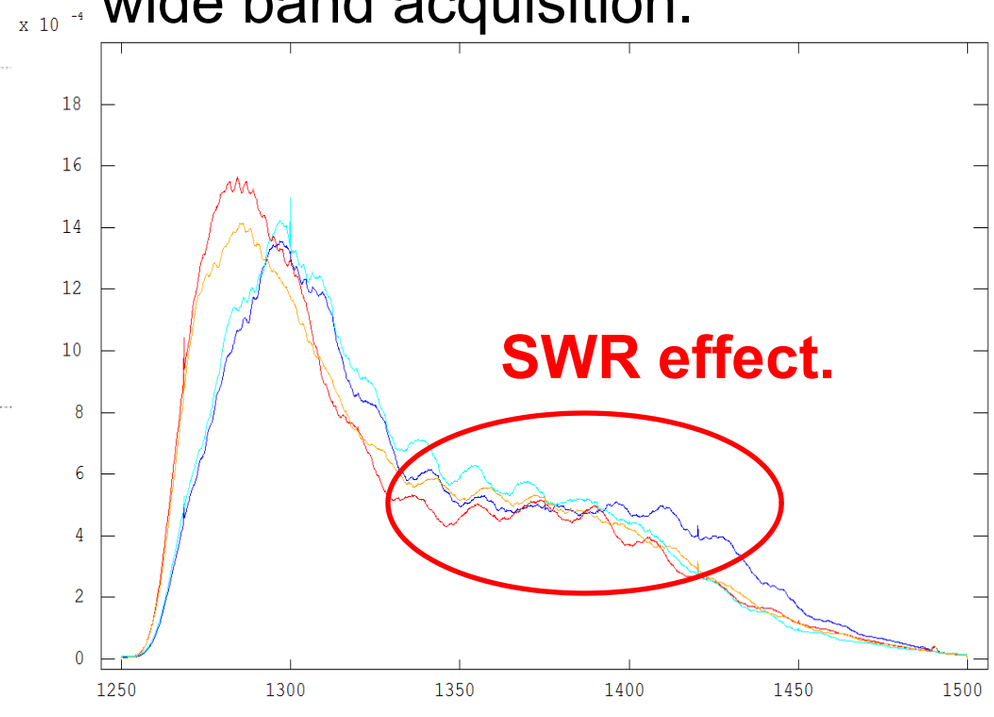
B 2 G

PAON IV : Current configuration

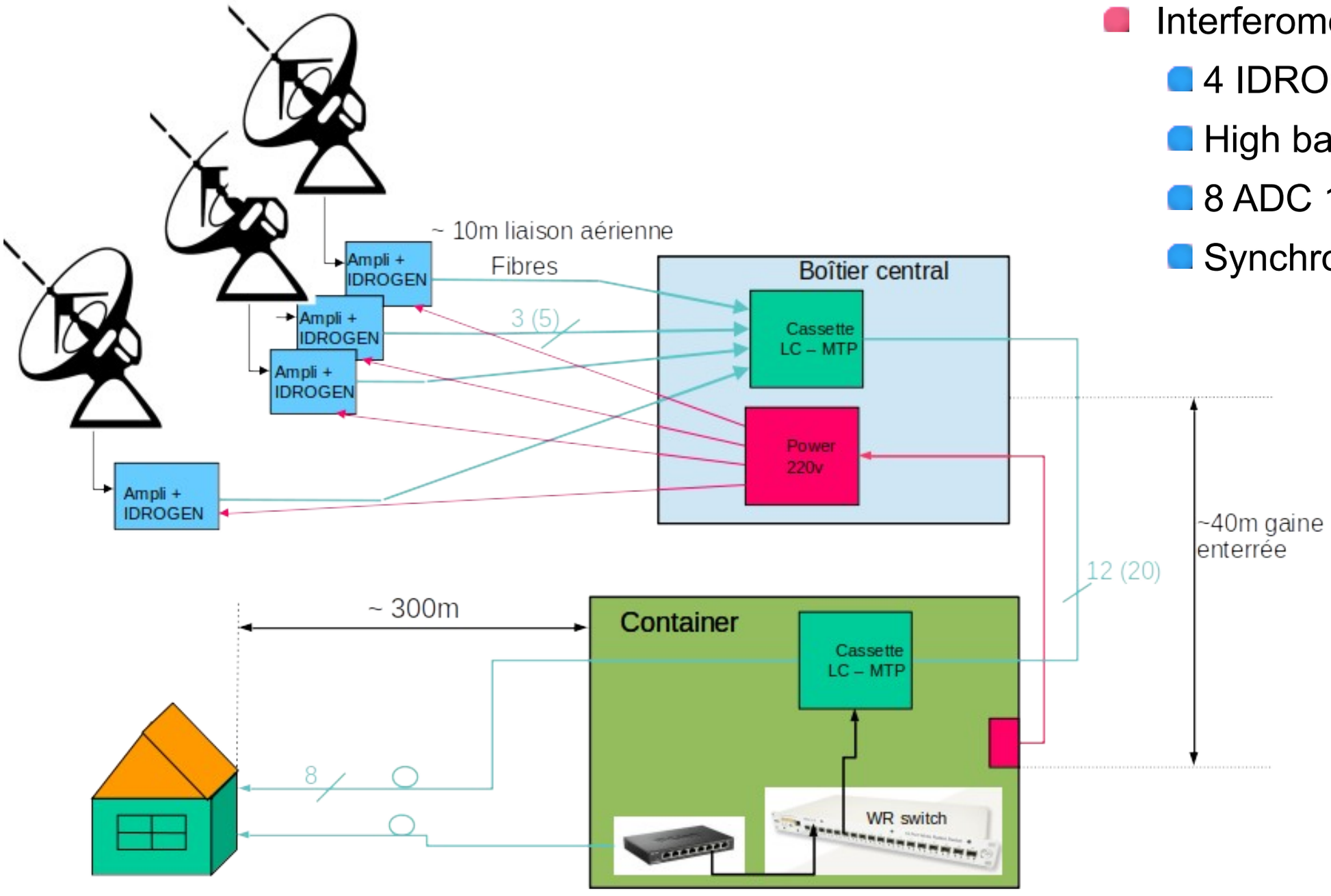
- Interferometer 4 radio dish of 5m
  - 4 IDROGEN board
  - High bandwidth : 250MHz
  - 8 ADC 8b 500MS/s
  - Synchronised by one PLL



SWR depends of:
long RF cables,
adaptation mismatch,
wide band acquisition.



PAON IV : Future configuration



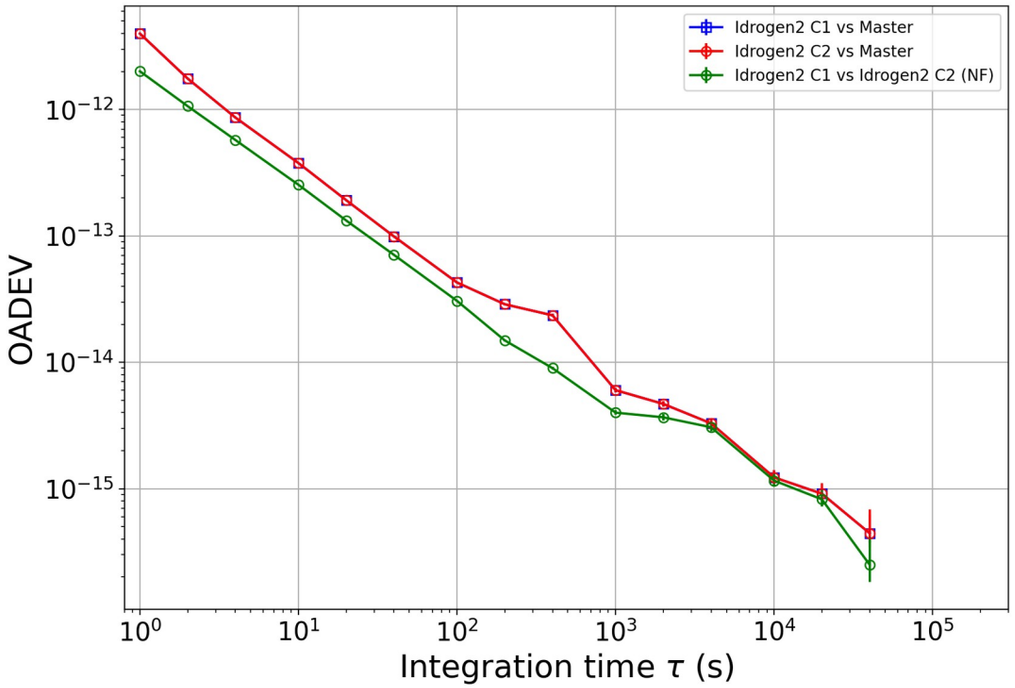
- Interferometer 4 radio dish of 5m
  - 4 IDROGEN board
  - High bandwidth : 500MHz
  - 8 ADC 14b 1GS/s
  - Synchronised by WR

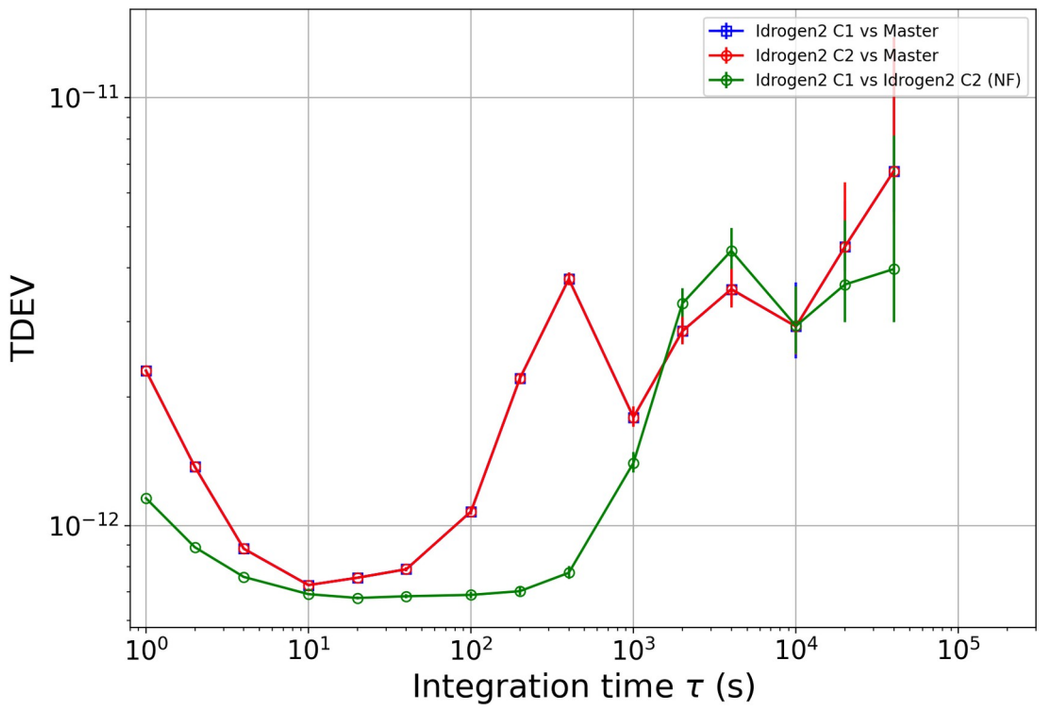
IDROGEN + mezzanine ADC

- Bandwidth 500 MHz à 1.5GHz
- Syncro & timing by WR
- Data transfer 2x 10G eth
- Configuration by IPBus 10G

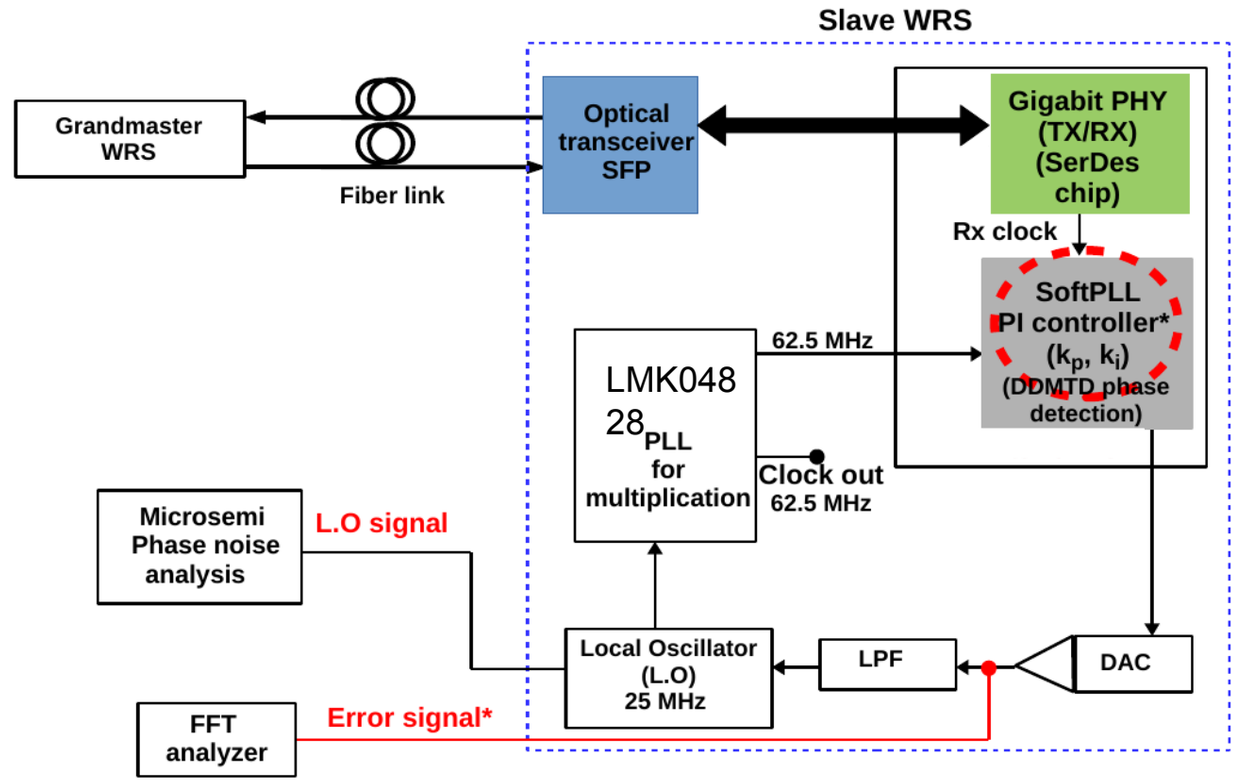
Backup

IDROGEN preliminary measurements





- For the test we measure the phase difference between 2 nodes (IDROGEN board)
  -



Fibers comparaison

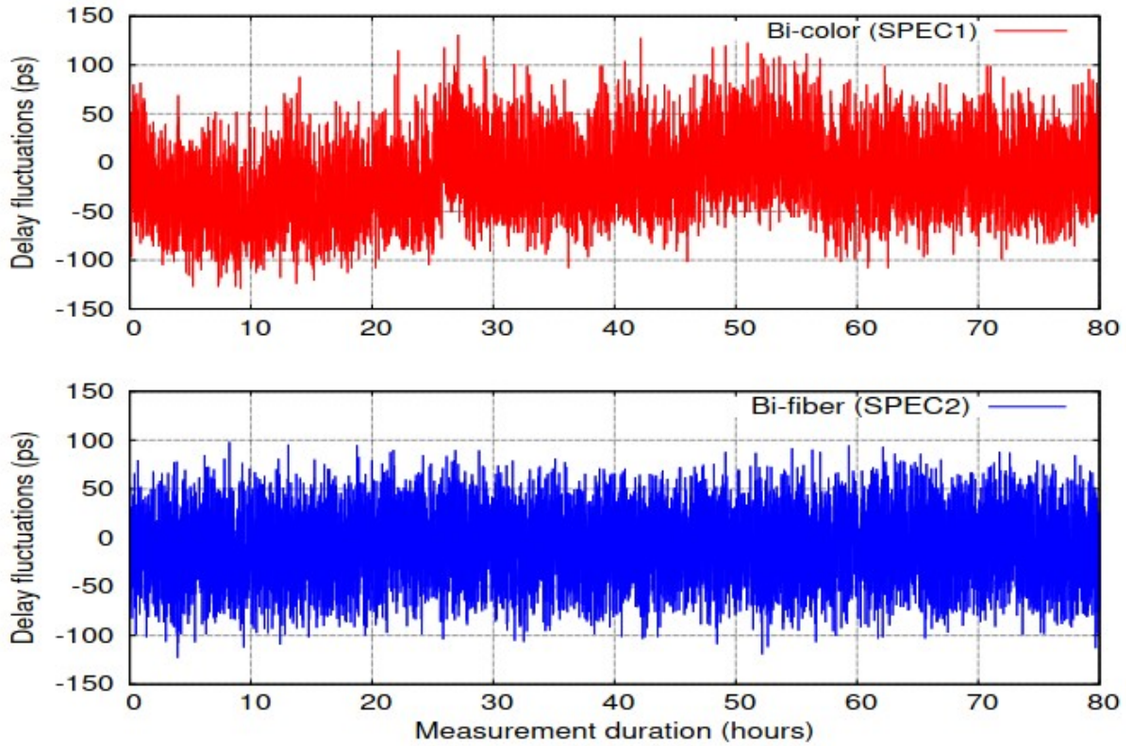
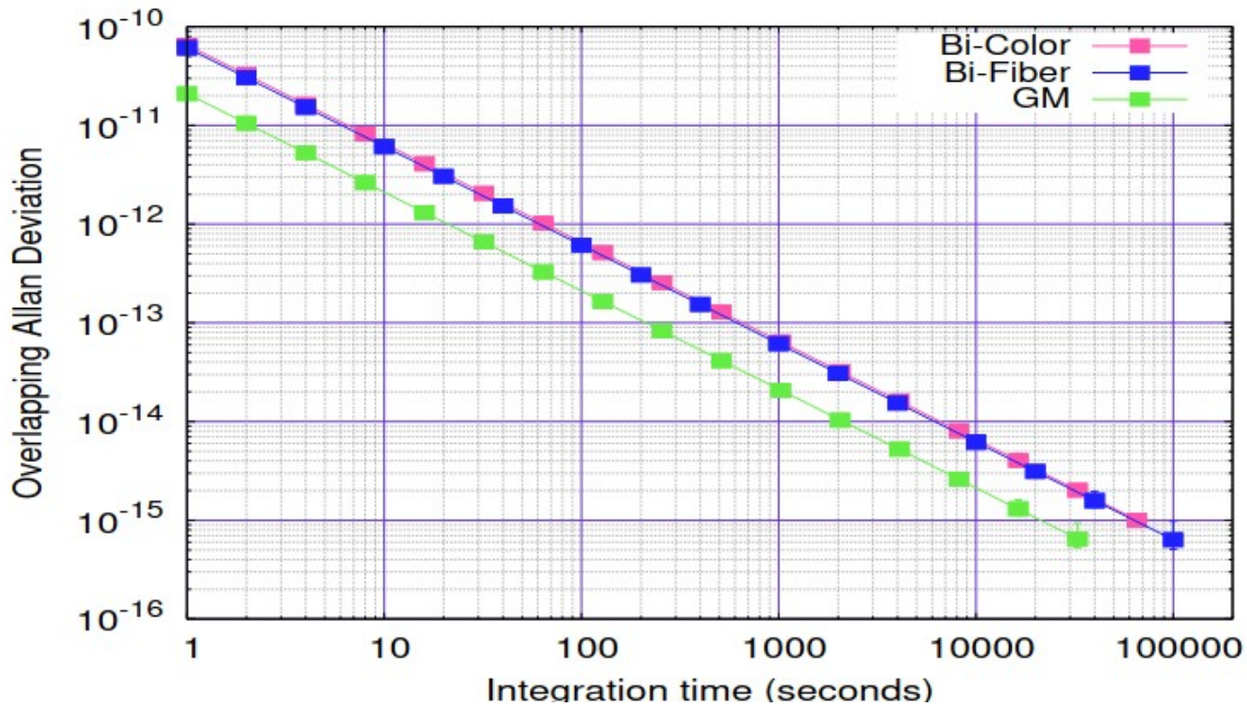
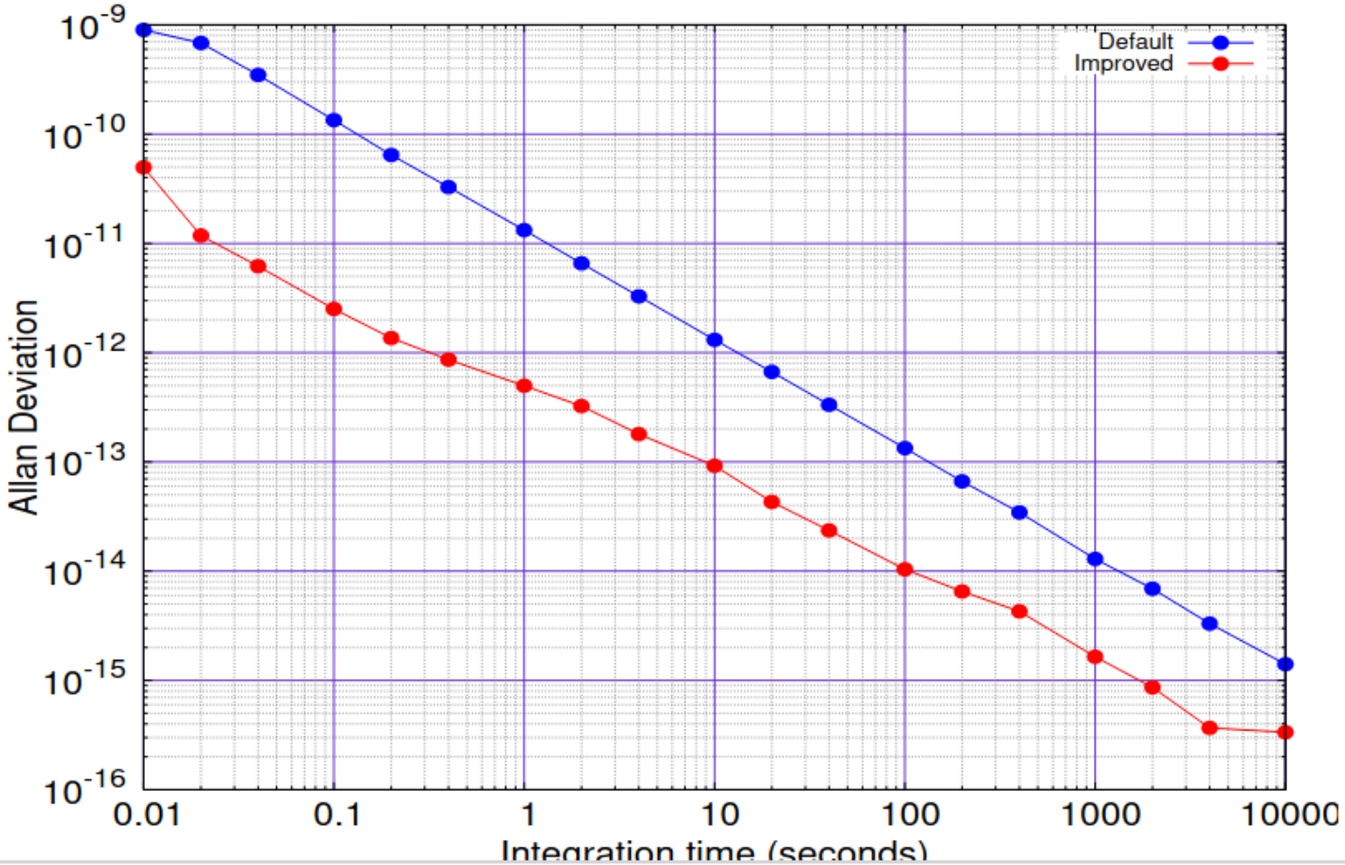


FIGURE 3.15: Phase data for the uni-directional (Bi-fiber) and bi-directional (Bi-color) setups.

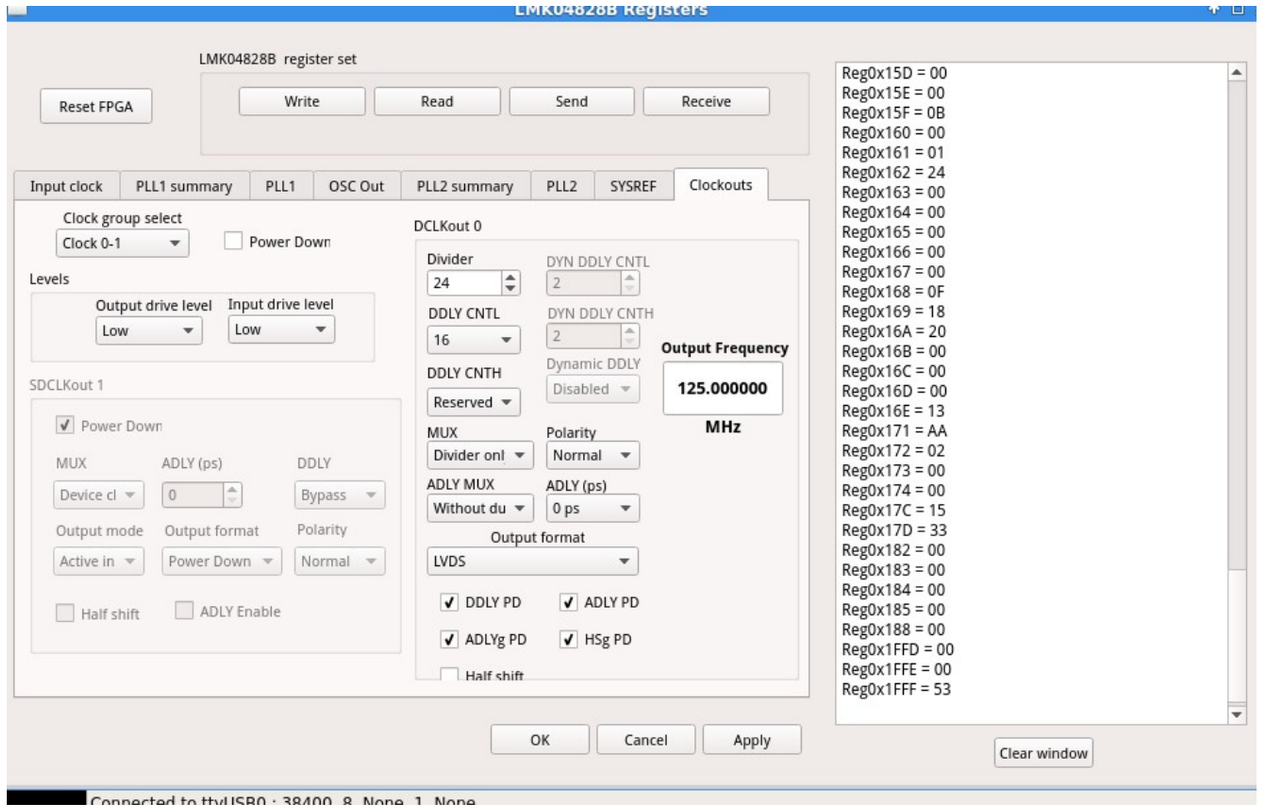


Ways to improve WR

- Increased PLL bandwith of the GM Local oscillator
- Better clocking scheme
- Better choice of components
- Decrease reponse time of the software PLL



IDROGEN Clock generator : LMK04828



- LMK04828
  - Frequency programmable 80MHz to 3 Ghz
  - Analog delay adjusment by 25ps step
  - ~ 100fs rms jitter
  - JESD20B compatible
  - Free runinng or synchro WR
  - Configure by µP.
  - Re-configuration by USB or Eth
  - Output clk on sma connector