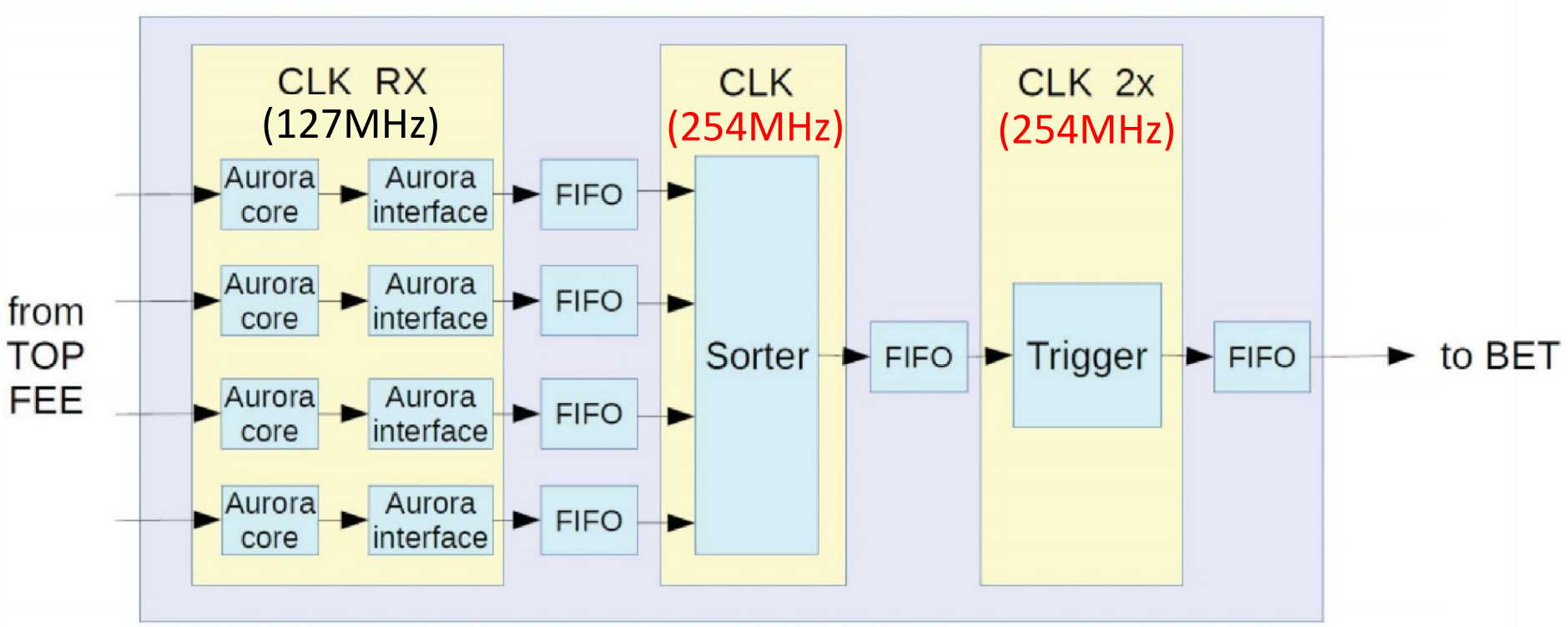
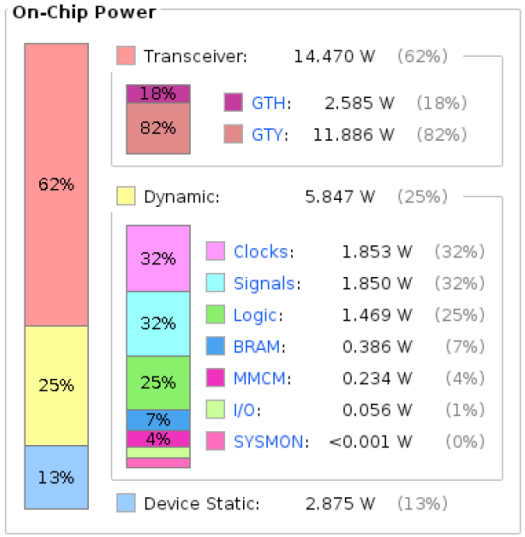

CLK RX
(127MHz)
CLK
(254MHz)
CLK 2x
(254MHz)
from
TOP
FEE
Aurora
core
Aurora
interface
FIFO
Sorter
Trigger
to BET

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**23.193 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**43.4°C**
Thermal Margin:	56.6°C (65.6 W)
Effective θJA:	0.8°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

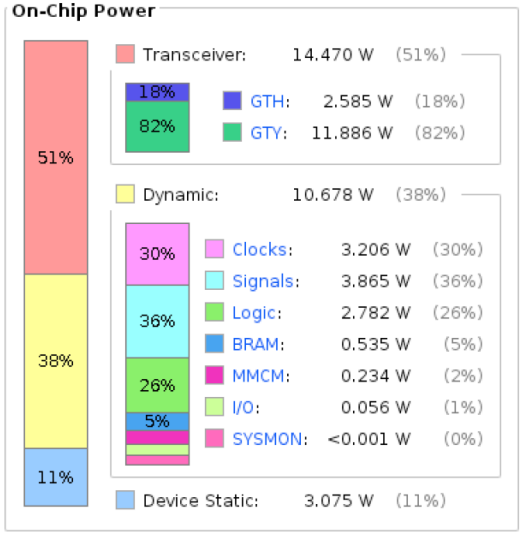
Launch Power Constraint Advisor to find and fix invalid switching activity



Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**28.224 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**47.4°C**
Thermal Margin:	52.6°C (60.8 W)
Effective θJA:	0.8°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

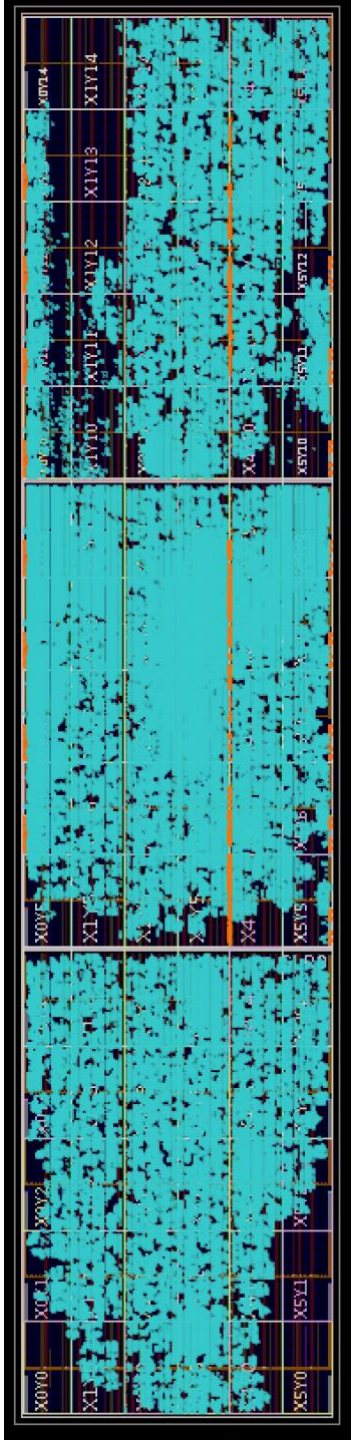
Launch Power Constraint Advisor to find and fix invalid switching activity



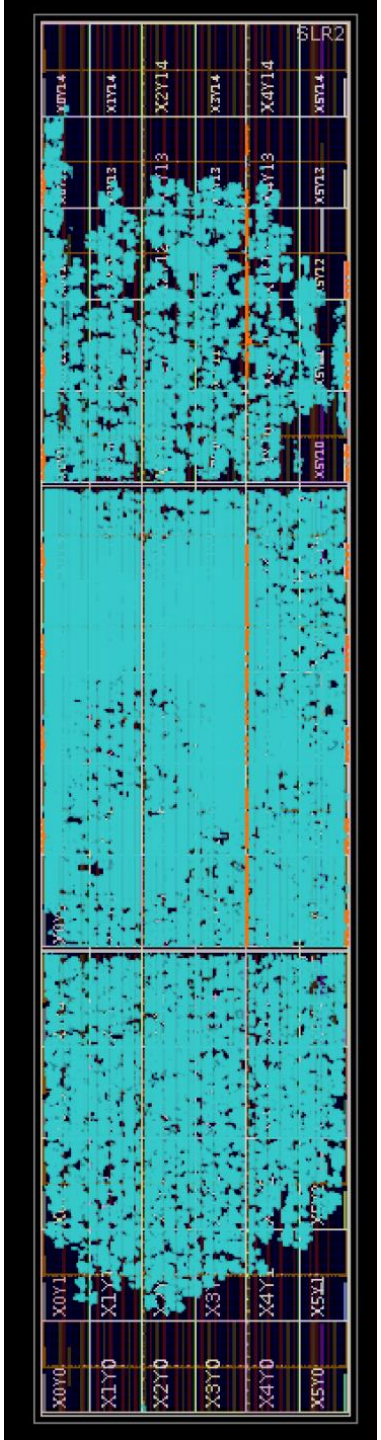
Total Power:
23.2W -> 28.2W

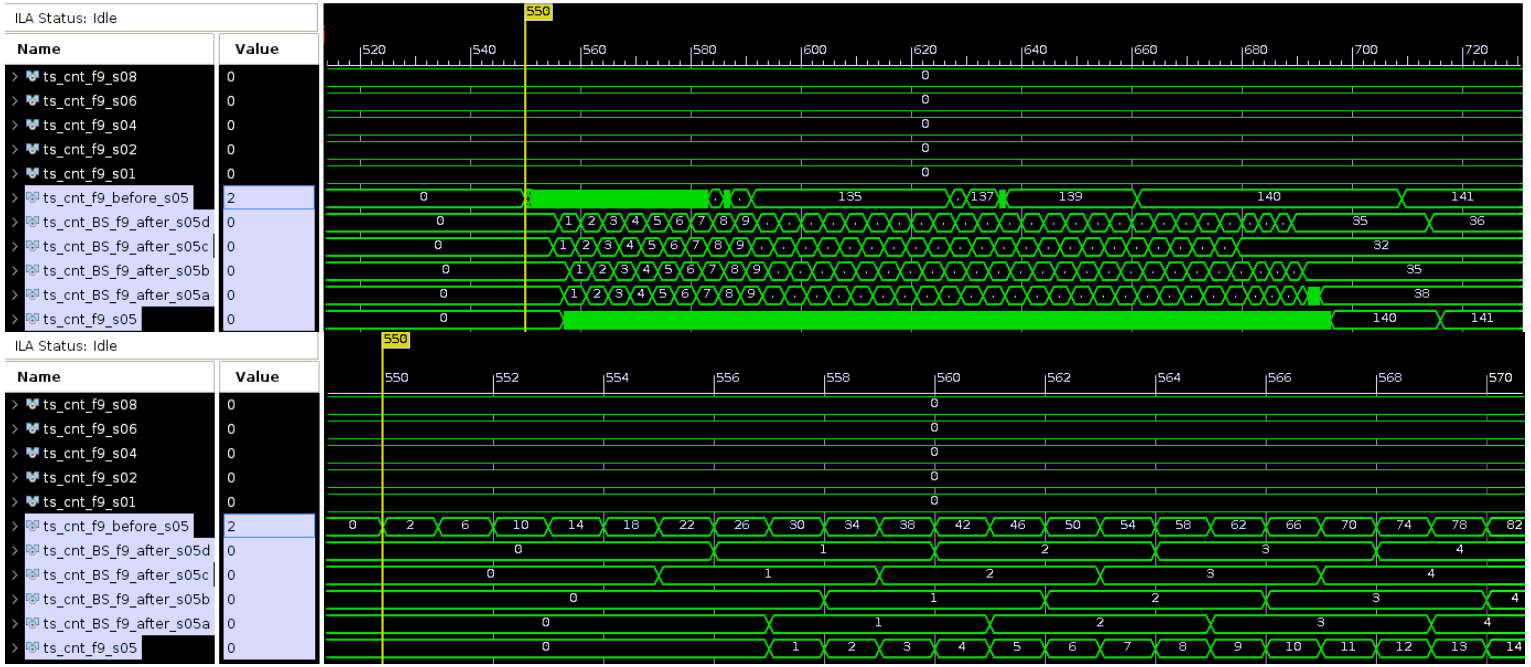
Temperature Test on UT4:
0x43 Left: 69 deg -> 74 deg
0x6d Right: 62 deg -> 67 deg

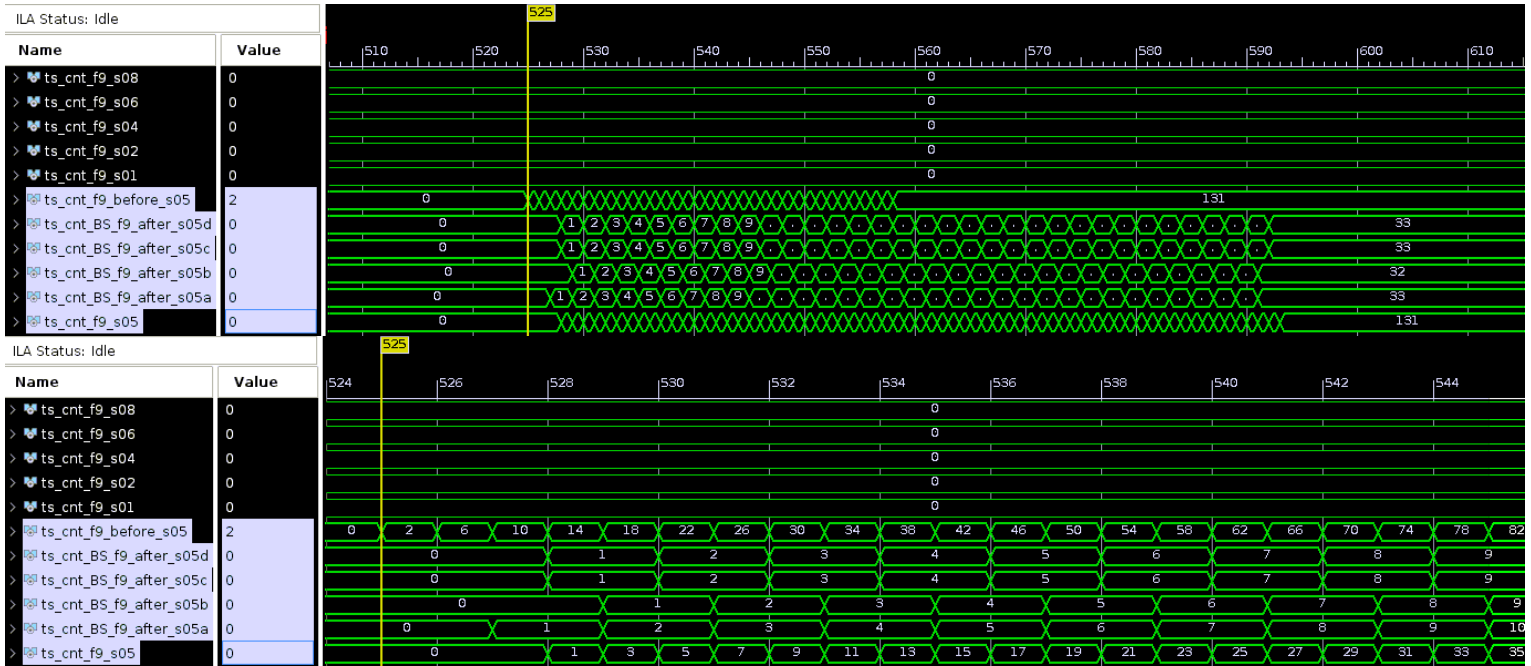
127MHz

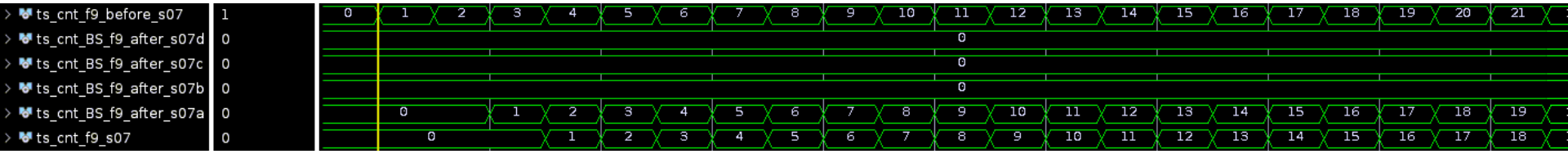


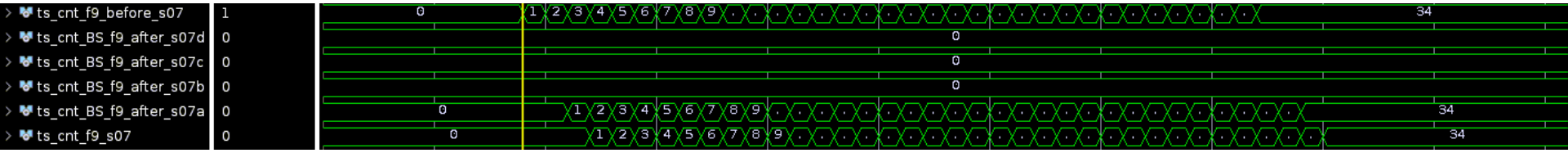
254MHz

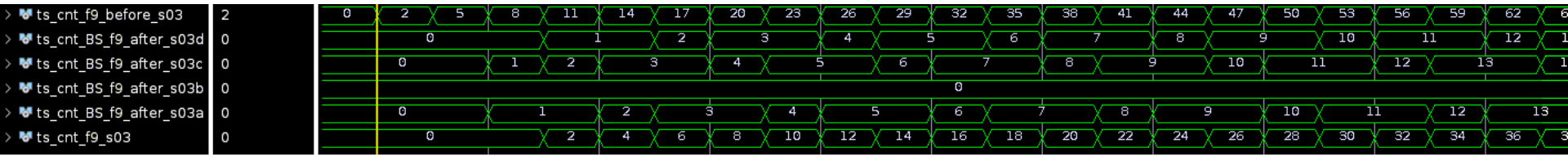


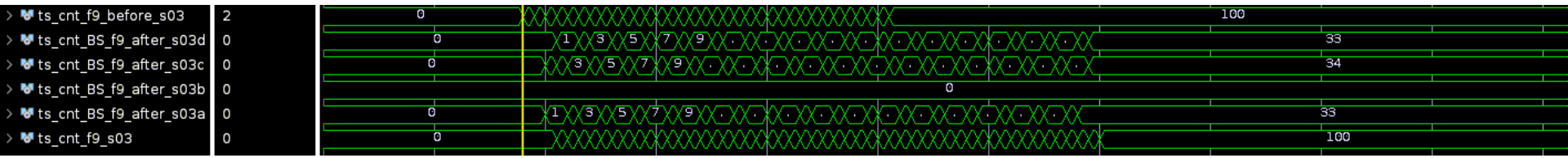

ILA Status: Idle
Name
Value
ts_cnt_f9_s08
ts_cnt_f9_s06
ts_cnt_f9_s04
ts_cnt_f9_s02
ts_cnt_f9_s01
ts_cnt_f9_before_s05
ts_cnt_BS_f9_after_s05d
ts_cnt_BS_f9_after_s05c
ts_cnt_BS_f9_after_s05b
ts_cnt_BS_f9_after_s05a
ts_cnt_f9_s05
550
ILA Status: Idle
Name
Value
550


ILA Status: Idle
Name
Value
ts_cnt_f9_s08
ts_cnt_f9_s06
ts_cnt_f9_s04
ts_cnt_f9_s02
ts_cnt_f9_s01
ts_cnt_f9_before_s05
ts_cnt_BS_f9_after_s05d
ts_cnt_BS_f9_after_s05c
ts_cnt_BS_f9_after_s05b
ts_cnt_BS_f9_after_s05a
ts_cnt_f9_s05
525
ILA Status: Idle
Name
Value
525


ts_cnt_f9_before_s07
ts_cnt_BS_f9_after_s07d
ts_cnt_BS_f9_after_s07c
ts_cnt_BS_f9_after_s07b
ts_cnt_BS_f9_after_s07a
ts_cnt_f9_s07


ts_cnt_f9_before_s07
ts_cnt_BS_f9_after_s07d
ts_cnt_BS_f9_after_s07c
ts_cnt_BS_f9_after_s07b
ts_cnt_BS_f9_after_s07a
ts_cnt_f9_s07


ts_cnt_f9_before_s03
ts_cnt_BS_f9_after_s03d
ts_cnt_BS_f9_after_s03c
ts_cnt_BS_f9_after_s03b
ts_cnt_BS_f9_after_s03a
ts_cnt_f9_s03


ts_cnt_f9_before_s03
ts_cnt_BS_f9_after_s03d
ts_cnt_BS_f9_after_s03c
ts_cnt_BS_f9_after_s03b
ts_cnt_BS_f9_after_s03a
ts_cnt_f9_s03